思 澈 科 技

SF32LB55x

Datasheet

V1.7.2

DS5501-SF32LB55x-EN

SiFli Technologies (Nanjing) Co., Ltd.
http://www.sifli.com

Revision History

Document Status

Document Status	Version Range	Description
Draft	0.0.0 ~0.9.9	Initial draft, informal release. The information is preliminary data, reflecting the specifications and performance of the product before mass production. No warranty is made as to the accuracy and the content is subject to change at any time without notice.
Release	1.0.0 ~1.9.9	Official release, and minor amendments might be made to the information to more accurately reflect the specifications and performance of mass-produced products; SiFli reserves the right to make changes to the document at any time without notice.

Revision History

Date	Version	Release Notes
2025-04-01	1.7.2	Added I/O characteristics table
2025-03-10	1.7.1	Updated the data bit width description that SPI can support
2024-11-06	1.7	Update description of peripheral I2S
2024-06-20	1.6	Updated SF32LB557 information to reflect VD3A6, and removed outdated content
2024-06-20	1.5	Added SF32LB557VD3A6 BGA169 Pin Layout
2024-05-16	1.4	Updated information of GPADC and temperature sensor
2024-05-07	1.3	Added ordering information
2024-03-07	1.2	Added IO drive strength information
2024-02-27	1.1	Adjusted table formats
2024-01-25	1.0	Updated Tstorage temperature range
2022-11-18	0.9	Added PSA Certified Level 1
2022-09-21	0.8	Revised details
2022-09-05	0.7	Updated data of power consumption
2022-08-26	0.6	Optimized typesetting
2022-08-15	0.5	Improved details
2022-05-23	0.4	Corrected text description
2021-11-24	0.3	Added GPU information
2021-06-30	0.2	Corrected typos
2021-06-24	0.1	Initial draft

Product Overview

SF32LB55x is a family of highly integrated high-performance System-on-Chip (SoC) MCUs designed for ultra-low-power Artifical Intelligence of Things (AIoT) scenarios. SF32LB55x adopts the big.LITTLE architecture with Arm Cortex-M33 STAR-MC1 processors, combining the best-in-class 2.5D GPU, neural network accelerator, and Bluetooth Low Energy 5.2. SF32LB55x can be used in a wide variety of applications such as wearables, smart display terminals, and smart homes.

The high-performance processor ("big core") of SF32LB55x can operate at up to 240MHz, providing 360DMIPS of computing power, and 965 EEMBC CoreMark; the low-power processor ("LITTLE core") can operate at up to 48MHz, serving as low-power sensor hub and running the Bluetooth protocol stack at the same time. The big.LITTLE architecture brings the balance between compute performance required for Human-Machine Interface (HMI) and power efficiency for sensor operations.

SF32LB55x integrates a world-class BLE5.2 transceiver, supporting 125kbps/500kbps/1Mbps/2Mbps modes. The maximum transmit power is 10dBm, the receiver has a peak power consumption of 2mA@3.3V, and sensitivity of -100dBm (1Mbps), with the link budget reaching 110dB.

SF32LB55x has rich internal and external memories. The high-performance processor has up to 1152KB SRAM, while the low-power processor has 256KB SRAM and 384KB ROM. The fully packaged chip has four QSPI memory interfaces, dedicated OPI-PSRAM interface, and SD/eMMC interfaces, which can be accessed by the big or LITTLE core processor depending on the requirements of task.

SF32LB55x provides a full range of display interfaces, including 8080, SPI/Dual-SPI/Quad-SPI, DPI, JDI interfaces, and MIPI-DSI (with extra QSPI for Always On Display), supporting 1024×1024, aRGB8888, and up to 60fps.

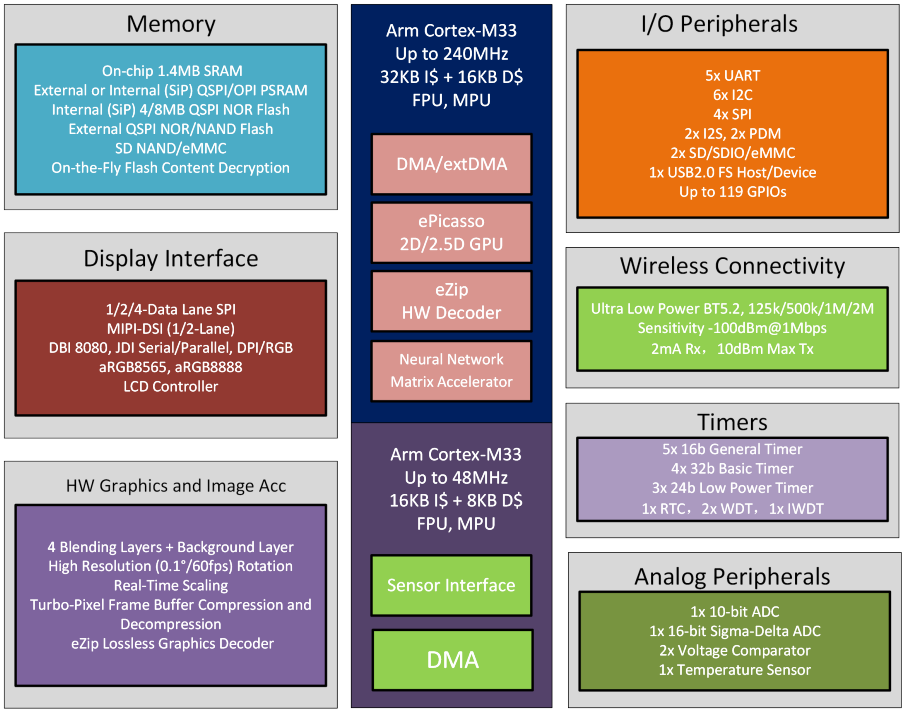


Figure 0-1: Functional Block Diagram

Product Features

CPU and Memory

- High-Performance Processor/ Big Core (HCPU)
  - Processor: Arm Cortex-M33 STAR-MC1
  - CPU Clock Speed: up to 240MHz, adjustable
  - Max. 360DMIPS, 965 EEMBC CoreMark
  - I/D-TCM: 64KB (dedicated)+128KB (shared with SRAM)
  - I/D-Cache: 32KB (2-way)+16KB (4-way)
  - SRAM: 1088KB (64 KB retention SRAM)
  - ROM: 64KB
  - CoreMark Power (@3.3V):
    - 34uA/MHz
    - 8.46uA/CoreMark
    - 118CoreMark/mA
  - Single Precision Floating Point Unit (FPU)
  - Memory Protection Unit (MPU)
  - Neural Network Co-Processor
- Low-Power Processor/ LITTLE Core (LCPU)
  - Processor: Arm Cortex-M33 STAR-MC1
  - CPU Clock Speed: up to 48MHz, adjustable
  - Max. 72DMIPS, 193 EEMBC CoreMark
  - I/D-TCM: 16KB (dedicated)+16KB (dedicated)
  - I/D-Cache: 16KB (2-way)+8KB (4-way)
  - SRAM: 224KB (all retention SRAM)
  - ROM: 384KB
  - CoreMark Power (@3.3V):
    - 11.8uA/MHz
    - 2.93uA/CoreMark
    - 341CoreMark/mA
  - Single Precision Floating Point Unit (FPU)
  - Memory Protection Unit (MPU)
  - Neural Network Co-Processor

Wireless Connectivity

- Bluetooth Low Energy 5.2: 125Kbps, 500Kbps, 1Mbps, 2Mbps
- Sensitivity at 1Mbps mode: -100dBm
- Max. transmit power: 10dBm
- Single antenna output, on-chip Balun, no external matching needed
- Rx peak power consumption: 2.0mA@3.3V
- Tx power consumption @0dBm: 2.6mA@3.3V
- Average power (3.3V, 200ms interval, Tx@0dBm):
  - ADV mode: 43.0uA
  - Connected mode: 30.1uA

2.5D GPU – ePicasso™

- 4-layer alpha blending +1 background layer architecture: 1 transform layer, 3 generic layers, 1 background layer
- Transform layer: Max. resolution 640×640, hardware-accelerated rotation, scaling and mirroring
- Generic layer: Max. resolution 1024×1024
- Support concatenated operation with eZip™, including transform layer operations
- Industry leading blending throughput performance: up to 1.5 cycle/pixel
- Support RGB565, RGB888, aRGB565, aRGB888, and alpha blending

Lossless Decompression Accelerator – eZip™

- Hardware decoding of proprietary lossless graphics compression format, compression ratio comparable to PNG
- Support generic data decompression, compression ratio comparable to gzip
- Independent DMA mode, for memory-to-memory image decompression
- Concatenated operation mode with ePicasso™, no need to buffer decompressed image in memory to complete ePicasso™operations

LCD Controller in High-Performance Domain

- MIPI-DBI: 8080, SPI, Dual-SPI, Quad-SPI
- Support MIPI-DPI
- MIPI-DSI: up to two data lanes, each supporting up to 240MHz/480Mbps
- JDI serial and parallel reflective display interfaces
- Support two-layer alpha blending, and solid color background layer
- TurboPixel™frame buffer decompression: hardware compression by extDMA, and decompression by the LCD controller, to enable high frame rate output with limited bandwidth

- Support RGB565, RGB888, aRGB565, aRGB888, and alpha blending

LCD Controller in Low-Power Domain

- MIPI-DBI: SPI/Dual-SPI/Quad-SPI for Always On Display (AOD)
- Support two-layer alpha blending, and solid color background layer
- Support RGB565, RGB888, aRGB565, aRGB888, and alpha blending
- Works with low-power processor/ LITTLE core, no high-performance processor/big core required

Neural Network Matrix Accelerator

- Highly efficient matrix convolution operation for TinyML scenarios and seamless API interface with Arm CMSIS-NN for easy porting of different neural network framework
- Independent bus interface and fully pipelined computing to maximize data throughput
- Max. processing power: up to 1.92GOPS
- Power consumption efficiency: up to 5.73TOPS/W

DMA

- General purpose DMA: support high-efficiency data transfer between internal memory and peripherals
- ExtDMA: for high-efficiency data transfer between internal memory and external memory, support TurboPixel™frame buffer compression, coupled with the decompression function of the LCD controller

Security

- AES accelerator
  - Symmetric encryption and decryption, support AES128, AES192, AES256 and SM4
  - Encryption and decryption modes including ECB, CTR and CBC
  - AES processes the source data in DMA mode, and writes data back to destination address
  - Support external Key, as well as Root Key
- CRC: Support fully programmable 7/8/16/32-bit generation polynomial, support 8/16/32-bit input data width, and can be driven by CPU or DMA for the CRC calculation
- True Random Number Generator (TRNG)
- Secure Boot
- 1024-bit eFuse to store Root of Trust and UID
- PSA Certified Level 1

Memory Interfaces

- 4×QSPI
  - Support QSPI-NOR Flash, QSPI-NAND Flash, or QSPI-PSRAM, Max. frequency 96MHz
  - QSPI1 is specially used for SiP flash
  - QSPI1/QSPI2 can be extended to dual QSPI-NOR Flash interface, to achieve 8-data lane throughput performance
  - QSPI1/QSPI2/QSPI4 support on-the-fly decryption (AES128-CTR or AES256-CTR) when fetching code from NOR Flash
  - QSPI4 is specially used for resouce extension of low-power processor/ LITTLE core, support NOR Flash or QSPI-PSRAM in specific application scenarios
- 1×OPI-PSRAM interface: support DDR, can be configured to 8-bit PSRAM interface, or be expanded to a set of 16-bit PSRAM interface by two sets of 8-bit PSRAM
- 2×SD/SDIO/eMMC (1×8b and 1×4b), support SD3.0, SDIO3.0, and eMMC4.51

Timers

- 5×16b General Purpose Timer (GPTIM)
- 4×32b Basic Timer (BTIM)
- 3×24b Low-Power Timer (LPTIM)
- 1×Real Time Clock (RTC)
- 2×24b Watch Dog Timer (WDT)
- 1×Independent Watch Dog Timer (IWDT)

Analog Peripherals

- 1×10-bit general purpose SAR ADC, up to 8 channels
- 1×16-bit Sigma-Delta ADC, up to 5 channels
- 1×On-chip temperature sensor
- 2×Low-power voltage comparator

I/O Peripherals

- Up to 119GPIOs
- 5×UART
- 6× I^2C
- 4×SPI
- 2× I^2S

- 2× PDM
- 1×USB2.0 FS Host/Device
- Peripheral Task Controller (PTC)

Power Management

- Input voltage: 1.7V – 3.6V
- Two on-chip high-efficiency bucks and low-power LDO
- Sleep current at RTC wake-up configuration: 600nA
- Sleep current at pin wake-up configuration: 280nA

Others

- Operation temperature: -40°C to 85°C
- Multiple package options available, providing rich GPIOs and interfaces for high-performance (HCPU) domain and low-power (LCPU) domain
  - BGA169, 119 (HCPU71+LCPU48) GPIOs, 7mm × 7mm × 0.94mm, 0.5mm pitch
  - BGA145, 95 (HCPU55+LCPU40) GPIOs, 7mm × 7mm × 0.94mm, 0.5mm pitch
  - BGA125, 84 (HCPU52+LCPU32) GPIOs, 7mm × 7mm × 0.94mm, 0.5mm pitch
  - QFN68L, 49 (HCPU28+LCPU21) GPIOs, 7mm × 7mm × 0.75mm, 0.35mm pitch

Applications

Smart Wearable

- Smart watch
- Smart wristband
- Wearable medical device
- Fitness equipment

Industrial Device

- Cost-effective display solution
- Graphical Human-Machine Interface (HMI) device
- Industrial sensor hub
- Industrial equipment monitoring
- Industrial instrumentation

Home Automation

- Smart lighting
- Smart home appliance
- Smart door lock
- Voice and gesture remote
- Stylus pen for pad, tablet PC, and smartphone

Generic Scenario

- Low-power sensor hub
- Bluetooth mesh

Product Series

Table 0-1: SF32LB55x Product Series

Function		SF32LB551	SF32LB553	SF32LB555	SF32LB557
Package	Type	QFN68L	BGA125	BGA145	BGA169
	Dimension (mm×mm×mm)	7×7×0.75	7×7×0.94	7×7×0.94	7×7×0.94
	Pitch (mm)	0.35	0.5	0.5	0.5
High-Performance Processor(HCPU)	Processor	Cortex-M33 STAR-MC1@240MHz			
	Cache	32KB-I$, 16KB-D$			
	TCM	64KB ITCM + 128KB DTCM[1]			
	SRAM	1088KB (Including 64KB Retention SRAM)			
	ROM	64KB			
	SiP PSRAM	4MB OPI(DDR)	4MB OPI(DDR)	4/8MB OPI(DDR)	16MB OPI(DDR)
	SiP Flash	4MB QSPI	4MB QSPI	4MB QSPI	1MB QSPI
	Off-chip Flash	QSPI	QSPI	QSPI	QSPI
	SDIO/eMMC	-	-	SD/eMMC ×1	SD/eMMC ×2
Low-Power Processor(LCPU)	Processor	Cortex-M33 STAR-MC1@48MHz			
	Cache	16KB-I$, 8KB-D$			
	TCM	16KB ITCM + 16KB DTCM			
	RAM	224KB （All Retention SRAM）			
	ROM	384KB			
	SiP PSRAM	-	-	-	2MB QPI
	Off-chip Flash	-	-	QSPI (shared)	-
Graphics	Graphics acceleration	ePicasso™ high performance 2.5D GPU @240MHz			
	Lossless compression	eZip™ decompression @240MHz			
	Display interface	SPI/DSPI/QSPI/8080		SPI/DSPI/QSPI/8080/MIPI-DSI/DPI/JDI	
	Always On Display	-		QSPI (shared)	DSPI (dedicated)
Power Management	Buck1	Y			
	Buck2	-	Y		
Bluetooth Low Energy	Protocol	BT5.2			
	Sensivitity	-100dBm			
	Rx power @3.3V	2.0mA			
	Max. Tx power	10dBm			
Timers (HCPU+LCPU)	16b GPTIM	2+3	2+3	2+3	2+3
	32b BTIM	2+2	2+2	2+2	2+2
	24b LPTIM	1+2	1+2	1+2	1+2
	RTC	1	1	1	1
	24b WDT	1+1	1+1	1+1	1+1
	IWDT	1	1	1	1
Analog Peripherals (HCPU+LCPU)	SAR ADC (8-ch)	0+1	0+1	0+1	0+1
	Sigma-Delta ADC (5-ch)	0+1	0+1	0+1	0+1
	Temperature Sensor	0+1	0+1	0+1	0+1
	LP COMP	0+2	0+2	0+2	0+2
I/O Peripherals (HCPU+LCPU)	GPIO	28+21	52+32	55+40	71+42
	UART	1+1	1+2	2+3	2+3
	I2C	1+2	3+2	3+2	3+3
	SPI	1+1	1+2	2+2	2+2
	I2S	1+0	1+0	1+0	2+0
	PDM	1+0	1+0	1+0	2+0
	SDIO/eMMC	1+0	1+0	1+0	2+0
	USB 2.0 FS	1+0	1+0	1+0	1+0

[1] ITCM: dedicated SRAM; DTCM: shared with SRAM

Contents

List of Figures

List of Tables

1 Introduction

1.1 System Architecture

SF32LB55x is a family of highly integrated and cost-effective System-on-Chip (SoC) MCUs desgined for ultra-low-power Artifical Intelligence of Things (AIoT) scenarios. SF32LB55x adopts the big.LITTLE architecture with two Arm Cortex-M33 STAR-MC1 processors.

- High-Performance Processor/Big Core (HCPU): CPU clock speed up to 240MHz, 32KB instruction cache (I-Cache) and 16KB data cache (D-Cache), 64KB ITCM, 128KB DTCM, 1088KB co-frequency SRAM (of which128KB is shared with D-Cache and 64KB is Retention RAM) and 384KB ROM; as the system master, it can efficiently access internal and external memory and is mainly used for system control, Human-Machine Interaction, and high-performance computing.
- Low-Power Processor/LITTLE Core (LCPU): CPU clock speed up to 48MHz, 16KB instruction cache (I-Cache) and 8KB data cache (D-Cache), 16KB ITCM, 16KB DTCM, 224KB low-power SRAM (all Retention RAM), and 384KB low-power ROM; it is mainly used as the system's ultra-low-power sensor hub and Bluetooth Low Energy connectivity controller which can meet the requirements of data acquisition, processing, transmission and control in ultra-low-power scenarios.

1.2 Cortex-M33 STAR-MC1 Processor

Cortex-M33 STAR-MC1 processor is the first processor of the "Star" series from Arm China. It has the key features of Cortex-M33, supporting the full functionality of the existing Arm v8-M architecture, and with an in-order three-stage pipeline, it can significantly reduce the power consumption of the system. It also has partial dual-issue 16-bit instruction capability, and the coprocessor interface is further improved to support the Cache.

With the performance reaching 1.5DMIPS/MHz and 4.02Coremark/MHz, Cortex-M33 STAR-MC1 delivers a 20% performance improvement over previous-generation Arm processors at the same clock speed.

Cortex-M33 STAR-MC1 has a coprocessor interface which can further enhance the capability of customized calculation to meet the requirements of different scenarios. The MCR (Move from Coprocessor to Register) and MRC (Move from Register to Coprocessor) instructions enable the transfer of register data and computation results between Cortex-M33 STAR-MC1 and the coprocessor, making it ideal for operations with small data volumes, complex calculations but relatively fragmented and low latency. While the coprocessor computes, Cortex-M33 STAR-MC1 processor can still execute other instructions in parallel, thus significantly improving execution efficiency.

In addition, the processor supports Digital Signal Processing (DSP) instruction sets and Floating Point Unit (FPU).

Tightly Coupled Memory (TCM) and Cache technologies are adopted in Cortex-M33 STAR-MC1 processor to enhance flexibility in the use of internal and external memory systems with different characteristics, ensuring the real-time response and computational efficiency of the processor in a variety of scenarios.

1.3 High-Performance Processor (Big Core) System (HPSYS)

1.3.1 Bus Architecture

The HPSYS provides an internal bus matrix based on the AHB protocol, which supports multiple master devices to access the address spaces of multiple slave devices in parallel. As shown in Figure 1-1, the master devices of the bus are located on the top side and the address spaces of the slave devices are located on the right side, and the black dots at the intersection represent bus connectivity.

The HCPU has access to all address spaces of the HPSYS and can access all address spaces of the LPSYS through HP2LP.

DMAC1 can access all address spaces of HPSYS except HPSYS_ITCM and Retention RAM, and can access all address spaces of LPSYS except LPSYS_DTCM through HP2LP.

Some master devices (LCPU and DMAC2) of the LPSYS can access the address spaces of QSPI1~3, the address spaces of HPSYS_RAM0~5, and all HPSYS_APB peripherals through LP2HP.

The address spaces of HPSYS_ITCM and Retention RAM are only accessible by the HCPU, which are not listed in the figure. 128KB address space is shared between DTCM and HPSYS_RAM0, and can be accessed by the HCPU and other master devices.

When multiple master devices access the address space of the same slave device at the same time, the access order will be determined based on the polling arbitration principle. As shown in the figure, when multiple master devices with unconnected borders access the address spaces of different slave devices at the same time, they will not be affected by each other. When two master devices with connected borders initiate access at the same time, LCDC1 has a fixed priority over AES, and the access order of other master devices will be decided based on the polling arbitration principle.

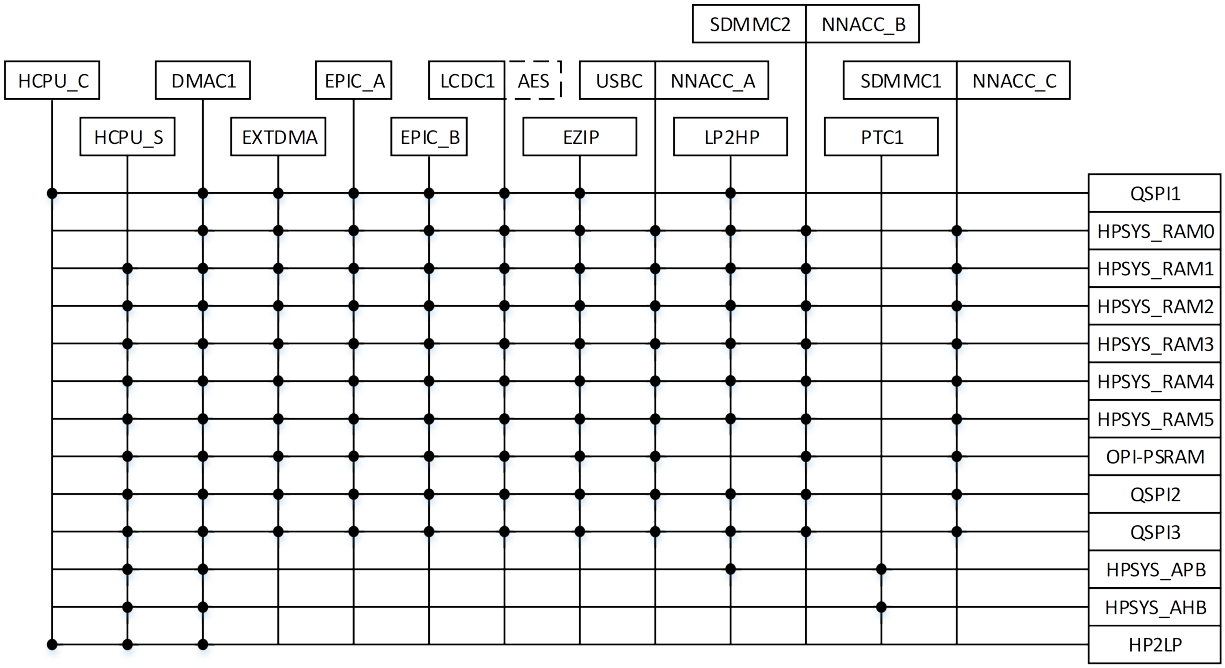


Figure 1-1: Bus Architecture of HPSYS

1.3.2 Clock Architecture

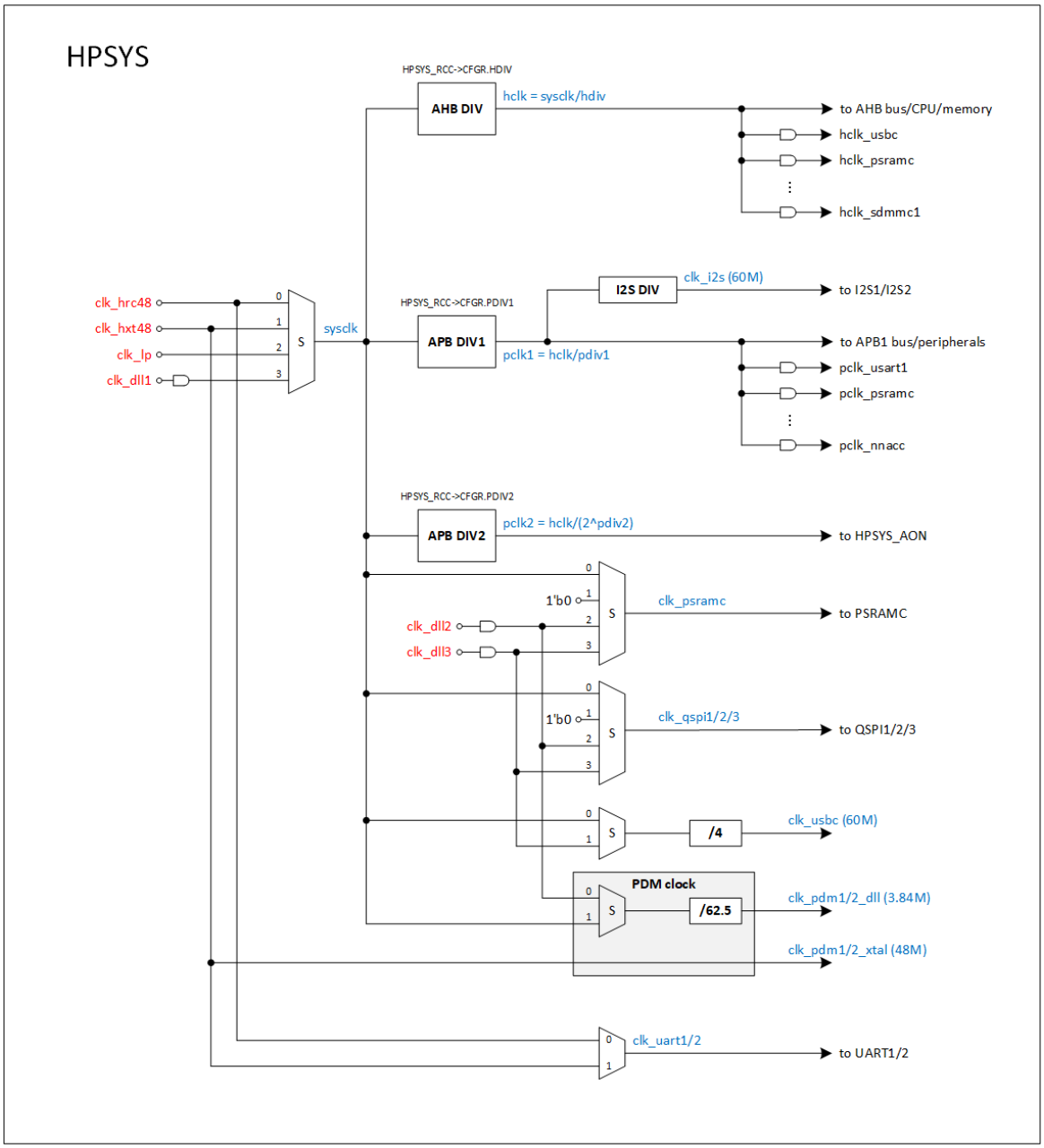


Figure 1-2: Clock Architecture of HPSYS

1.3.3 Memory Type

1.3.3.1 Cache

The HCPU has 32KB 2-way I-Cache (Level 1 instruction cache) and 16KB 4-way D-Cache (Level 1 data cache), which can greatly improve CPU execution efficiency during XIP. The MPU (Memory Protection Unit) should be configured appropriately to set the cache address segment and non-cache address segment to balance efficiency and ease of use.

1.3.3.2 TCM

The HCPU has 64KB zero-wait-cycle I-TCM with address space 0x0001_0000-0x0001_FFFF. This TCM memory is exclusive to the HCPU and cannot be accessed by other AHB masters. It can be used to place codes and data with high real-time (or delay determinism) requirements.

The HCPU also has 128KB zero-wait-cycle D-TCM with address space 0x2000_0000-0x2001_FFFF. This TCM memory is connected to the bus and can also be accessed by other AHB masters.

1.3.3.3 SRAM

There is a total of 1088KB SRAM on the HPSYS bus, which includes:

- 1024KB zero-wait-cycle SRAM with address space 0x2000_0000 -0x200F_FFFF (the first 128KB shared with DTCM), accessible to all AHB masters. Maximum frequency is 240MHz, which can maximize CPU performance.
- 64KB Retention SRAM with address space 0x0002_0000-0x0002_FFFF, accessible to the HCPU, maximum frequency 120MHz.

1.3.3.4 Off-chip RAM

The HPSYS supports external OPI DDR pSRAM with address space 0x6000_0000 - 0x63FF_FFFF, the actual accessible address is determined by the capacity of the external particles. The maximum interface frequency is DDR 120MHz and the data bit width is 8-bit.

1.3.3.5 Off-chip Flash

The HPSYS supports multiple external NOR/NAND FLASHs, in which

- 0x1000_0000-0x11FF_FFFF address segment for accessing SIP FLASH with a maximum interface frequency of 96MHz
- 0x6400_0000-0x67FF_FFFF address segment can be connected to FLASH2, recommended frequency is 60MHz
- 0x6800_0000-0x6FFF_FFFF address segment can be connected to FLASH3, recommended frequency is 60MHz

1.3.4 Address Mapping

Table 1-1: Address Mapping of HPSYS

Category	Memory/IP	Address Space	HCPU Address Space		LCPU Address Space	
			Starting Address	Ending Address	Starting Address	Ending Address
HPSYS_ITCM	ROM	64KB	0x0000_0000	0x0000_FFFF		
	RAM	64KB	0x0001_0000	0x0001_FFFF		
Retention RAM		64KB	0x0002_0000	0x0002_FFFF		
XIP Memory	QSPI1 Memory	32MB	0x1000_0000	0x11FF_FFFF	0x1000_0000	0x11FF_FFFF
HPSYS_RAM (1024KB) 0x2000_0000 0x200F_FFFF	HPSYS_RAM0	128KB	0x2000_0000	0x2001_FFFF	0x2A00_0000	0x2A01_FFFF
	HPSYS_RAM1	128KB	0x2002_0000	0x2003_FFFF	0x2A02_0000	0x2A03_FFFF
	HPSYS_RAM2	128KB	0x2004_0000	0x2005_FFFF	0x2A04_0000	0x2A05_FFFF
	HPSYS_RAM3	128KB	0x2006_0000	0x2007_FFFF	0x2A06_0000	0x2A07_FFFF
	HPSYS_RAM4	256KB	0x2008_0000	0x200B_FFFF	0x2A08_0000	0x2A0B_FFFF
	HPSYS_RAM5	256KB	0x200C_0000	0x200F_FFFF	0x2A0C_0000	0x2A0F_FFFF

Continued on the next page

Table 1-1: Address Mapping of HPSYS (continued)

Category	Memory/IP	Address Space	HCPU Address Space		LCPU Address Space	
			Starting Address	Ending Address	Starting Address	Ending Address
HPSYS_APB1 (192KB) 0x4000_0000 0x4002_FFFF	RCC1	4KB	0x4000_0000	0x4000_0FFF	0x4000_0000	0x4000_0FFF
	DMAC1	4KB	0x4000_1000	0x4000_1FFF	0x4000_1000	0x4000_1FFF
	MAILBOX1	4KB	0x4000_2000	0x4000_2FFF	0x4000_2000	0x4000_2FFF
	PINMUX1	4KB	0x4000_3000	0x4000_3FFF	0x4000_3000	0x4000_3FFF
	UART1	4KB	0x4000_4000	0x4000_4FFF	0x4000_4000	0x4000_4FFF
	UART2	4KB	0x4000_5000	0x4000_5FFF	0x4000_5000	0x4000_5FFF
	EZIP	4KB	0x4000_6000	0x4000_6FFF	0x4000_6000	0x4000_6FFF
	EPIC	4KB	0x4000_7000	0x4000_7FFF	0x4000_7000	0x4000_7FFF
	LCDC1	4KB	0x4000_8000	0x4000_8FFF	0x4000_8000	0x4000_8FFF
	I2S1	4KB	0x4000_9000	0x4000_9FFF	0x4000_9000	0x4000_9FFF
	I2S2	4KB	0x4000_A000	0x4000_AFFF	0x4000_A000	0x4000_AFFF
	SYSCFG1	4KB	0x4000_B000	0x4000_BFFF	0x4000_B000	0x4000_BFFF
	EFUSEC	4KB	0x4000_C000	0x4000_CFFF	0x4000_C000	0x4000_CFFF
	AES	4KB	0x4000_D000	0x4000_DFFF	0x4000_D000	0x4000_DFFF
	CRC	4KB	0x4000_E000	0x4000_EFFF	0x4000_E000	0x4000_EFFF
	TRNG	4KB	0x4000_F000	0x4000_FFFF	0x4000_F000	0x4000_FFFF
	GPTIM1	4KB	0x4001_0000	0x4001_0FFF	0x4001_0000	0x4001_0FFF
	GPTIM2	4KB	0x4001_1000	0x4001_1FFF	0x4001_1000	0x4001_1FFF
	BTIM1	4KB	0x4001_2000	0x4001_2FFF	0x4001_2000	0x4001_2FFF
	BTIM2	4KB	0x4001_3000	0x4001_3FFF	0x4001_3000	0x4001_3FFF
	WDT1	4KB	0x4001_4000	0x4001_4FFF	0x4001_4000	0x4001_4FFF
	SPI1	4KB	0x4001_5000	0x4001_5FFF	0x4001_5000	0x4001_5FFF
	SPI2	4KB	0x4001_6000	0x4001_6FFF	0x4001_6000	0x4001_6FFF
	EXTDMA	4KB	0x4001_7000	0x4001_7FFF	0x4001_7000	0x4001_7FFF
	PSRAMC	4KB	0x4001_8000	0x4001_8FFF	0x4001_8000	0x4001_8FFF
	NNACC	4KB	0x4001_9000	0x4001_9FFF	0x4001_9000	0x4001_9FFF
	PDM1	4KB	0x4001_A000	0x4001_AFFF	0x4001_A000	0x4001_AFFF
	PDM2	4KB	0x4001_B000	0x4001_BFFF	0x4001_B000	0x4001_BFFF
	I2C1	4KB	0x4001_C000	0x4001_CFFF	0x4001_C000	0x4001_CFFF
	I2C2	4KB	0x4001_D000	0x4001_DFFF	0x4001_D000	0x4001_DFFF
	DSIHOST	4KB	0x4001_E000	0x4001_EFFF	0x4001_E000	0x4001_EFFF
	DSIPHY	4KB	0x4001_F000	0x4001_FFFF	0x4001_F000	0x4001_FFFF
	PTC1	4KB	0x4002_0000	0x4002_0FFF	0x4002_0000	0x4002_0FFF
	BUSMON1	4KB	0x4002_1000	0x4002_1FFF	0x4002_1000	0x4002_1FFF
	I2C3	4KB	0x4002_2000	0x4002_2FFF	0x4002_2000	0x4002_2FFF
	Reserved	54KB	0x4002_3000	0x4002_FFFF	0x4002_3000	0x4002_FFFF
HPSYS_APB2 (64KB) 0x4003_0000 0x4003_FFFF	HPSYS_AON	4KB	0x4003_0000	0x4003_0FFF	0x4003_0000	0x4003_0FFF
	LPTIM1	4KB	0x4003_1000	0x4003_1FFF	0x4003_1000	0x4003_1FFF
	Reserved	4KB	0x4003_2000	0x4003_2FFF	0x4003_2000	0x4003_2FFF
	Reserved	4KB	0x4003_3000	0x4003_3FFF	0x4003_3000	0x4003_3FFF
	Reserved	48KB	0x4003_4000	0x4003_FFFF	0x4003_4000	0x4003_FFFF

Continued on the next page

Table 1-1: Address Mapping of HPSYS (continued)

Category	Memory/IP	Address Space	HCPU Address Space		LCPU Address Space	
			Starting Address	Ending Address	Starting Address	Ending Address
HPSYS_AHB (256KB) 0x5000_0000 0x5003_FFFF	GPIO1	4KB	0x5000_0000	0x5000_0FFF		
	QSPI1	4KB	0x5000_1000	0x5000_1FFF		
	QSPI2	4KB	0x5000_2000	0x5000_2FFF		
	QSPI3	4KB	0x5000_3000	0x5000_3FFF		
	SDMMC1	4KB	0x5000_4000	0x5000_4FFF		
	SDMMC2	4KB	0x5000_5000	0x5000_5FFF		
	USBC	4KB	0x5000_6000	0x5000_6FFF		
	Reserved	36KB	0x5000_7000	0x5000_FFFF		
	GFX_RAM	64KB	0x5001_0000	0x5001_FFFF		
	Reserved	128KB	0x5002_0000	0x5003_FFFF		
External Memory (256MB)	OPI-PSRAM	64MB	0x6000_0000	0x63FF_FFFF		
	QSPI2 Memory	64MB	0x6400_0000	0x67FF_FFFF	0x6400_0000	0x67FF_FFFF
	QSPI3 Memory	128MB	0x6800_0000	0x6FFF_FFFF	0x6800_0000	0x6FFF_FFFF

1.3.5 Interrupt List

Table 1-2: Interrupt List of HCPU

IRQ #	IRQ Source
HCPU_NMI	WDT1
HCPU_IRQ[0]	AON1
HCPU_IRQ[1]	LCPU_IRQ[1]
HCPU_IRQ[2]	LCPU_IRQ[2]
HCPU_IRQ[3]	LCPU_IRQ[3]
HCPU_IRQ[4]	LCPU_IRQ[4]
HCPU_IRQ[5]	LCPU_IRQ[5]
HCPU_IRQ[6]	LCPU_IRQ[6]
HCPU_IRQ[7]	LCPU_IRQ[7]
HCPU_IRQ[8]	LCPU_IRQ[8]
HCPU_IRQ[9]	LCPU_IRQ[9]
HCPU_IRQ[10]	LCPU_IRQ[10]
HCPU_IRQ[11]	LCPU_IRQ[11]
HCPU_IRQ[12]	LCPU_IRQ[12]
HCPU_IRQ[13]	LCPU_IRQ[13]
HCPU_IRQ[14]	LCPU_IRQ[14]
HCPU_IRQ[15]	LCPU_IRQ[15]
HCPU_IRQ[16]	LCPU_IRQ[16]
HCPU_IRQ[17]	LCPU_IRQ[17]
HCPU_IRQ[18]	LCPU_IRQ[18]
HCPU_IRQ[19]	LCPU_IRQ[19]
HCPU_IRQ[20]	LCPU_IRQ[20]
HCPU_IRQ[21]	LCPU_IRQ[21]
HCPU_IRQ[22]	LCPU_IRQ[22]
HCPU_IRQ[23]	LCPU_IRQ[23]
HCPU_IRQ[24]	LCPU_IRQ[24]
HCPU_IRQ[25]	LCPU_IRQ[25]
HCPU_IRQ[26]	LCPU_IRQ[26]
HCPU_IRQ[27]	LCPU_IRQ[27]

Continued on the next page

Table 1-2: Interrupt List of HCPU (continued)

IRQ #	IRQ Source
HCPU_IRQ[28]	LCPU_IRQ[28]
HCPU_IRQ[29]	LCPU_IRQ[29]
HCPU_IRQ[30]	LCPU_IRQ[30]
HCPU_IRQ[31]	LCPU_IRQ[31]
HCPU_IRQ[32]	LCPU_IRQ[32]
HCPU_IRQ[33]	LCPU_IRQ[33]
HCPU_IRQ[34]	LCPU_IRQ[34]
HCPU_IRQ[35]	LCPU_IRQ[35]
HCPU_IRQ[36]	LCPU_IRQ[36]
HCPU_IRQ[37]	LCPU_IRQ[37]
HCPU_IRQ[38]	LCPU_IRQ[38]
HCPU_IRQ[39]	LCPU_IRQ[39]
HCPU_IRQ[40]	LCPU_IRQ[40]
HCPU_IRQ[41]	LCPU_IRQ[41]
HCPU_IRQ[42]	LCPU_IRQ[42]
HCPU_IRQ[43]	LCPU_IRQ[43]
HCPU_IRQ[44]	LCPU_IRQ[44]
HCPU_IRQ[45]	LCPU_IRQ[45]
HCPU_IRQ[46]	LPTIM1
HCPU_IRQ[47]	Reserved
HCPU_IRQ[48]	Reserved
HCPU_IRQ[49]	RTC
HCPU_IRQ[50]	DMAC1_CH1
HCPU_IRQ[51]	DMAC1_CH2
HCPU_IRQ[52]	DMAC1_CH3
HCPU_IRQ[53]	DMAC1_CH4
HCPU_IRQ[54]	DMAC1_CH5
HCPU_IRQ[55]	DMAC1_CH6
HCPU_IRQ[56]	DMAC1_CH7
HCPU_IRQ[57]	DMAC1_CH8
HCPU_IRQ[58]	LCPU2HCPU
HCPU_IRQ[59]	UART1
HCPU_IRQ[60]	SPI1
HCPU_IRQ[61]	I2C1
HCPU_IRQ[62]	EPIC
HCPU_IRQ[63]	LCDC1
HCPU_IRQ[64]	I2S1
HCPU_IRQ[65]	I2S2
HCPU_IRQ[66]	EFUSEC
HCPU_IRQ[67]	AES
HCPU_IRQ[68]	PTC1
HCPU_IRQ[69]	TRNG
HCPU_IRQ[70]	GPTIM1
HCPU_IRQ[71]	GPTIM2
HCPU_IRQ[72]	BTIM1
HCPU_IRQ[73]	BTIM2
HCPU_IRQ[74]	UART2
HCPU_IRQ[75]	SPI2
HCPU_IRQ[76]	I2C2
HCPU_IRQ[77]	EXTDMA
HCPU_IRQ[78]	PSRAMC
HCPU_IRQ[79]	SDMMC1

Continued on the next page

Table 1-2: Interrupt List of HCPU (continued)

IRQ #	IRQ Source
HCPU_IRQ[80]	SDMMC2
HCPU_IRQ[81]	NNACC
HCPU_IRQ[82]	PDM1
HCPU_IRQ[83]	DSI
HCPU_IRQ[84]	GPIO1
HCPU_IRQ[85]	QSPI1
HCPU_IRQ[86]	QSPI2
HCPU_IRQ[87]	QSPI3
HCPU_IRQ[88]	EZIP
HCPU_IRQ[89]	PDM2
HCPU_IRQ[90]	USBC
HCPU_IRQ[91]	I2C3
HCPU_IRQ[92]	Reserved
HCPU_IRQ[93]	Reserved
HCPU_IRQ[94]	Reserved
HCPU_IRQ[95]	Reserved

1.4 Low-Power Processor (LITTLE Core) System (LPSYS)

1.4.1 Bus Architecture

The LPSYS provides an internal bus matrix based on the AHB protocol, which supports multiple master devices to access the address spaces of multiple slave devices in parallel.

As shown in Figure 1-3, the master devices of the bus are located on the top side and the address spaces of the slave devices are located on the right side, and the black dots at the intersection represent bus connectivity.

LCPU has access to all address spaces of LPSYS and can access the address spaces of QSPI1~3, HPSYS_RAM0~5, and all HPSYS_APB peripherals through LP2HP.

DMAC2 can access all address spaces of LPSYS except LPSYS_ROM, and can access the address spaces of QSPI1~3, HPSYS_RAM0~5, and all HPSYS_APB peripherals through LP2HP.

Some master devices (HCPU and DMAC1) of the HPSYS are able to access all address spaces of the LPSYS through HP2LP.

LPSYS_ITCM and LPSYS_DTCM can be accessed by LCPU and DMAC2, and also by some master devices (HCPU and DMAC1) of the HPSYS.

When multiple master devices access the address space of the same slave device at the same time, the access order will be determined based on the polling arbitration principle. When multiple master devices access the address spaces of different slave devices at the same time, they will not be affected by each other.

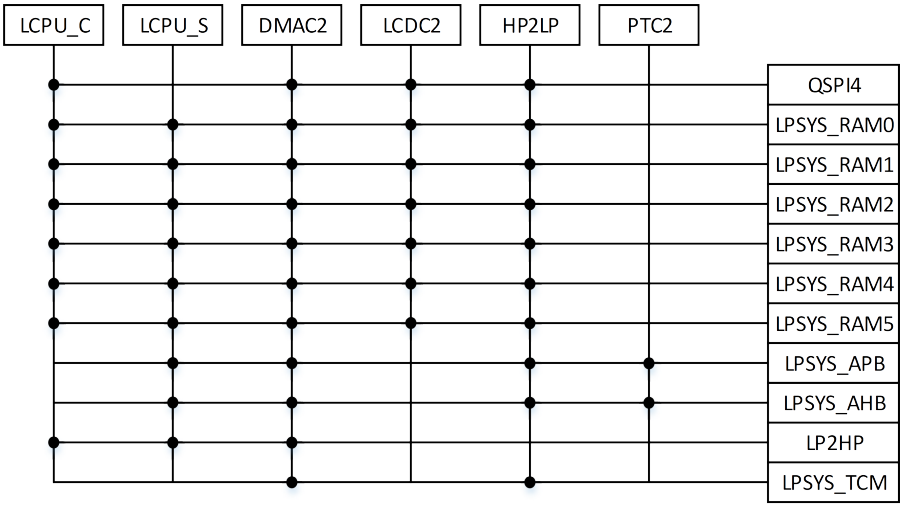


Figure 1-3: Bus Architecture of LPSYS

1.4.2 Clock Architecture

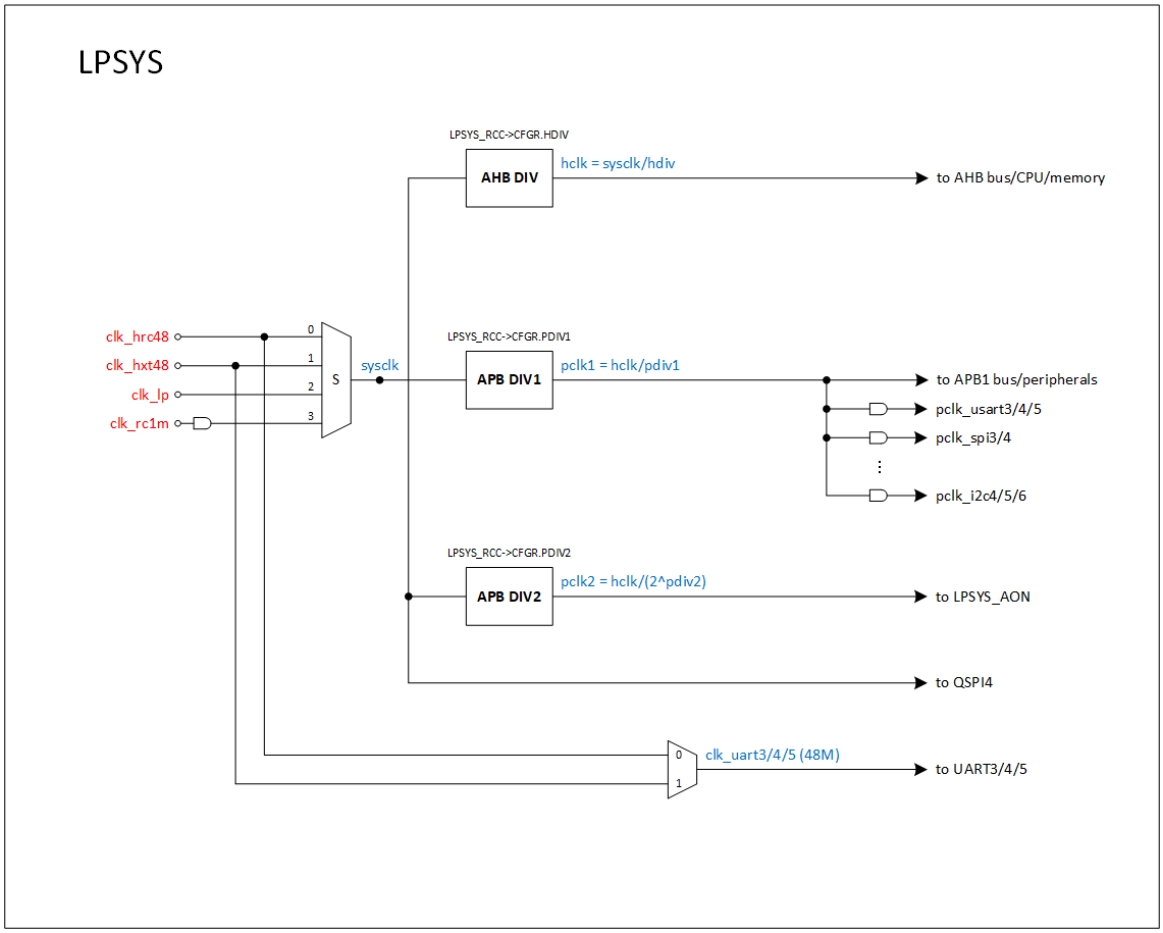


Figure 1-4: Clock Architecture of LPSYS

1.4.3 Memory Type

1.4.3.1 Cache

LCPU has 16KB 2-way I-Cache (Level 1 instruction cache) and 8KB 4-way D-Cache (Level 1 data cache).

1.4.3.2 TCM

LCPU has 16KB zero-wait-cycle I-TCM with address space 0x000F_C000-0x000F_FFFF. This TCM memory is exclusive to LCPU and can be initialized by HCPU via address segments 0x0B0F_C000 - 0x0B0F_FFFF. It is recommended to place codes and data with high real-time (or delay determinism) requirements.

LCPU also has 16KB zero-wait-cycle D-TCM with address space 0x200F_C000 - 0x200F_FFFF. This TCM memory is exclusive to LCPU and can be initialized by HCPU via address segment 0x2B0F_C000 - 0x2B0F_FFFF.

1.4.3.3 SRAM

There is a total of 224KB SRAM on LPSYS bus, which includes:

- 0x2010_0000-0x2010_7FFF, 32KB zero-wait-cycle SRAM, maximum frequency 48M
- 0x2010_8000-0x2013_7FFF, 192KB one-wait-cycle SRAM, maximum frequency 48M

All SRAMs can hold data in low-power mode.

1.4.3.4 Off-chip Flash

LPSYS supports external FLASH4 with address space 0x1200_0000-0x13FF_FFFF.

1.4.4 Address Mapping

Table 1-3: Address Mapping of LPSYS

Category	Memory/IP	Address Space	HCPU Address Space		LCPU Address Space	
			Starting Address	Ending Address	Starting Address	Ending Address
LPSYS_ITCM	ROM	384KB	0x0B00_0000	0x0B05_FFFF	0x0000_0000	0x0005_FFFF
	RAM	16KB	0x0B0F_C000	0x0B0F_FFFF	0x000F_C000	0x000F_FFFF
LPSYS_DTCM	RAM	16KB	0x2B0F_C000	0x2B0F_FFFF	0x200F_C000	0x200F_FFFF
XIP Memory	QSPI4 Memory	32MB	0x1200_0000	0x13FF_FFFF	0x1200_0000	0x13FF_FFFF
LPSYS_RAM (128KB) 0X2010_0000 0x2011_FFFF	LPSYS_RAM0	16KB	0x2010_0000	0x2010_3FFF	0x2010_0000	0x2010_3FFF
	LPSYS_RAM1	16KB	0x2010_4000	0x2010_7FFF	0x2010_4000	0x2010_7FFF
	LPSYS_RAM2	32KB	0x2010_8000	0x2010_FFFF	0x2010_8000	0x2010_FFFF
	LPSYS_RAM3	64KB	0x2011_0000	0x2011_FFFF	0x2011_0000	0x2011_FFFF
	LPSYS_RAM4	64KB	0x2012_0000	0x2012_FFFF	0x2012_0000	0x2012_FFFF
	LPSYS_RAM5	32KB	0x2013_0000	0x2013_7FFF	0x2013_0000	0x2013_7FFF

Continued on the next page

Table 1-3: Address Mapping of LPSYS (continued)

Category	Memory/IP	Address Space	HCPU Address Space		LCPU Address Space	
			Starting Address	Ending Address	Starting Address	Ending Address
LPSYS_APB1 (192KB) 0x4004_0000 0x4006_FFFF	RCC2	4KB	0x4004_0000	0x4004_0FFF	0x4004_0000	0x4004_0FFF
	DMAC2	4KB	0x4004_1000	0x4004_1FFF	0x4004_1000	0x4004_1FFF
	MAILBOX2	4KB	0x4004_2000	0x4004_2FFF	0x4004_2000	0x4004_2FFF
	PINMUX2	4KB	0x4004_3000	0x4004_3FFF	0x4004_3000	0x4004_3FFF
	PATCH	4KB	0x4004_4000	0x4004_4FFF	0x4004_4000	0x4004_4FFF
	UART3	4KB	0x4004_5000	0x4004_5FFF	0x4004_5000	0x4004_5FFF
	UART4	4KB	0x4004_6000	0x4004_6FFF	0x4004_6000	0x4004_6FFF
	UART5	4KB	0x4004_7000	0x4004_7FFF	0x4004_7000	0x4004_7FFF
	Reserved	4KB	0x4004_8000	0x4004_8FFF	0x4004_8000	0x4004_8FFF
	SPI3	4KB	0x4004_9000	0x4004_9FFF	0x4004_9000	0x4004_9FFF
	SPI4	4KB	0x4004_A000	0x4004_AFFF	0x4004_A000	0x4004_AFFF
	Reserved	4KB	0x4004_B000	0x4004_BFFF	0x4004_B000	0x4004_BFFF
	I2C4	4KB	0x4004_C000	0x4004_CFFF	0x4004_C000	0x4004_CFFF
	I2C5	4KB	0x4004_D000	0x4004_DFFF	0x4004_D000	0x4004_DFFF
	I2C6	4KB	0x4004_E000	0x4004_EFFF	0x4004_E000	0x4004_EFFF
	SYSCFG2	4KB	0x4004_F000	0x4004_FFFF	0x4004_F000	0x4004_FFFF
	GPTIM3	4KB	0x4005_0000	0x4005_0FFF	0x4005_0000	0x4005_0FFF
	GPTIM4	4KB	0x4005_1000	0x4005_1FFF	0x4005_1000	0x4005_1FFF
	GPTIM5	4KB	0x4005_2000	0x4005_2FFF	0x4005_2000	0x4005_2FFF
	BTIM3	4KB	0x4005_3000	0x4005_3FFF	0x4005_3000	0x4005_3FFF
	BTIM4	4KB	0x4005_4000	0x4005_4FFF	0x4005_4000	0x4005_4FFF
	WDT2	4KB	0x4005_5000	0x4005_5FFF	0x4005_5000	0x4005_5FFF
	GPADC	4KB	0x4005_6000	0x4005_6FFF	0x4005_6000	0x4005_6FFF
	SDADC	4KB	0x4005_7000	0x4005_7FFF	0x4005_7000	0x4005_7FFF
	Reserved	4KB	0x4005_8000	0x4005_8FFF	0x4005_8000	0x4005_8FFF
	LPCOMP	4KB	0x4005_9000	0x4005_9FFF	0x4005_9000	0x4005_9FFF
	TSEN	4KB	0x4005_A000	0x4005_AFFF	0x4005_A000	0x4005_AFFF
	PTC2	4KB	0x4005_B000	0x4005_BFFF	0x4005_B000	0x4005_BFFF
	LCDC2	4KB	0x4005_C000	0x4005_CFFF	0x4005_C000	0x4005_CFFF
	BUSMON2	4KB	0x4005_D000	0x4005_DFFF	0x4005_D000	0x4005_DFFF
	Reserved	4KB	0x4005_E000	0x4005_EFFF	0x4005_E000	0x4005_EFFF
	Reserved	4KB	0x4005_F000	0x4005_FFFF	0x4005_F000	0x4005_FFFF
	Reserved	64KB	0x4006_0000	0x4006_FFFF	0x4006_0000	0x4006_FFFF
LPSYS_APB2 (64KB) 0x4007_0000 0x4007_FFFF	LPSYS_AON	4KB	0x4007_0000	0x4007_0FFF	0x4007_0000	0x4007_0FFF
	LPTIM2	4KB	0x4007_1000	0x4007_1FFF	0x4007_1000	0x4007_1FFF
	LPTIM3	4KB	0x4007_2000	0x4007_2FFF	0x4007_2000	0x4007_2FFF
	Reserved	4KB	0x4007_3000	0x4007_3FFF	0x4007_3000	0x4007_3FFF
	Reserved	24KB	0x4007_4000	0x4007_9FFF	0x4007_4000	0x4007_9FFF
	PMUC	4KB	0x4007_A000	0x4007_AFFF	0x4007_A000	0x4007_AFFF
	RTC	4KB	0x4007_B000	0x4007_BFFF	0x4007_B000	0x4007_BFFF
	IWDT	4KB	0x4007_C000	0x4007_CFFF	0x4007_C000	0x4007_CFFF
	Reserved	12KB	0x4007_D000	0x4007_FFFF	0x4007_D000	0x4007_FFFF

Continued on the next page

Table 1-3: Address Mapping of LPSYS (continued)

Category	Memory/IP	Address Space	HCPU Address Space		LCPU Address Space	
			Starting Address	Ending Address	Starting Address	Ending Address
LPSYS_AHB (256KB) 0x5004_0000 0x5007_FFFF	GPIO2	4KB	0x5004_0000	0x5004_0FFF	0x5004_0000	0x5004_0FFF
	QSPI4	4KB	0x5004_1000	0x5004_1FFF	0x5004_1000	0x5004_1FFF
	RFC	8KB	0x5004_2000	0x5004_3FFF	0x5004_2000	0x5004_3FFF
	PHY	4KB	0x5004_4000	0x5004_4FFF	0x5004_4000	0x5004_4FFF
	Reserved	44KB	0x5004_5000	0x5004_FFFF	0x5004_5000	0x5004_FFFF
	MAC	64KB	0x5005_0000	0x5005_FFFF	0x5005_0000	0x5005_FFFF
	Reserved	128KB	0x5006_0000	0x5007_FFFF	0x5006_0000	0x5007_FFFF
PHY_DUMP	PHY_DUMP	64KB	0x5008_0000	0x5008_FFFF	0x5008_0000	0x5008_FFFF

1.4.5 Interrupt List

Table 1-4: Interrupt List of LCPU

IRQ #	IRQ Source
LCPU_NMI	WDT2
LCPU_IRQ[0]	AON2
LCPU_IRQ[1]	BT_MAC
LCPU_IRQ[2]	DMAC2_CH1
LCPU_IRQ[3]	DMAC2_CH2
LCPU_IRQ[4]	DMAC2_CH3
LCPU_IRQ[5]	DMAC2_CH4
LCPU_IRQ[6]	DMAC2_CH5
LCPU_IRQ[7]	DMAC2_CH6
LCPU_IRQ[8]	DMAC2_CH7
LCPU_IRQ[9]	DMAC2_CH8
LCPU_IRQ[10]	PATCH
LCPU_IRQ[11]	Reserved
LCPU_IRQ[12]	UART3
LCPU_IRQ[13]	UART4
LCPU_IRQ[14]	UART5
LCPU_IRQ[15]	Reserved
LCPU_IRQ[16]	SPI3
LCPU_IRQ[17]	SPI4
LCPU_IRQ[18]	Reserved
LCPU_IRQ[19]	I2C4
LCPU_IRQ[20]	I2C5
LCPU_IRQ[21]	I2C6
LCPU_IRQ[22]	GPTIM3
LCPU_IRQ[23]	GPTIM4
LCPU_IRQ[24]	GPTIM5
LCPU_IRQ[25]	BTIM3
LCPU_IRQ[26]	BTIM4
LCPU_IRQ[27]	Reserved
LCPU_IRQ[28]	GPADC
LCPU_IRQ[29]	SDADC
LCPU_IRQ[30]	Reserved
LCPU_IRQ[31]	Reserved
LCPU_IRQ[32]	TSEN
LCPU_IRQ[33]	PTC2

Continued on the next page

Table 1-4: Interrupt List of LCPU (continued)

IRQ #	IRQ Source
LCPU_IRQ[34]	LCDC2
LCPU_IRQ[35]	GPIO2
LCPU_IRQ[36]	QSPI4
LCPU_IRQ[37]	Reserved
LCPU_IRQ[38]	Reserved
LCPU_IRQ[39]	Reserved
LCPU_IRQ[40]	Reserved
LCPU_IRQ[41]	LPCOMP
LCPU_IRQ[42]	LPTIM2
LCPU_IRQ[43]	LPTIM3
LCPU_IRQ[44]	Reserved
LCPU_IRQ[45]	Reserved
LCPU_IRQ[46]	HCPU2LCPU
LCPU_IRQ[47]	RTC

1.5 Power Management

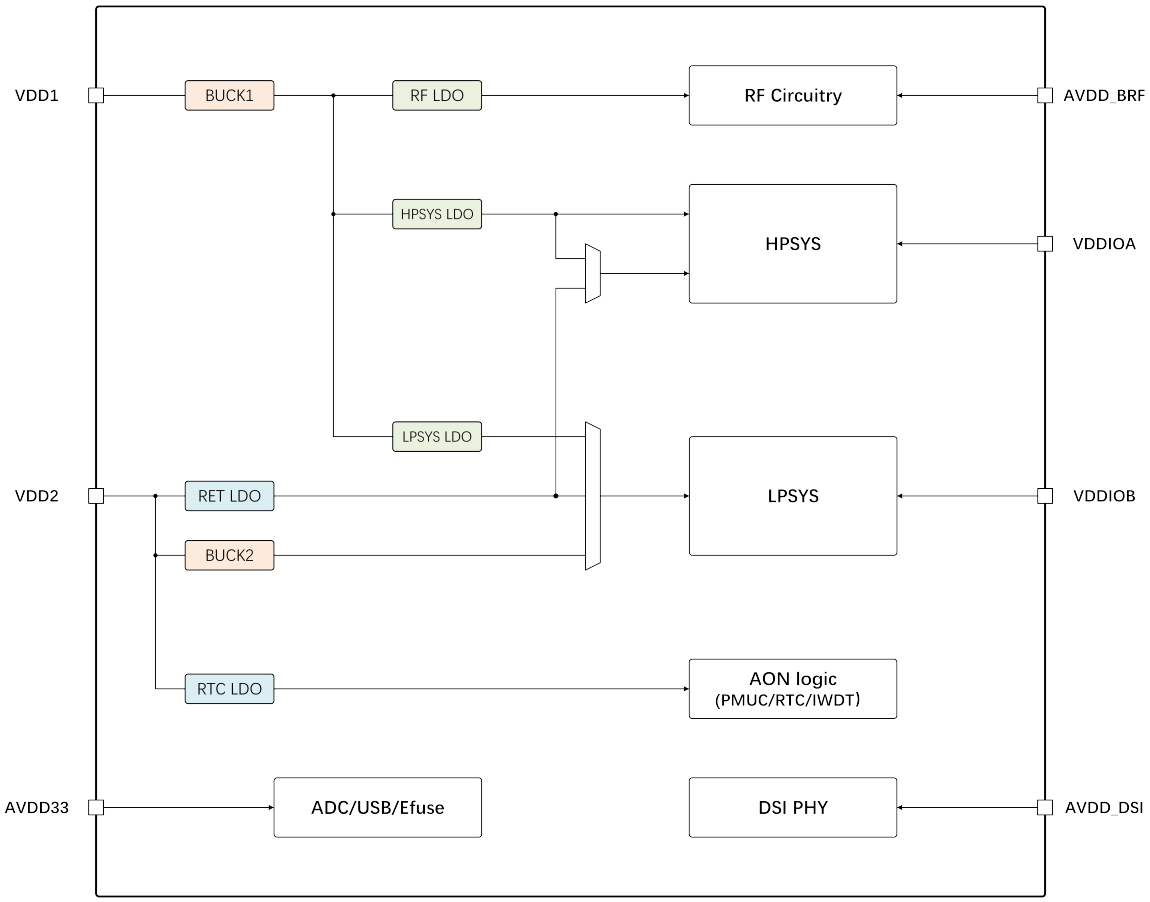


Figure 1-5: Architecture of Power Management

2 High-Performance Dedicated Computing

2.1 ePicasso™ High-Performance 2.5D GPU

In 2.5D image processing, many common image operations will consume a lot of CPU computing resources. ePicasso™ is an acceleration GPU designed specifically for 2.5D image operations. It can provide exponential speed improvements for common 2.5D image operations such as layer overlay, scaling, and rotation. In addition, ePicasso™ is compatible with various common RGB image formats, simplifying the conversion of different image formats in the system.

2.1.1 Layer Overlay

ePicasso™ supports up to four foreground layers and one monochrome background layer. The input and output formats include commonly used RGB565, RGB888, ARGB8565 and ARGB8888. Each foreground layer has a separate overlay mode and overlay area. In addition, each layer also has a separate filter configuration option, which can make the layer filter out a specific color. This function can be used for simple image capture.

2.1.2 Graphics Scaling

ePicasso™ has a layer called functional layer, which, in addition to supporting overlays, enables the scaling of graphics up to eight times, with an accuracy of 1/256. The scaling can be configured separately in the X and Y directions to suit different requirements.

2.1.3 Graphics Rotation

In addition to scaling, the functional layer of ePicasso™ can support high-precision rotation of images. Users can customize the sin/cos values of the rotation angle to meet the rotation requirements of any angle. Rotation and scaling can be enabled at the same time to complete two operations of the image at one time, which improves the performance of image processing.

2.2 LCD Controller

The LCD controller is mainly used to output data from the Framebuffer to the external display, and the existing LCD controller can support common screen interfaces, including DBI, DPI and DSI. In addition, the LCD controller also supports images of compressed format, which can significantly reduce the memory usage bandwidth and improve system performance.

2.2.1 TurboPixel™ Frame Buffer Compression

To improve the frame rate of the image and the smoothness of the display, multiple (two or three) frame buffers are frequently used. Typically, in order to parallelize image output and image processing, dedicated frame buffers are required to output image data to the screen. To reduce the memory space and reading bandwidth of these frame

buffers, the MCU system provides a TurboPixel™ image frame compression module based on proprietary algorithm. When reading the image data, the decompression module in the LCD controller can directly read the compressed data and output the decompressed data to the screen. In this way, the memory space of the frame buffer and the bandwidth resources consumed by reading can be saved.

2.2.2 Display Interface

The LCD controller is mainly used for the adaptation between the data for display and the mainstream display interfaces, and the following display interfaces are supported by this chip.

2.2.2.1 MIPI-DBI

The LCD controller can support serial SPI mode and parallel 8080 mode in the DBI interface. For SPI mode, the LCD controller can support both 3-wire and 4-wire modes, as well as dual/quad data line operations. It supports 8-bit RGB332, 16-bit RGB565 and 24-bit RGB888 in color format. For the 8080 mode, the LCD controller supports bus widths of 8-bit, 16-bit and 24-bit, and also supports color formats of RGB332, RGB444, RGB565, RGB666 and RGB888.

2.2.2.2 MIPI-DPI

To support screens without built-in cache, the LCD controller has also added support for the DPI interface, which has a 24-bit data width and supports color formats of RGB565 and RGB888. In addition, the LCD controller provides flexible VBP, VFP, HBP and HFP controls to meet the needs of different screen types.

2.2.2.3 MIPI-DSI

As a serial high-speed bus, DSI is mainly for high-resolution and highly integrated screen usage scenarios, such as wearable devices. The LCD controller has also added support for the DSI interface. In high-speed mode, it can support up to 2 bi-directional data lines, with a maximum transfer rate of 480Mbps per line. In low-speed mode, the LCD controller can also support 1 bi-directional data line. This configuration can meet the requirements of most wearable devices.

2.2.2.4 JDI Reflective Display

To meet the low-power requirements of wearable products, JDI has developed an ultra-low-power reflective display that uses the sun's rays to present images. Compared with the traditional LCD screen, the power consumption can be reduced by more than 95%. It can be used in wearable products to achieve long battery life. The LCD controller also added support for JDI reflective display interface, including serial interface and parallel interface. The two interfaces can support up to 64-color display, and support partial refresh and full-screen refresh, thereby further reducing the power consumption of screen refresh and meeting the needs of long battery life.

2.3 eZip™ Lossless Compression Decoder

The eZip™ decoder is a real-time lossless decompression module based on proprietary algorithm, with a compression rate equivalent to that of the Zip format. It can be used to decode the general data before saving it, which will improve the real-time loading capability of the data. If the data is transferred from outside the chip, the transfer after compression will help shorten the transfer time and reduce the power consumption.

In addition, eZip™ also supports image compression of proprietary formats, with a compression rate equivalent to that of the PNG format, and supports independent DMA operations or reading linked with ePicasso™. When operating independently, eZip™ can flexibly decompress and transport the compressed pictures stored in Flash or RAM to the target cache through the DMA mechanism. In the linkage mode, ePicasso™ reads pictures from the memory in real time and decompresses them in real time through the eZip™ module, and then performs the required 2.5D calculations according to the general graphics process, thereby saving the cache for temporary storage of decompressed pictures.

Through the above mechanism, eZip™ can effectively reduce the demand for storage capacity of image materials, maximize the richness of materials in limited storage, and reduce the bandwidth requirements for off-chip storage, thereby greatly improving the overall operating efficiency of the system.

The eZip™ module is a module for decoding the eZip™ compressed images and outputting them. The module reads compressed data through the AHB bus, and the decoded image data can be configured to be output through the AHB bus or directly sent to the epic module for subsequent processing.

The module has the following characteristics:

- The data address input/output via the AHB bus can be configured
- Output image data can be sent directly to the epic module
- Can output image data for a specified area
- Support decoding parameter cache function, which can shorten decoding time in case of cache hit

2.4 Neural Network Accelerator

2.4.1 Neural Network Matrix Convolution Accelerator (NNACC)

The matrix convolution accelerator is designed to meet the needs for the underlying matrix computing power in machine learning, and can be widely applied to various neural network frameworks. The accelerator has rich memory and access interfaces and provides flexible data address configuration. It supports a maximum input matrix of 255×255 and a maximum number of input and output channels of 128. It supports 8bit integer operations, which can meet most of the edge-end AI computing requirements, such as voice command recognition, heart rate, pedometer, electrocardiogram and other sensor calculations.

2.4.2 Neural Network Co-Processor (NN Co-Processor)

The neural network coprocessor is connected to the hpcpu/lpcpu through the coprocessor interface. The software calls the processor through special coprocessor instructions.

The coprocessor has the following characteristics:

- Data bus width of 64Bit
- Support MAC operations with 8Bit width
- Support 4 independent MAC operations for a single instruction

3 Peripherals

3.1 Bluetooth Low Energy 5.2

3.1.1 RF and Baseband

BLE RF and baseband include the transmitter and the receiver. The transmitter modulates the baseband signal to the 2.4G BLE frequency band and transmits it, and the receiver receives the over-the-air 2.4G BLE frequency band signal and demodulates it to the baseband signal.

The main features are:

- Support Bluetooth 5.2 protocol: 1M PHY (1Mbps), 2M PHY (2Mbps), Coded PHY (125Kbps, 500Kbps)
- Integrated AGC
- Support RSSI
- The receiver supports automatic frequency offset correction
- Adjustable transmit power, 10dBm max
- Integrated Balun and antenna matching network, no off-chip matching required

3.1.2 Controller

The BLE controller supports BLE 5.2 protocol and is mainly used for package encoding and decoding as well as event scheduling.

The main features are:

- Support all package formats (broadcast package/extended broadcast package/data package, etc.)
- Support data encryption and decryption
- Support data stream processing (CRC and whitening)
- Support two FM modes
- Support low-power mode

3.2 Analog Peripherals

3.2.1 10Bit Analog/Digital Converter

GPADC contains a SARADC, and the basic function is to convert the external input voltages into digital signals.

The main features of GPADC are:

- 10-bit resolution
- Maximum sampling rate 3MS/s
- Single-ended input voltage: 0 ~ 1.1V
- Differential input voltage: -0.7V ~ 0.7V

- Support 8 single-ended analog inputs or 4 pairs of differential analog inputs
- Support single measurement mode and cyclic measurement mode
- Each measurement can be divided into 8 time slots, and each time slot can be individually configured with analog input channels
- Support software (write register) and hardware (e.g. timer) triggering
- Support DMA channels
- Sampling frequency can be configured

Table 3-1: 10-bit GPADC Specifications

	Min.	Typ.	Max.	Unit	Comments
Resolution		10		bit	
T_{sample} (Differential)	166.67n		666.67n	s	fs=1/(T_{sample}+$T_{conversion}$)
T_{sample} (Single-Ended)	583.33n		666.67n	s	
$T_{conversion}$	166.67n		666.67n	s	
Sample rate (fs)			3	Msps	
ENOB (Differential)		8.5		bit	V_{in}=-1dBFs, no averaging
ENOB (Single-Ended)		7.6		bit	V_{in}=-3dBFs, no averaging
SNDR (Differential)		52.93		dB	V_{in}=-1dBFs, no averaging
SNDR (Single-Ended)		47.51		dB	V_{in}=-3dBFs, no averaging
Current Consumption		87.04		uA	fs=3Msps
		60.59		uA	fs=750ksps

The relationship between GPADC source resistance R_{AIN} and the sampling time is as follows:

Resolution (bit)	T_{sample} (ns)	Maximum source resistance R_{AIN} (kOhm)
10	125	1
	166.67	5
	291.67	10
	458.33	20
	666.67	30

3.2.2 16Bit Analog/Digital Converter

The SDADC is mainly used for the measurement of signals, and supports continuous sampling as well as single sampling. The reference voltage is 0~2V, and the gain is 0.25 to 4 times. The measurement range that can be achieved by single-ended is 0V~(0.65×reference voltage/gain), the measurement range that can be achieved by differential is -(0.65×reference voltage/gain)~(0.65×reference voltage/gain), but the measurement range can't exceed 0~AVDD, with a minimum measurement error of ±60uV, and a sampling rate of 4kHz for single sampling and 8kHz for continuous sampling.

Main functions:

- Support 16bit data accuracy
- Support up to 2 differential or 5 single-ended channel sampling
- Support multiple sampling of multiple channels which can be configured by the software

3.2.3 Temperature Sensor

The temperature sensor converts the temperature into a voltage that changes with the temperature, and then converts the voltage into a number through the ADC. The system calls the temperature sensor through the software.

The main features are as follows:

- Temperature sensor resolution 0.2°C
- Support temperature range from -40°C to 125°C
- Temperature sensor accuracy -3°C to 3°C
- Support polling or interrupt mode reading

3.2.4 Voltage Comparator

The LPCOMP (Low-Power Comparator) contains two independent voltage comparators which can compare the voltage of an external input analog signal to the reference voltage value to produce the comparison result. The two comparators can measure different signals separately or measure the same signal and produce a combined output. The reference voltage value can be input from an external source or generated internally by the chip. The comparator results can be read via IO output or via registers, and can also generate interrupt/ PTC event triggers or wake-up signals.

The LPCOMP is also capable of real-time monitoring when the system enters certain low-power modes, and waking the system up when a specific comparison result is detected.

Main features of LPCOMP:

- Two comparators, which can be used independently or in combination for window comparison
- Reference voltage selection
  - Internally generated 4 levels of reference voltage
  - External input
- Configurable hysteresis comparison
- Configurable power/speed gear
- Polarity reversal of the comparison results
- Post-processing of the comparison results
  - High/Low level
  - Rising edge/falling edge/any edge
- Multiple outputs
  - IO
  - Register
  - Interrupt
  - PTC trigger
  - LPTIM clock
  - Low-power sleep wakeup
- The system can also work under low-power mode (light sleep/deep sleep) and can be woken up

3.3 DMA

3.3.1 ExtDMA

The ExtDMA (Extended Direct Memory Access) enables efficient data transfer between two different address ranges on the bus, and integrates the TurboPixel™image frame compression module for image compression while transferring. ExtDMA can also be used as a general-purpose DMA when compression is not enabled. Compared to DMAC, ExtDMA is more efficient in accessing external memory (e.g. FLASH, PSRAM), but it has only one channel, supports only 4-byte aligned handling, and does not respond to peripheral requests.

Main features of ExtDMA:

- Single AHB master controller,access SRAM PSRAM FLASH,etc.,support burst transmission
- Single transmission channel, built-in FIFO with a depth of 16 and a bit width of 32 bits
- Both the source address and the destination address are accessed in 4 bytes, and support automatic address increment
- The maximum number of transmission units in a single configuration is 2^20-1, with a fixed 4-byte transmission per unit, i.e., a maximum of 4M bytes in a single transmission
- Each channel supports transmission completion, half transmission, and transmission error event flags, and can generate interrupt requests independently
- Integrated TurboPixel™image frame compression function, support RGB565/ RGB888/ ARGB8888 format input, supports up to 512 pixels in a single line.

3.3.2 DMAC

The DMAC (Direct Memory Access Controller) is used to carry out data transfer between two different address ranges on the bus. DMAC has a total of 8 independent channels. Each channel can be configured with a source address range and a target address range, which are respectively mapped to the address range of each memory or peripheral, so as to achieve high-efficiency transmission between memory-memory, memory-peripheral, peripheral-memory, and peripheral-peripheral, which can effectively alleviate the workload of the CPU.

The DMAC supports peripheral response mode and memory handling mode: In the peripheral response mode, the DMAC performs handling based on the DMA request of the peripheral, thereby adapting the bandwidth of the peripheral; In the memory handling mode, the DMAC does not wait for the DMA request of the peripheral, and will complete data transfer as soon as possible. When multiple channels are enabled at the same time, the DMAC will transport in order of priority from high to low; and in the process of transporting lower priority channels, the higher priority channels can carry out the preemption handling. Each channel can generate an interrupt or PTC trigger when the transmission is halfway or complete.

DMAC1 and DMAC2 is located in HPSYS and can respond to DMA requests from HPSYS peripherals. DMAC3 is located in LPSYS and can respond to DMA requests from LPSYS peripherals.

Main features of DMAC:

- Single AHB master controller,access SRAM PSRAM FLASH,AHB,APB,etc.
- 8 independent configurable channels
- The DMA request for each channel can be selected from up to 64 peripheral DMA requests, or can be requested by software
- Each channel supports 4 levels of priority configuration, when the priority is the same, it is judged according to the channel number

- Support peripheral-memory, memory-peripheral, memory-memory, peripheral-peripheral transfer
- Support single-byte/ double-byte/ 4-byte access to both source and destination addresses independently.The addresses of the source and target must be aligned according to the size of the transmission data unit, and support automatic address increment.During the transmission process, the address does not support crossing the 1MB boundary
- The number of single transmission units can be configured from 0 to 65536.
- Support cyclic buffering mode, which will automatically restart after a single transfer is completed
- Each channel supports 3 types of event flags,i.e. transmission completed, half-transmission, transmission error, and can independently generate interrupts or PTC triggers
- Each channel supports block transfer mode with configurable block size

3.4 I/O Peripherals

3.4.1 General Purpose Input/ Output (GPIO)

The system has a total of 128 GPIO pins, of which 80 are HPSYS and 48 are LPSYS. Different functions can be assigned to these pins by configuring the corresponding registers.

When configured as an output function, the output value can be configured through the register.

When configured as an input function, the input value can be queried through the corresponding register, and support the input signal interrupt trigger at the same time. The interrupt trigger mode can be set to level trigger and edge trigger, which includes upper and lower dual-edge trigger.

3.4.2 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous Receiver/Transmitter (UART) supports full-duplex mode and offers baud rates up to 6Mbps and a variety of configurable data formats, providing a flexible and efficient means of data interaction for communication with external standardized devices. It also supports DMA for multi-packet transceiving.

UART1 and UART2 are located in HPSYS。UART3、UART4 and UART5 are located in LPSYS。

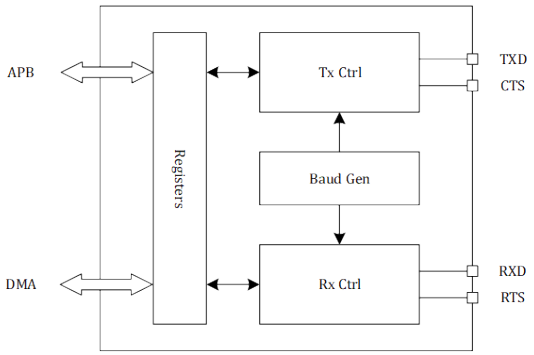


Figure 3-1: UART

Main features of UART:

- Full-duplex asynchronous communication

- Configurable 16 times oversampling or 8 times oversampling, select frequency priority or clock tolerance priority
- Flexible baud rate configuration, when the input clock is 48MHz and the oversampling rate is 16, the baud rate is 3Mbps
- Configurable packet length (7/8/9 bits)
- Configurable stop bit (1/2 bits)
- Hardware flow control (CTS/RTS)
- DMA multi-packet sending and receiving
- Receiving parity check and sending parity generation
- Receiving and sending interrupts, and other error interrupts

Baud rate calculation instructions

Assuming that the input clock is fixed at 48MHz, the baud rate calculation formula is as follows:

$$Baud\ Rate = \frac{48MHz}{(BRR_{INT} + \frac{BRR_{FRAC}}{16})(16\ or\ 8)} \tag{3.1}$$

3.4.3 I2C

The I2C (Inter-Integrated Circuit) interface supports both the roles of master and slave. It can be used as a master to communicate with I2C slave peripherals, or as a slave to respond to an external I2C master. I2C has a built-in 8-byte FIFO, which can perform single read and write, or batch data read and write through DMA. I2C supports standard mode, fast mode, fast mode plus, and high-speed mode, with a maximum speed of 3.4Mbps.

Main features of I2C:

- Can be used as master and slave at the same time
- Support bus multi-master
- Support standard mode (up to 100kbps)
- Support fast mode (up to 400kbps)
- Support fast mode + (up to 1Mbps)
- Support high-speed mode (up to 3.4Mbps)
- As a master, it supports access to 7-bit or 10-bit addressing
- As a slave, it supports access to 7-bit addressing
- Configurable bus timing
- Support clock stretching
- 8-byte FIFO, support DMA
- Configurable digital anti-jitter circuit

3.4.4 PDM

The PDM (Pulse Density Modulation) interface is mainly used to convert the PDM audio signal captured by the PDM microphone into PCM (Pulse Code Modulation) signal for subsequent audio processing.

Main functions:

- Support left and right stereo signals at the same time, and can also collect mono signals separately
- Available PDM microphone clock rates: 3.072MHz, 1.536MHz, 0.768MHz, 1.024MHz, 2.4MHz, 1.6MHz, 0.8MHz.

- Support PCM data rates: 48kHz, 32kHz, 24kHz, 16kHz, 12kHz, 8kHz
- Support 24bit and 16bit PCM signals
- Support resolution of 0.5dB and adjustable from -15dB to 45dB gain

3.4.5 I2S

The I2S interface is used for audio input and output, and can be used to connect external audio chips, digital microphones and other devices. Compared with the analog audio interface, the I2S digital audio interface has a better anti-interference ability and a more streamlined interface protocol.

Main features of I2S:

- Support master mode only
- Support full duplex mode
- Configurable I2S data format, including left-justified, right-justified and standard format
- Support multiple audio data formats, including 8-bit and 16-bit mono and stereo formats
- Configurable I2S PCM signal bit width, up to 24-bit

3.4.6 Serial Peripheral Interface (SPI)

The SPI supports 3 communication formats: SSP/ SPI/ Microwire. SSP/ SPI is a full-duplex communication protocol, and the controller can be configured in Master or Slave mode. Microwire is a half-duplex communication protocol, and the controller can only be configured in Master mode. The SPI controller has a built-in transmit/receive FIFO. The transmit FIFO and the receive FIFO share the same address. The receive FIFO is accessed when the address is read, and the transmit FIFO is accessed when the address is written. SPI1/ SPI2 are located in HPSYS, and SPI3/ SPI4 are located in LPSYS.

The features of SPI are as follows:

- Support 8 to 32Bit data width
- In SPI format, the clock polarity and phase can be set by register SPO and SPH
- Chip select signal polarity can be configured
- FIFO depth can be set to 32Bits×16Entry or 4Bits/ 8Bits×32Entry
- Both receive and transmit support DMA mode
- The maximum clock frequency of SPI in HPSYS is 48MHz; the maximum clock frequency of SPI in LPSYS is 24MHz

The working sequences of various communication formats are as follows:

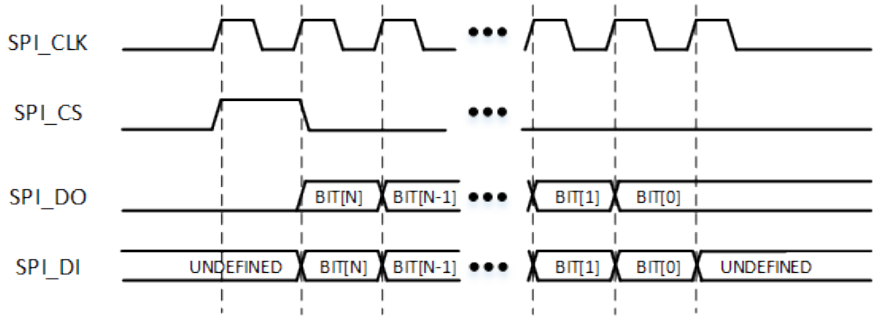


Figure 3-2: Single Transmit and Receive Sequence of SSP Format

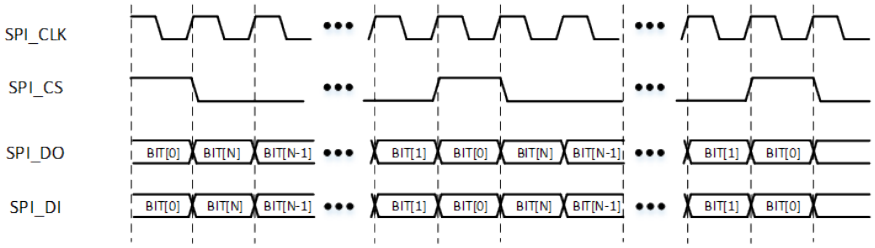


Figure 3-3: Continuous Transmit and Receive Sequence of SSP Format

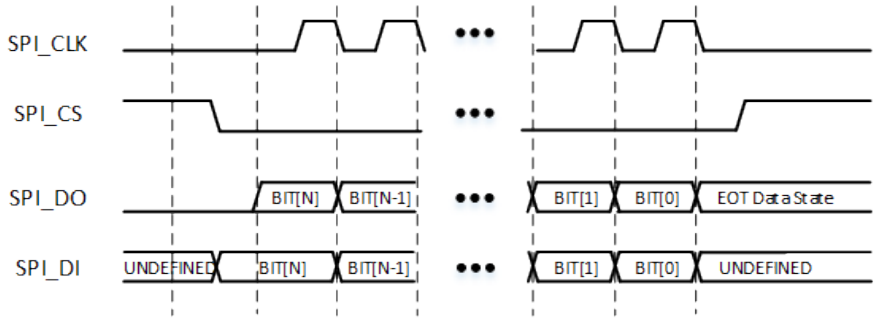


Figure 3-4: Single Transmit and Receive Sequence of SPI Format

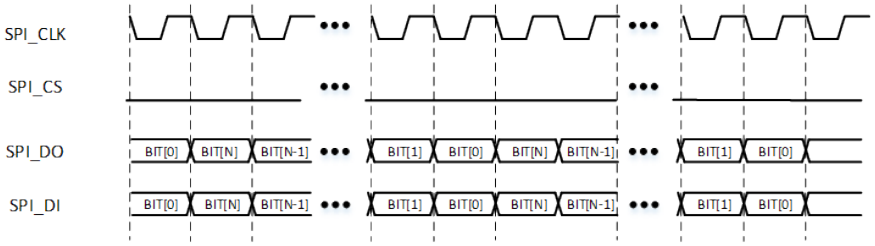


Figure 3-5: Continuous Transmit and Receive Sequence of SPI Format

The following figures illustrate the effect of SPH/SPO settings in SPI format:

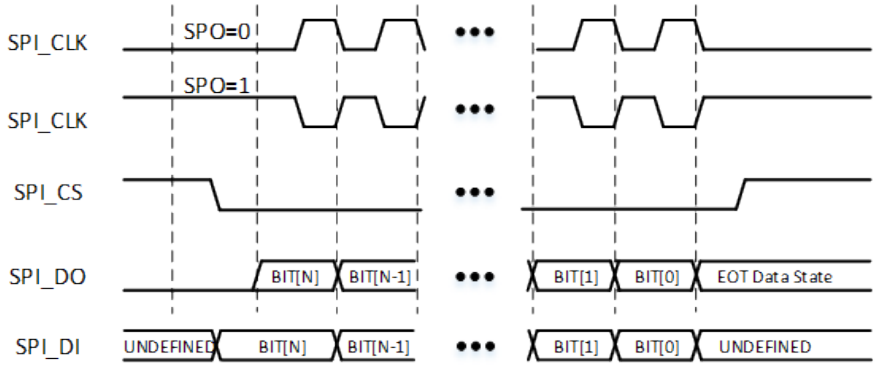


Figure 3-6: SPI Sequence at SPH=0

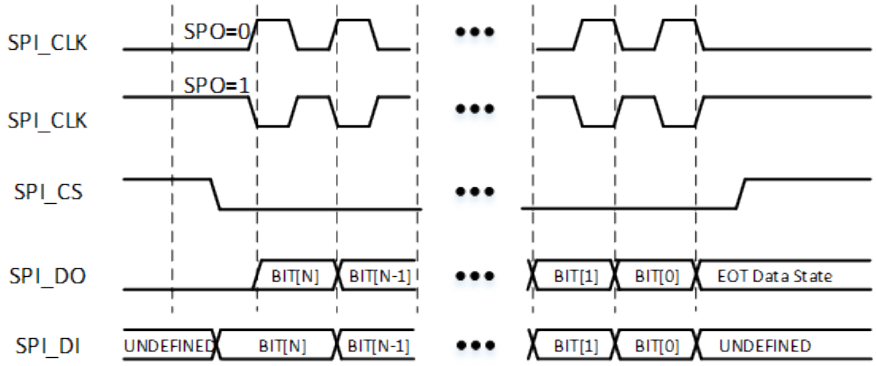


Figure 3-7: SPI Sequence at SPH=1

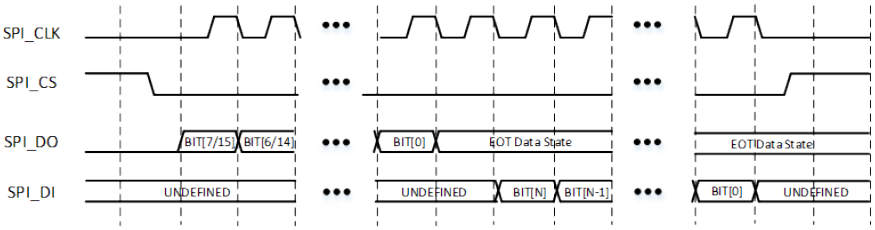


Figure 3-8: Single Transmit and Receive Sequence of Microwire Format

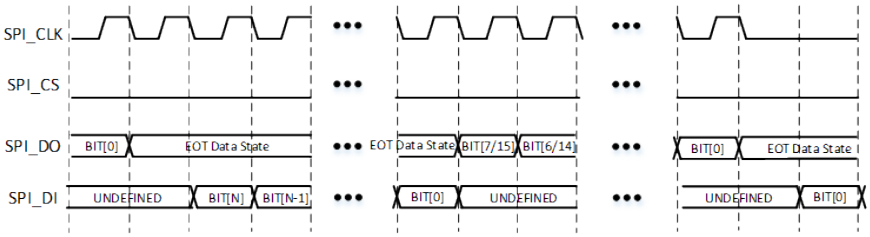


Figure 3-9: Multiple Transmit and Receive Sequence of Microwire Format

3.4.7 Peripheral Task Controller (PTC)

The PTC (Peripheral Task Controller) is a stand-alone peripheral controller, which can automatically complete the mutual scheduling and control tasks of each peripheral without waking up the CPU. Based on the event triggering of the selected peripherals, the PTC can automatically rewrite the working mode or working state of each peripheral, and can chain these tasks together to form an automatically triggered task sequence, thus completing a complex and fast response task chain. In the process of the task chain, the CPU can stay asleep all the time, thereby effectively saving power.

The PTC has a total of 8 channels, independent trigger source can be selected for each channel and independent task can be can be configured. The tasks that can be performed include two types: write the specified data directly to the specified address; read out the contents of the specified address, perform XOR/ and/ or/ addition with the specified data and then write it back. When the task of each channel is completed, a trigger signal can be generated to trigger the tasks of other channels.

PTC1 is located in HPSYS and can control the peripherals on the HPSYS bus. PTC2 is located in LPSYS and can control the peripherals on the LPSYS bus.

Main features of PTC:

- 8 independently configured channels can work at the same time
- Each channel trigger can be selected from 128 trigger sources, including PTC's own trigger sources
- Access to AHB and APB peripheral address space, word-aligned access only
- Support directly writing data, or rewriting after reading
- Support 32-bit XOR/ and/ or/ addition operations
- Fixed priority arbitration, the smaller the channel number, the higher the priority
- The register space of 4 words is used for data cache

3.4.8 USB2.0 FS

This chip integrates a full-speed (FS) USB 2.0 Device interface with the following functions.

- Software configurable endpoint settings, support suspend/ resume
- Support dynamic FIFO size
- Support session request protocol and host negotiation protocol
- Support full speed and slow speed modes
- On-chip integrated USB2.0 FS PHY

3.5 Timers

3.5.1 General-Purpose Timer

The GPTIM (General-Purpose Timer) is based on a 16-bit counter, and can realize functions such as timing, measuring the pulse length of the input signal (input capture) or generating output waveforms (output comparison and PWM). The counter itself can count up, down or up/down. The counting clock can be the system PCLK, IO input signal or cascaded input signal, and can be prescaled from 1 to 65536 times. The GPTIM has 4 channels in total, which can be independently configured as input capture or output mode. The results of counting, input capture and output comparison can generate interrupts, DMA requests or PTC events. The GPTIM has a Master-Slave Mode interface, which can be multi-level cascaded to realize functions such as multi-level counting or synchronous triggering.

Main features of GPTIM:

- 16-bit increment, decrement, increment/ decrement auto-reload counter, the maximum count is 65535
- 16-bit programmable (can be modified in real time) prescaler, the clock division is any value between 1~65536
- 8-bit configurable repeat count
- Support One Pulse Mode (OPM), the counter will stop automatically when the repeated counting is completed
- 4 independent channels, which can be configured as input or output modes respectively
- Input mode
  - Rising edge/ falling edge capture
  - PWM pulse width and period capture (requires two channels)
  - Optional one of 4 input ports or 1 external trigger port, supporting anti-jitter filtering and pre-frequency reduction
- Output mode
  - Forced output high/ low level
  - Output high/ low/ toggle level when counting to the comparison value
  - PWM output, pulse width and period can be configured

  - Multi-channel PWM combined output to generate multiple PWMs with interrelationships
  - Single pulse/ retrigger single pulse mode output
- Master-Slave Mode
  - Support multi-counter interconnection, which can be used as a slave device to be controlled by external input or other master devices while generating control signals as a master device
  - Control modes include reset, trigger, gate control, etc.
  - Support synchronous start and reset of multiple counters
- Encoding mode input, control the incremental/ decremental counting of the counter
- An interrupt/ DMA request/ PTC trigger is generated when the following events occur:
  - Update: Counter increment overflow /decrement overflow, counter initialization (by software or internal/external trigger)
  - Trigger event (counter start, stop, initialization or counting triggered internally/ externally)
  - Input capture
  - Output comparison

3.5.2 Basic Timer

The BTIM (Basic Timer) is based on a 32-bit incremental counter and can realize the timing function. The counter clock can be the system PCLK or cascaded input signal, and can be prescaled from 1 to 65536 times. The timing results can generate interrupts, DMA requests, or PTC events. The BTIM has a Master-Slave Mode interface, which can be multi-level cascaded to realize functions such as multi-level counting or synchronous triggering.

Main features of BTIM:

- 32-bit incremental auto-reload counter
- 16-bit programmable prescaler, the clock division is any value between 1~65536
- Support One Pulse Mode (OPM), the counter will stop automatically when the counting is completed
- Master-Slave Mode
  - Support interconnection with BTIM and GPTIM, which can be used as a slave device to be controlled by external input or other master devices while generating control signals as a master device
  - Control modes include reset, trigger, gate control, etc.
  - Support multiple timers to start and reset simultaneously
- Interrupt, DMA request and PTC trigger will be generated in case of counter overflow or initialization

3.5.3 Low-Power Timer

The LPTIM (Low-Power Timer) is based on a 24-bit incremental counter, and can realize functions such as timing, generating output waveform (output comparison and PWM), and waking up the system. The counter clock can be the system clk, low-power clock, IO input signal or comparator output, and can be prescaled up to 128 times and cycle counting up to 256 times. Depending on the counting results, the PWM output as well as the interrupt can be generated,or the wake-up signal can be generated to wake up the system from the low-power mode. When the IO input signal is used as the count clock, it supports counting independent of the internal clock and generates the wake-up signal, allowing the system to turn off the internal clock.

Main features of LPTIM:

- 24-bit upward automatic reload counter, the maximum count is 16777215 (2^24-1)

- Counting clock selection
  - Internal clock, PCLK2 or low-power clock
  - IO input signal or comparator output with selectable edges, can use the internal clock for anti-jitter, and can also count independently without relying on the internal clock
- 8-level prescaling, clock division is 0 to the 7th power of 2
- 1~256 cycles
- Counting mode
  - Continuous counting mode
  - One Pulse Mode, counting ends after the number of cycles is completed
- Configurable polarity output mode
  - PWM output, can be configured with pulse width and period
  - Single toggle output
  - Single pulse or specified number of pulse output
- Trigger mode
  - Software trigger
  - IO input signal edge trigger, support anti-jitter filtering
- Timeout detection, the counter will be reset on each external trigger
- The interrupt or wake-up signal will be generated when the following events occur:
  - Update
  - Counter overflow
  - Output comparison
  - External trigger

3.5.4 Watchdog

The watchdog timer, as a counter, is mainly used to reset the system after the set time is reached to prevent the software from hanging up.

Basic functions of watchdog timer:

- Support two working modes:
  - Mode0
    - wdt will not generate interruption, and will reset the system directly after the set time is reached
    - Support up to 24-bit counter
  - Mode1
    - Divided into two periods. After reaching the set time of the first period, the interrupt will be generated. After reaching the set time of the second period, the system will be reset
    - Support up to 24-bit counter for each period
- Support write protection to prevent software from misoperation of wdt

3.6 Encryption

3.6.1 AES

The AES accelerator is an arithmetic accelerator for symmetric encryption algorithms. Users can configure the encryption and decryption algorithm keys and initial vectors to perform encryption and decryption operations on the data in the memory, and store the results in the designated memory area.

Compared with software encryption and decryption, the AES accelerator has higher computing speed, more flexible configuration, and better access efficiency to peripheral storage devices. In addition, in bypass mode, the AES accelerator can also be used as a DMA for data transmission.

Features of AES:

- Support AES-128, AES-192, AES-256 and State Secrets SM4 algorithm standard
- Support ECB, CTR and CBC modes
- RootKey can be called to perform encryption and decryption operations, while ensuring that RootKey cannot be read by external programs

3.6.2 CRC

The CRC (Cyclic Redundancy Check) can perform CRC calculations with a specific bit width, any generated polynomial, and any initial value. Data can be input via CPU or DMA with a minimum input unit of a single byte and no maximum byte limit. A single PCLK cycle is sufficient for a single byte input calculation. The check result will be obtained instantly after all data inputs are completed. It supports input data high/ low bit reversal and output data high/ low bit reversal. It supports input data with different valid bit widths.

Features of CRC:

- 7/8/16/32-bit CRC calculation
- Any custom polynomial
- Any initial value
- Supports single byte/ double byte/ triple byte/ quadruple byte valid bit width for input data
- Supports byte/ double byte/ quadruple byte high and low bit reversal for input data
- Supports high and low bit reversal for output data
- Calculation speed is 1 byte per PCLK cycle

3.6.3 True Random Number Generator (TRNG)

The TRNG (True Random Number Generator) is a module that generates random numbers based on the instability of oscillation circuits. No external random entropy source is required for this module, and the random numbers can be generated by activating multiple internal oscillation circuits with a certain entropy source processing logic.

Features of TRNG:

- Independent internal entropy source
- Generate 256-bit seeds and 256-bit random numbers in a single pass
- Deadlock check against entropy source

3.7 Memory Interfaces

3.7.1 QSPI Interface

The QSPI controller is a dedicated off-chip memory communication interface for NOR/ NAND Flash and pSRAM memory particles with single- wire, dual- wire and quad-wire SPI. Various operations can be implemented by the CPU via register or AHB address mapping. The controller also supports Dual Flash mode to further increase bandwidth and capacity.

The QSPI controller supports two modes of operation: (1) register mode and (2) address-mappping mode. The switching between the two modes is automatically completed by the hardware and can be dynamically interspersed for execution. In either mode, highly customizable SPI command timing is supported for compatibility with various memory particles.

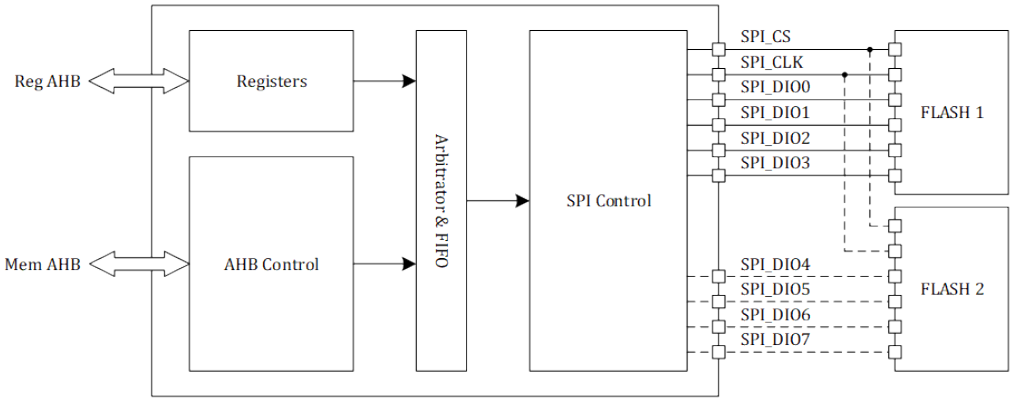


Figure 3-10: QSPI Controller Block Diagram

Register Mode:

- Send a SPI command timing via register operation. The command can also be set as a status query command to be sent repeatedly until the read back data meets a preset status
- Support sending a sequence of two SPI command timings, the second of which can be set as a status query command to be sent repeatedly until the read back data meets a preset status
- Support DMA channels for FIFO data handling

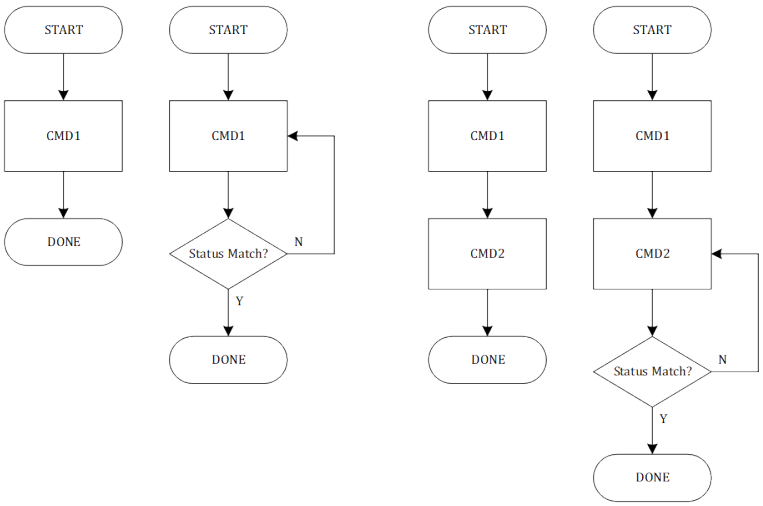


Figure 3-11: Sequence of Single and Multiple Command Timings in Register Mode

Address mapping mode:

- Map the external memory to the AHB address space, and convert the bus read and write to the preset SPI command timing
- Support Byte (8-bit), Half-word (16-bit) and Word (32-bit) AHB access
- Efficient conversion of AHB Wrap operations to meet XIP real-time requirements
- Support XIP real-time (On-The-Fly) decryption, the mode is AES128-CTR or AES256-CTR
- Support Resume function, CS can be selectively pulled low after a single access, if the next read address is consecutive with the previous one, the data will be read directly, omitting the command and address part

3.7.2 OPI-PSRAM Interface

The OPI-PSRAM interface provides access to off-chip PSRAM through address mapping, supporting both direct CPU access and DMA access.

Features of OPI-PSRAM:

- Support OPI DDR PSRAM, the maximum clock frequency is 120MHz
- The maximum addressing range is 256Mb
- Support 8-bit or 16-bit bus bandwidth
- Built-in transceiver FIFO
- Support 8/16/32-bit wide access
- Support DMA access
- Timeout mechanism

3.7.3 SD/SDIO/eMMC

SDMMC supports SD protocol 3.0 and eMMC standard 4.51, and can be used as a HOST controller to interact with SD/SDIO/eMMC devices. SDMMC has a built-in chained DMA controller and 1K byte FIFO, which can read and write data independently, supporting block data handling. SDMMC supports SDR single-wire, 4-wire and 8-wire modes, and supports DDR 4-wire modes.

Features of SDMMC:

- Compatible with SD Host Controller Standard Specification Version 3.0
- Compatible with SD 3.0 Physical Layer Specification Version 3.01
- Compatible with SDIO Specification Version 3.0
- Compatible with JEDEC JESD84-B451 eMMC 4.51 Specification
- Support SDSC/SDHC/SDXC/SDHS card
- Support UHS-1: SDR12/SDR25/DDR50
- Support SDR single-wire, 4-wire and 8-wire modes
- Support DDR 4-wire modes
- Built-in 1K byte FIFO, support up to 512 bytes in a single block
- Configurable clock
- Built-in chained DMA

3.8 Summary of Peripheral Interface Rates

Table 3-2: Common Interface Rates

Controller	Max. Rate	Unit	Remarks
QSPI1	96	MHz	SiP NOR Flash
QSPI2	60	MHz	External NOR/NAND Flash or QSPI-PSRAM
QSPI3	60	MHz	External NOR/NAND Flash or QSPI-PSRAM
QSPI4	48	MHz	External NOR Flash
PSRAMC	120	MHz	External or SiP OPI-PSRAM
SDMMC	48	MHz	
I2C	3.4	MHz	
SPI1/2	48	MHz	
SPI3/4	8	MHz	
UART	3	Mbaud	
I2S	48	KHz	Sampling rate 48KHz, 32-bit×2 channel
GPADC	3	Msps	
SDADC	4	Ksps	

4 Electrical Characteristics

4.1 Basic Electrical Characteristics

Table 4-1: Operating Conditions

Symbol	Description	Min	Typ	Max	Unit
VDD	Power supply voltage from external source	1.7	3.3	3.6	V
T_{amb}	Ambient temperature	-40	25	85	°C
V_{IL}	CMOS low level input voltage	0		$0.3\times V_{IO}$	V
V_{IH}	CMOS high level input voltage	$0.7\times V_{IO}$			V
V_{TH}	CMOS threshold voltage		$0.5\times V_{IO}$		V

Table 4-2: Absolute Max. Values

Symbol	Description	Min	Typ	Max	Unit
VDD	Power supply voltage from external source			3.8	V
$T_{Storage}$	Storage temperature	-40		125	°C
V_{IN}	Input voltage	0		V_{IO}+0.3	V
V_{LNA}	LNA input level			0	dBm
I_{IN}	Input current			20	mA

Table 4-3: I/O characteristics @3.3V

Symbol	Description	Min	Typ	Max	Unit
C_{IN}	pipe foot capacitor	2.5	3	3.5	pF
V_{IH}	high-level input voltage	0.7*VDDIOA	-	VDDIOA	V
V_{IL}	low-level input voltage	VSS	-	0.3*VDDIOA	V
I_{IH}	high-level input current	-	10	40	nA
I_{IL}	low-level input current	-	10	40	nA
V_{OH}	high-level output voltage (high-resistance load)	0.8*VDDIOA	-	VDDIOA	V
V_{OL}	low-level output voltage (high-resistance load)	VSS	-	0.2*VDDIOA	V
I_{OH}	high-level driving current (V_{OH}=0.8*VDDIOA,max driver)	12	30	38	mA
I_{OL}	low-level driving current (V_{OH}=0.2*VDDIOA,max driver)	12	30	38	mA
R_{PU}	internal pull-up resistance	7	10	20	kΩ
R_{PD}	internal pull-down resistance	7	10	20	kΩ
V_{IH_nRST}	chip reset release voltage	0.7*VDD	-	VDD	V
V_{IL_nRST}	chip reset voltage	VSS	-	0.3*VDD	V

4.2 Reliability

Table 4-4: Reliability Test

Test Item	Test Condition		Applicable Product	Test Criteria
HTOL	125°C, 1000 hours		SF32LB55x	JESD22-A108
ESD	HBM（HUMAN BODY MODE）	± 4000 V	SF32LB551x	JS-001-2017
		± 2000 V	SF32LB555x	JS-001-2017
	CDM（CHARGE DEVICE MODE）	±1000V	SF32LB55x	JS-002-2018
	MM (MACHINE MODE)	± 200V	SF32LB55x	JESD22-A115C
Latch-up	LU (LATCH-UP)	I-Test: ± 200mA	SF32LB55x	JESD78E
		OVT: +1.5×Vdd_{MAX}	SF32LB55x	
MSL3	Baking: 125°C, 24 hours Soaking: 30°C, 60% RH, 192 hours Reflow Soldering: 260 + 0°C, 20 seconds, 3 times		SF32LB55x	J-STD-020 JESD47 JESD22-A113
TCT	-65°C~150°C, 1000 cycles		SF32LB55x	JESD22-A104
uHAST	130°C, 85% RH, 96 hours		SF32LB55x	JESD22-A118
HTSL	150°C, 1000 hours		SF32LB55x	JESD22-A103
LTSL	-40°C, 1000 hours		SF32LB55x	JESD22-A119
PCT	QFN: 121°C, 100% RH, 29.7PSI, 96 hours		SF32LB551x	JESD22-A102
Solderability	QFN: 245±5°C, Aging 8 hours		SF32LB551x	J-STD-002D-2013

4.3 Power Consumption Characteristics

4.3.1 Power Off Power Consumption

Table 4-5: Power Off Power Consumption

Symbol	1.8V (Typical)	Unit
$I_{POWER\ OFF\ (RTC\ wakeup)}$	600	nA
$I_{POWER\ OFF\ (Key\ wakeup)}$	280	nA

4.3.2 Processor Power Consumption

Table 4-6: Processor Power Consumption (SF32LB551)

Symbol	Condition		3.3V (Typical)	1.8V (Typical)	Unit
$I_{CoreMark}$	HPSYS	240MHz	9.8	18.0	mA
		192MHz	8.2	15.1	mA
	LPSYS	48MHz	0.933	1.710	mA
		24MHz	0.566	1.038	mA
$I_{WhileLoop}$	HPSYS	240MHz	6.7	12.3	mA
		192MHz	5.7	10.5	mA
	LPSYS	48MHz	0.715	1.310	mA
		24MHz	0.455	0.835	mA

Table 4-7: Processor Power Consumption (SF32LB555)

Symbol	Condition		3.3V (Typical)	1.8V (Typical)	Unit
$I_{CoreMark}$	HPSYS	240MHz	9.3	17.0	mA
		192MHz	7.7	14.1	mA
	LPSYS	48MHz	0.728	1.334	mA
		24MHz	0.445	0.816	mA
$I_{WhileLoop}$	HPSYS	240MHz	6.2	11.3	mA
		192MHz	5.2	9.6	mA
	LPSYS	48MHz	0.537	0.985	mA
		24MHz	0.349	0.639	mA

4.3.3 BLE Power Consumption

Table 4-8: BLE Power Consumption

Symbol	Condition	3.3V[a] (Typical)	1.8V [b] (Typical)	Unit
$I_{\triangle TX}$	TX_{POWER}=0dBm	2.9	5.0	mA
$I_{\triangle TX}$	TX_{POWER}=4dBm	5.5	9.2	mA
$I_{\triangle TX}$	TX_{POWER}=10dBm	16.4	3.0[c]	mA
			14.6[d]	mA
$I_{\triangle RX}$		2.0	3.6	mA
I_{SLEEP}		2.7	5.0	uA

[a] In Table 4-8, 3.3V refers to that VDD1, VDD2, AVDD33, AVDD_DSI and AVDD_BRF are 3.3V power supply.

[b] 1.8V refers to that VDD1, VDD2, AVDD_DSI and AVDD_BRF are 1.8V power supply, AVDD33 is 3.3V power supply.

[c] For 1.8V power supply, when TX_{POWER}=10dBm, the total power consumption of VDD1, VDD2, AVDD33, AVDD_DSI and AVDD_BRF would be around 3.0mA.

[d] For 1.8V power supply, when TX_{POWER}=10dBm, the power consumption of AVDD33 is 14.6mA.

4.3.4 BLE ADV Scenario

Table 4-9: BLE ADV Scenario

Symbol	Condition		3.3V (Typical)	1.8V (Typical)	Unit
	BT TX Power	ADV Interval			
$I_{ADV\_AVERAGE}$	0dBm	50ms	151	276.8	uA
		200ms	43	78.8	uA
		500ms	17.9	32.9	uA
		1000ms	10.5	19.2	uA

4.3.5 BLE Connection Scenario

Table 4-10: BLE Connection Scenario

Symbol	Condition		3.3V [a] (Typical)	1.8V [b] (Typical)	Unit
	BT TX Power	Connection Interval			
$I_{Connection\_AVERAGE}$	0dBm	50ms	106.1	194.5	uA
		200ms	30.1	55.1	uA
		500ms	14.7	26.9	uA
		1000ms	9.5	17.5	uA

[a] The above 3.3V power consumption data is calculated based on the test data of 1.8V power supply (assuming 3.3V power supply and 100% power conversion efficiency), the calculation formula: $I_{3V3} = I_{1V8} \times 1.8/3.3$.

[b] The above power consumption is the sum of VDD1, VDD2, AVDD33, AVDD_DSI and AVDD_BRF currents of SF32LB55x.

4.4 Bluetooth RF

4.4.1 Transmitter Performance

Table 4-11: Transmitter Performance - 1Mbps Mode

Parameter	Condition	Min	Typ	Max	Unit
Maximum RF transmit power			10		dBm
RF power control range		-20		10	dBm
Adjacent channel transmit power (@+10dm transmit power)	F = F_0+1MHz		-40		dBm
	F = F_0-1MHz		-40		dBm
	F = F_0+2MHz		-45		dBm
	F = F_0-2MHz		-45		dBm
	F = F_0+3MHz		-45		dBm
	F = F_0-3MHz		-45		dBm
	F = F_0+>3MHz		-45		dBm
	F = F_0->3MHz		-45		dBm
Δf_{1avg} Maximum modulation		225	250	275	kHz
Δf_{2max} Minimum modulation		185	210		kHz
$\Delta f_{2avg}/\Delta f_{1avg}$		0.8	0.89		
ICFT		-150	±20	150	kHz
Drift rate		-20	±4	20	kHz/50us
Drift		-50	±4	50	kHz
Harmonic spur (@+10dm transmit power)	Second harmonic		-55		dBm
	Third harmonic		-55		dBm

Table 4-12: Transmitter Performance - 2Mbps Mode

Parameter	Condition	Min	Typ	Max	Unit
Maximum RF transmit power			10		dBm
RF power control range		-20		10	dBm
Adjacent channel transmit power (@+10dm transmit power)	F = F_0+4MHz		-40		dBm
	F = F_0-4MHz		-40		dBm
	F = F_0+5MHz		-40		dBm
	F = F_0-5MHz		-40		dBm
	F = F_0+>5MHz		-40		dBm
	F = F_0->5MHz		-40		dBm
Δf_{1avg} Maximum modulation		450	500	550	kHz
Δf_{2max} Minimum modulation		370	420		kHz
$\Delta f_{2avg}/\Delta f_{1avg}$		0.8	0.89		
ICFT		-150	±20	150	kHz
Drift rate		-20	±4	20	kHz/50us
Drift		-50	±4	50	kHz
Harmonic Spur (@+10dm transmit power)	Second harmonic		-55		dBm
	Third harmonic		-55		dBm

4.4.2 Receiver Performance

Table 4-13: Receiver Performance - 125Kbps Mode

Parameter	Condition	Min	Typ	Max	Unit
Sensitivity with dirty transmit off@30.8% PER & 37bytes		-108.5	-108		dBm
Sensitivity with dirty transmit on@30.8% PER & 37bytes		-108	-107.5		dBm
Maximum received signal@30.8% PER			20		dBm
C/I co-channel		0.9	1		dB
Adjacent channel selectivity C/I	F = F0+1MHz		-12		dB
	F = F0-1MHz		-9		dB
	F = F0+2MHz		-48		dB
	F = F0-2MHz		-44		dB
	F = F0+3MHz		-58		dB
	F = F0-3MHz		-44		dB
Adjacent channel selectivity C/I	F = Fimage(F0-4MHz)		-32		dB

Table 4-14: Receiver Performance - 500Kbps Mode

Parameter	Condition	Min	Typ	Max	Unit
Sensitivity with dirty transmit off@30.8% PER & 37bytes		-105	-104.5		dBm
Sensitivity with dirty transmit on@30.8% PER & 37bytes		-104.3	-104		dBm
Maximum received signal@30.8% PER			20		dBm
C/I co-channel		1.7	2		dB
Adjacent channel selectivity C/I	F = F0+1MHz		-12		dB
	F = F0-1MHz		-9		dB
	F = F0+2MHz		-48		dB
	F = F0-2MHz		-43		dB
	F = F0+3MHz		-58		dB
	F = F0-3MHz		-43		dB
Adjacent channel selectivity C/I	F = Fimage(F0-4MHz)		-31		dB

Table 4-15: Receiver Performance - 1Mbps Mode

Parameter	Condition	Min	Typ	Max	Unit
Sensitivity with dirty off@30.8% PER & 37bytes		-100.5	-100		dBm
Sensitivity with dirty on@30.8% PER & 37bytes		-99.8	-99.3		dBm
Maximum received signal@30.8% PER			20		dBm
C/I co-channel		6.6	7		dB
Adjacent channel selectivity C/I	F = F_0+1MHz		-10		dB
	F = F_0-1MHz		-7		dB
	F = F_0+2MHz		-43		dB
	F = F_0-2MHz		-40		dB
	F = F_0+3MHz		-50		dB
	F = F_0-3MHz		-40		dB
Adjacent channel selectivity C/I	F = F_{image}(F_0-4MHz)	-38	-24		dB
Out of band blocking performance	30MHz 2000MHz		-15		dBm
	2000MHz-2400MHz		-18		dBm
	2500-3000MHz		-15		dBm
	3000MHz-12.5GHz		-10		dBm
Intermodulation			-22		dBm

Table 4-16: Receiver Performance - 2Mbps Mode

Parameter	Condition	Min	Typ	Max	Unit
Sensitivity with dirty off@30.8% PER & 37bytes		-98	-97.5		dBm
Sensitivity with dirty on@30.8% PER & 37bytes		-96.8	-96.3		dBm
Maximum received signal@30.8% PER			20		dBm
C/I co-channel		6.6	7		dB
Adjacent channel selectivity C/I	F = F_0+2MHz		-10		dB
	F = F_0-2MHz		-8		dB
	F = F_0+4MHz		-44		dB
	F = F_0-4MHz		-34		dB
	F = F_0+6MHz		-50		dB
	F = F_0-6MHz		-24		dB
Adjacent channel selectivity C/I	F = F_{image}(F_0-4MHz)	-38	-24		dB
Out of band blocking performance	30MHz 2000MHz		-15		dBm
	2000MHz-2400MHz		-18		dBm
	2500-3000MHz		-15		dBm
	3000MHz-12.5GHz		-10		dBm
Intermodulation			-22		dBm

4.5 IO Drive Strength

Table 4-17: IO Drive Strength

DS0	DS1	Driving Capability
0	0	2mA
0	1	4mA
1	0	8mA
1	1	12mA

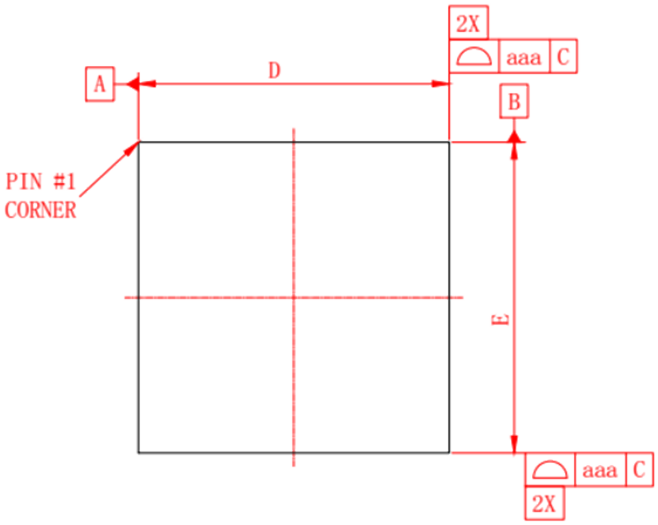
5 Packaging and Hardware

5.1 Pin Layout and Package Information

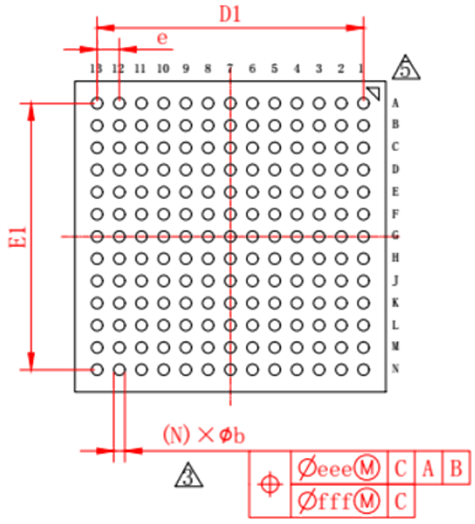
5.1.1 SF32LB557（BGA169）

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	A1 VDD1	A2 BUCK2_VOUT	A3 BUCK2_VSW	A4 VSS	A5 XTAL32K_XO	A6 XTAL32K_XI	A7 VDDIOB	A8 PB<33>	A9 XTAL48M_XI	A10 XTAL48M_XO	A11 VSS	A12 PB<25>	A13 PB<26>
B	B1 BUCK1_VSW	B2 VDD2	B3 PVSS2	B4 LDOVCC2_VOUT	B5 PB<38>	B6 PB<43>	B7 PB<39>	B8 PB<32>	B9 PB<28>	B10 AVSS1	B11 VSS	B12 PB<24>	B13 PB<27>
C	C1 BUCK1_VOUT	C2 VDD_RET	C3 VDD_RTC	C4 PB<41>	C5 PB<48>	C6 PB<44>	C7 PB<34>	C8 PB<31>	C9 PB<29>	C10 PB<11>	C11 PB<22>	C12 AVSS2	C13 AVSS4
D	D1 LDO_VOUT2	D2 PVSS1	D3 RSTN	D4 PB<40>	D5 PB<47>	D6 PB<46>	D7 PB<36>	D8 PB<30>	D9 PB<8>	D10 PB<14>	D11 NC	D12 AVSS3	D13 ANT
E	E1 LDO_VOUT1	E2 VSS	E3 PA<78>	E4 PA<79>	E5 PA<80>	E6 PB<45>	E7 PB<37>	E8 PB<35>	E9 NC	E10 PB<10>	E11 PB<20>	E12 AVDD_BRF	E13 AVSS5
F	F1 VDD_SIP	F2 VSS	F3 PA<77>	F4 PA<66>	F5 PA<51>	F6 PA<48>	F7 PA<46>	F8 PB<5>	F9 PB<6>	F10 PB<19>	F11 PB<15>	F12 AVDD33	F13 SDMADC_VREF
G	G1 PA<68>	G2 PA<70>	G3 PA<67>	G4 PA<65>	G5 PA<53>	G6 PA<47>	G7 PA<45>	G8 PA<18>	G9 PB<4>	G10 PB<9>	G11 PB<16>	G12 AVSS33	G13 SDMADC_INPUT
H	H1 PA<64>	H2 DSI_DP1	H3 DSI_DN1	H4 PA<63>	H5 PA<44>	H6 PA<29>	H7 PA<27>	H8 PA<20>	H9 PA<4>	H10 PA<14>	H11 PA<6>	H12 PB<23>	H13 SDMADC_VSS_VREF
J	J1 DSI_REXT	J2 DSI_CLKP	J3 DSI_CLKN	J4 PA<55>	J5 PA<34>	J6 PA<31>	J7 PA<25>	J8 PA<15>	J9 PA<12>	J10 PA<10>	J11 PB<13>	J12 PB<17>	J13 PB<18>
K	K1 AVDD_DSI	K2 DSI_DP0	K3 DSI_DN0	K4 PA<54>	K5 PA<43>	K6 PA<36>	K7 PA<28>	K8 PA<26>	K9 MODE	K10 PA<8>	K11 PA<0>	K12 NC	K13 PB<12>
L	L1 AVSS_DSI	L2 PA<58>	L3 PA<56>	L4 PA<52>	L5 PA<38>	L6 PA<37>	L7 PA<23>	L8 PA<30>	L9 PA<22>	L10 PA<2>	L11 NC	L12 VSS	L13 NC
M	M1 PA<62>	M2 PA<60>	M3 VSS	M4 PA<50>	M5 PA<41>	M6 PA<35>	M7 PA<32>	M8 PA<19>	M9 PA<24>	M10 PA<11>	M11 PA<7>	M12 PA<3>	M13 NC
N	N1 PA<61>	N2 PA<59>	N3 PA<57>	N4 PA<49>	N5 PA<42>	N6 VDDIOA	N7 PA<33>	N8 PA<21>	N9 PA<17>	N10 PA<13>	N11 PA<9>	N12 PA<5>	N13 PA<1>

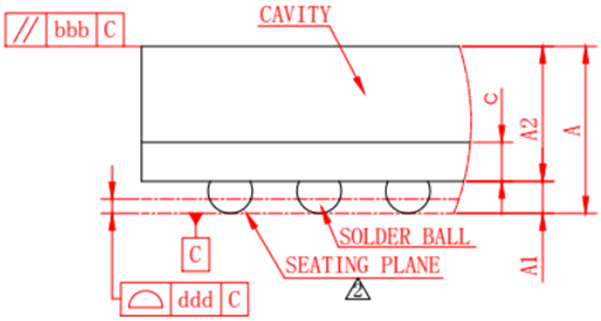
Figure 5-1: SF32LB557（BGA169）Pin Layout（Top View）



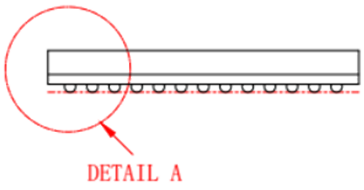
Top View



Bottom View



DETAIL A



Side View

symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.840	0.940	1.040	0.033	0.037	0.041
A1	0.130	0.180	0.230	0.005	0.007	0.009
A2	0.710	0.760	0.810	0.028	0.030	0.032
c	0.180	0.220	0.260	0.007	0.009	0.010
D	6.900	7.000	7.100	0.272	0.276	0.280
E	6.900	7.000	7.100	0.272	0.276	0.280
D1	---	6.000	---	---	0.236	---
E1	---	6.000	---	---	0.236	---
e	---	0.500	---	---	0.020	---
b	0.200	0.250	0.300	0.008	0.010	0.012
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.050			0.002		
Ball Diam	0.250			0.010		
N	169			169		
MD/ME	13/13			13/13		

TECHNOLOGY SPECIFICATION[技术要求]

1. BALL PAD OPENING: 0.230mm; [球形防焊开口: 0.230mm;]

⚠3 PRIMARY DATUM C AND SEATING PLANE ARE THE SOLDER BALLS;
[主要基准C和底面是锡球;]

⚠4 DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C; [尺寸b是测量最大锡球直径, 平行于主要基准C;]

4. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd; [特殊特性C类: bbb, ddd;]

⚠5 THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY;
[PIN 1 标识仅供参考;]

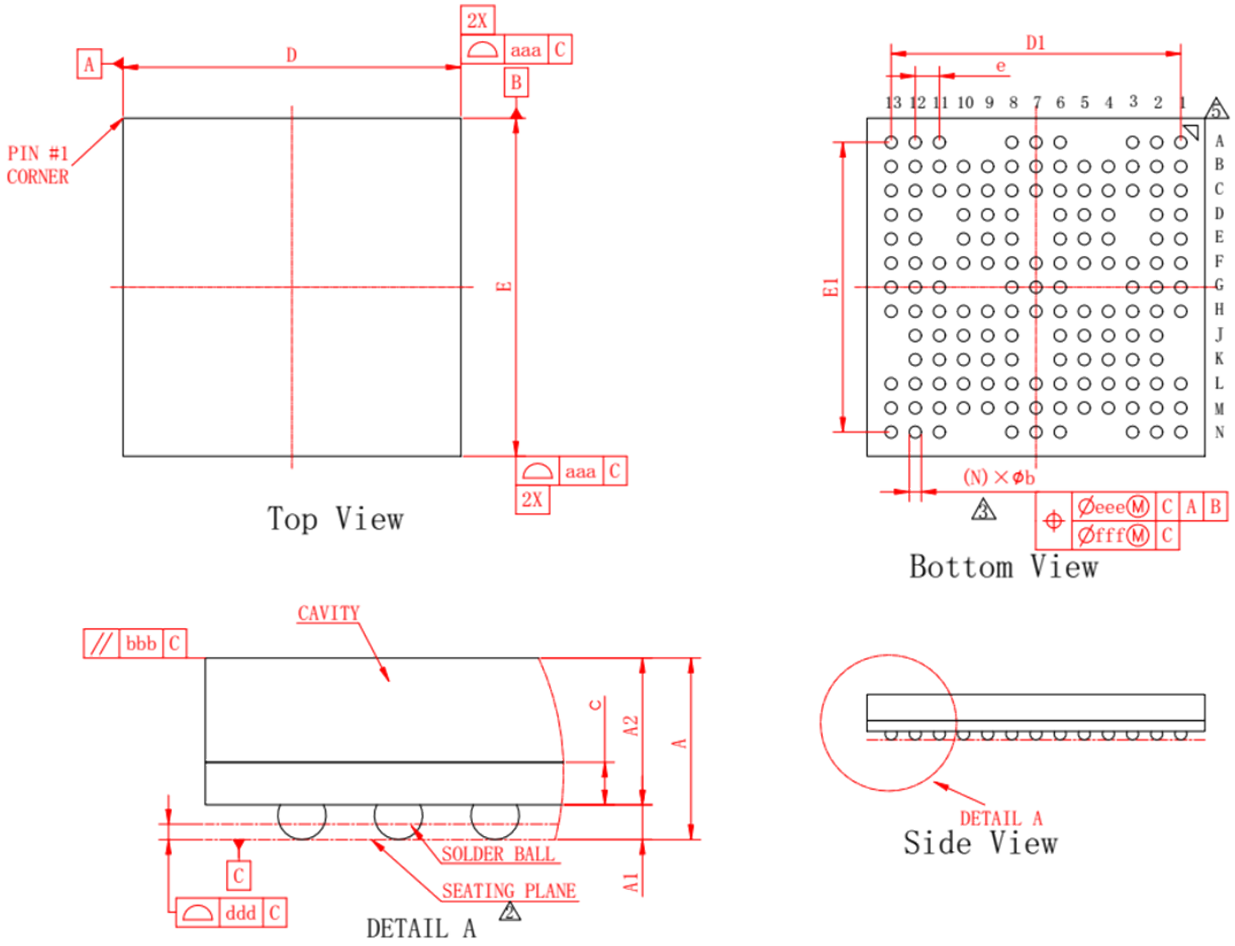
6. BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES;
[禁止使用一级环境管理物质;]

Figure 5-2: SF32LB557 (BGA169) Package Information

5.1.2 SF32LB555（BGA145）

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	A1 RSTN	A2 VDD1	A3 BUCK2_VSW			A6 VDD_RTC	A7 XTAL32K_XI	A8 XTAL48M_XI			A11 PB<29>	A12 PB<25>	A13 PB<26>
B	B1 BUCK1_VSW	B2 VDD2	B3 BUCK2_VOUT	B4 LDOVCC2_VOUT	B5 VDD_RET	B6 PB<34>	B7 XTAL32K_XO	B8 AVSS1	B9 XTAL48M_XO	B10 PB<28>	B11 PB<30>	B12 PB<24>	B13 PB<27>
C	C1 BUCK1_VOUT	C2 PA<80>	C3 PVSS1	C4 PVSS2	C5 PB<45>	C6 PB<43>	C7 PB<33>	C8 PB<15>	C9 PB<19>	C10 PB<23>	C11 PB<31>	C12 AVSS2	C13 AVSS4
D	D1 LDO_VOUT2	D2 PA<79>		D4 PB<48>	D5 PB<44>	D6 PB<36>		D8 PB<14>	D9 PB<16>	D10 PB<22>		D12 AVSS3	D13 ANT
E	E1 LDO_VOUT1	E2 PA<78>		E4 PB<47>	E5 PB<37>	E6 PB<35>		E8 PB<32>	E9 PB<13>	E10 PB<18>		E12 AVDD_BRF	E13 AVSS5
F	F1 VDD_SIP	F2 PA<77>	F3 PA<70>	F4 PA<68>	F5 PB<46>	F6 VSS	F7 VSS	F8 VSS	F9 PB<12>	F10 PB<17>	F11 PB<11>	F12 AVDD33	F13 SDMADC_VREF
G	G1 PA<66>	G2 PA<65>	G3 DSI_REXT			G6 VSS	G7 VSS	G8 VSS			G11 PB<10>	G12 AVSS33	G13 SDMADC_INPUT
H	H1 PA<63>	H2 DSI_DP1	H3 DSI_DN1	H4 AVSS_DSI	H5 PA<55>	H6 PA<48>	H7 VSS	H8 MODE	H9 PB<7>	H10 PB<6>	H11 PB<9>	H13 VDDIOB	H13 SDMADC_VSS_VREF
J		J2 DSI_CLKP	J3 DSI_CLKN	J4 AVDD_DSI	J5 PA<54>	J6 PA<47>		J8 PA<30>	J9 PA<20>	J10 PA<10>	J11 PB<5>	J12 PB<8>	
K		K2 DSI_DP0	K3 DSI_DN0	K4 PA<56>	K5 PA<46>	K6 PA<43>		K8 PA<28>	K9 PA<14>	K10 PA<0>	K11 PB<1>	K12 PB<4>	
L	L1 PA<61>	L2 PA<60>	L3 PA<57>	L4 PA<49>	L5 PA<42>	L6 PA<41>	L7 PA<36>	L8 PA<34>	L9 PA<8>	L10 PA<6>	L11 PA<5>	L12 PA<1>	L13 PB<3>
M	M1 PA<58>	M2 PA<53>	M3 PA<51>	M4 PA<44>	M5 PA<38>	M6 PA<37>	M7 PA<35>	M8 PA<29>	M9 PA<25>	M10 PA<21>	M11 PA<19>	M12 PA<7>	M13 PA<3>
N	N1 PA<52>	N2 PA<50>	N3 PA<45>			N6 VDDIOA	N7 PA<31>	N8 PA<27>			N11 PA<23>	N12 PA<17>	N13 PA<9>

Figure 5-3: SF32LB555 (BGA145) Pin Layout (Top View)



symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.840	0.940	1.040	0.033	0.037	0.041
A1	0.130	0.180	0.230	0.005	0.007	0.009
A2	0.710	0.760	0.810	0.028	0.030	0.032
c	0.180	0.220	0.260	0.007	0.009	0.010
D	6.900	7.000	7.100	0.272	0.276	0.280
E	6.900	7.000	7.100	0.272	0.276	0.280
D1	---	6.000	---	---	0.236	---
E1	---	6.000	---	---	0.236	---
e	---	0.500	---	---	0.020	---
b	0.200	0.250	0.300	0.008	0.010	0.012
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.050			0.002		
Ball Diam	0.250			0.010		
N	145			145		
MD/ME	13/13			13/13		

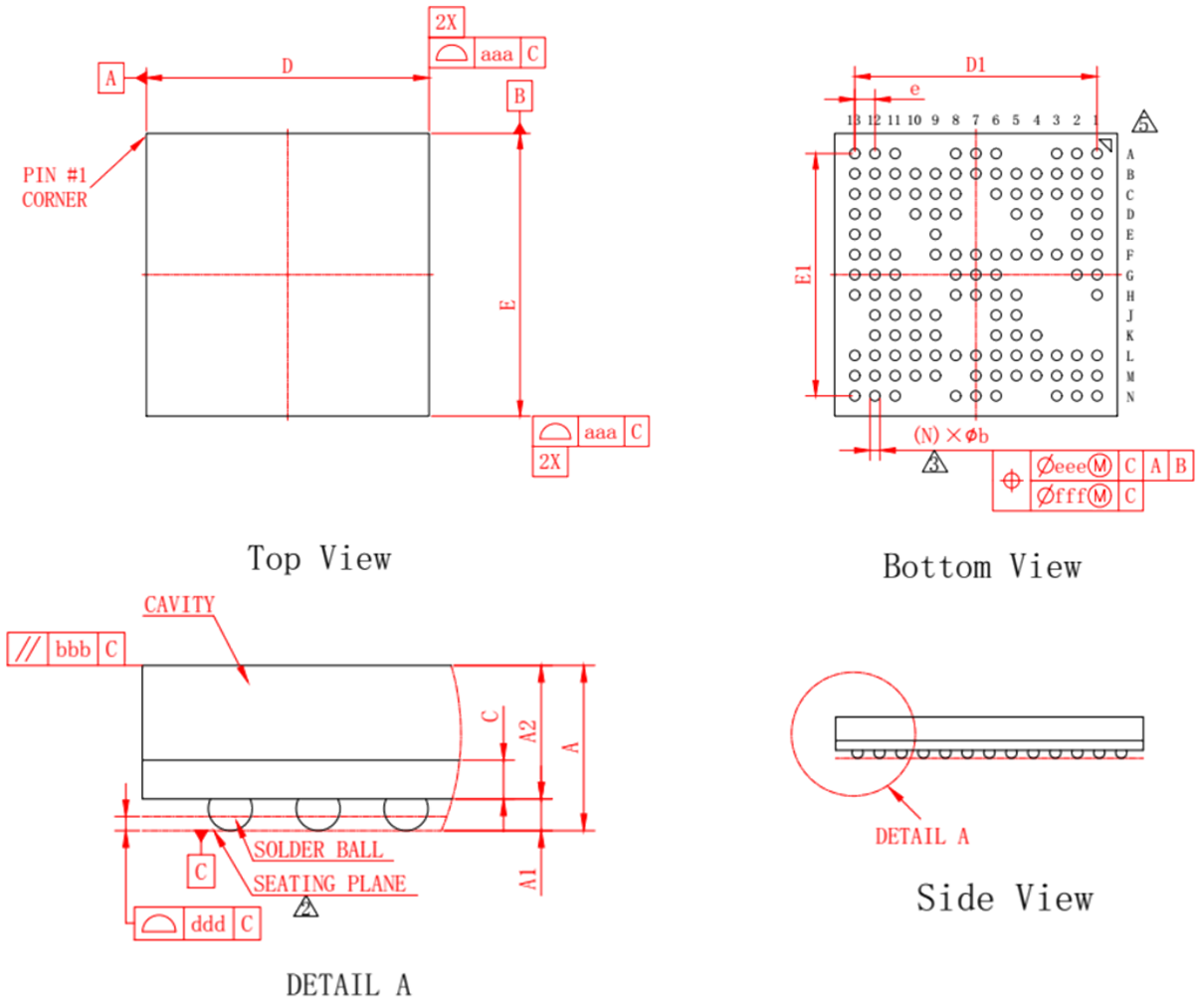
TECHNOLOGY SPECIFICATION[技术要求]
1. BALL PAD OPENING: 0.23mm; [球形防焊开口: 0.23mm;]
⚠4 PRIMARY DATUM C AND SEATING PLANE ARE THE SOLDER BALLS;
[主要基准C和底面是锡球;]
⚠4 DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C; [尺寸b是测量最大锡球直径, 平行于主要基准C;]
4. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd; [特殊特性C类: bbb, ddd;]
⚠5 THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY;
[PIN 1 标识仅供参考;]
6. BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES;
[禁止使用一级环境管理物质;]

Figure 5-4: SF32LB555 (BGA145) Package Information

5.1.3 SF32LB553（BGA125）

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	A1 RSTN	A2 VDD1	A3 BUCK2_VSW			A6 VDD_RTC	A7 XTAL32K_XI	A8 XTAL48M_XI			A11 PB<29>	A12 PB<25>	A13 PB<26>
B	B1 BUCK1_VSW	B2 VDD2	B3 BUCK2_VOUT	B4 LDOVCC2_VOUT	B5 VDD_RET	B6 PB<34>	B7 XTAL32K_XO	B8 AVSS1	B9 XTAL48M_XO	B10 PB<28>	B11 PB<30>	B12 PB<24>	B13 PB<27>
C	C1 BUCK1_VOUT	C2 PA<80>	C3 PVSS1	C4 PVSS2	C5 PB<45>	C6 PB<43>		C8 PB<15>	C9 PB<19>	C10 PB<23>	C11 PB<31>	C12 AVSS2	C13 AVSS4
D	D1 LDO_VOUT2	D2 PA<79>		D4 PB<48>	D5 PB<44>			D8 PB<14>	D9 PB<16>	D10 PB<22>		D12 AVSS3	D13 ANT
E	E1 LDO_VOUT1	E2 PA<78>		E4 PB<47>					E9 PB<13>			E12 AVDD_BRF	E13 AVSS5
F	F1 VDD_SIP	F2 PA<77>	F3 PA<70>	F4 PA<68>	F5 PB<46>	F6 VSS	F7 VSS	F8 VSS	F9 PB<12>		F11 PB<11>	F12 AVDD33	F13 SDMADC_VREF
G	G1 PA<66>	G2 PA<65>				G6 VSS	G7 VSS	G8 VSS			G11 PB<10>	G12 AVSS33	G13 SDMADC_INPUT
H	H1 PA<63>				H5 PA<55>	H6 PA<48>	H7 VSS	H8 MODE		H10 PB<6>	H11 PB<9>	H13 VDDIOB	H13 SDMADC_VSS_VREF
J					J5 PA<54>	J6 PA<47>			J9 PA<20>	J10 PA<10>	J11 PB<5>	J12 PB<8>	
K				K4 PA<56>	K5 PA<46>	K6 PA<43>			K9 PA<14>	K10 PA<0>	K11 PB<1>	K12 PB<4>	
L	L1 PA<61>	L2 PA<60>	L3 PA<57>	L4 PA<49>	L5 PA<42>	L6 PA<41>	L7 PA<36>	L8 PA<34>	L9 PA<8>	L10 PA<6>	L11 PA<5>	L12 PA<1>	L13 PB<3>
M	M1 PA<58>	M2 PA<53>	M3 PA<51>	M4 PA<44>	M5 PA<38>	M6 PA<37>	M7 PA<35>		M9 PA<25>	M10 PA<21>	M11 PA<19>	M12 PA<7>	M13 PA<3>
N	N1 PA<52>	N2 PA<50>	N3 PA<45>			N6 VDDIOA	N7 PA<31>	N8 PA<27>			N11 PA<23>	N12 PA<17>	N13 PA<9>

Figure 5-5: SF32LB553 (BGA125) Pin Layout (Top View)



symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.840	0.940	1.040	0.033	0.037	0.041
A1	0.130	0.180	0.230	0.005	0.007	0.009
A2	0.710	0.760	0.810	0.028	0.030	0.032
c	0.180	0.220	0.260	0.007	0.009	0.010
D	6.900	7.000	7.100	0.272	0.276	0.280
E	6.900	7.000	7.100	0.272	0.276	0.280
D1	---	6.000	---	---	0.236	---
E1	---	6.000	---	---	0.236	---
e	---	0.500	---	---	0.020	---
b	0.200	0.250	0.300	0.008	0.010	0.012
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.050			0.002		
Ball Diam	0.250			0.010		
N	125			125		
MD/ME	13/13			13/13		

TECHNOLOGY SPECIFICATION[技术要求]

1. BALL PAD OPENING: 0.230mm; [球形防焊开口: 0.230mm;]

⚠4 PRIMARY DATUM C AND SEATING PLANE ARE THE SOLDER BALLS;
[主要基准C和底面是锡球;]

⚠3 DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C; [尺寸b是测量最大锡球直径, 平行于主要基准C;]

4. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd; [特殊特性C类: bbb, ddd;]

⚠5 THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY;
[PIN 1 标识仅供参考;]

6. BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES;
[禁止使用一级环境管理物质;]

Figure 5-6: SF32LB553 (BGA125) Package Information

5.1.4 SF32LB551（QFN68L）

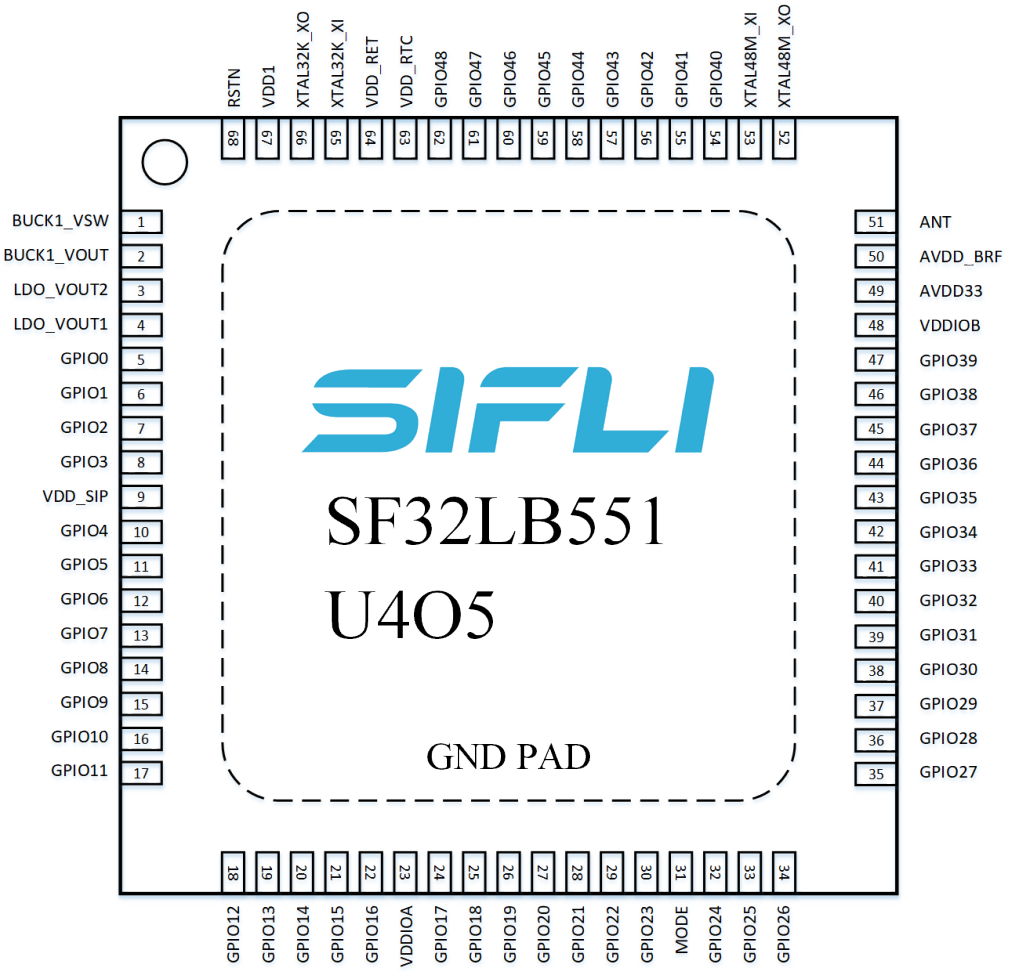
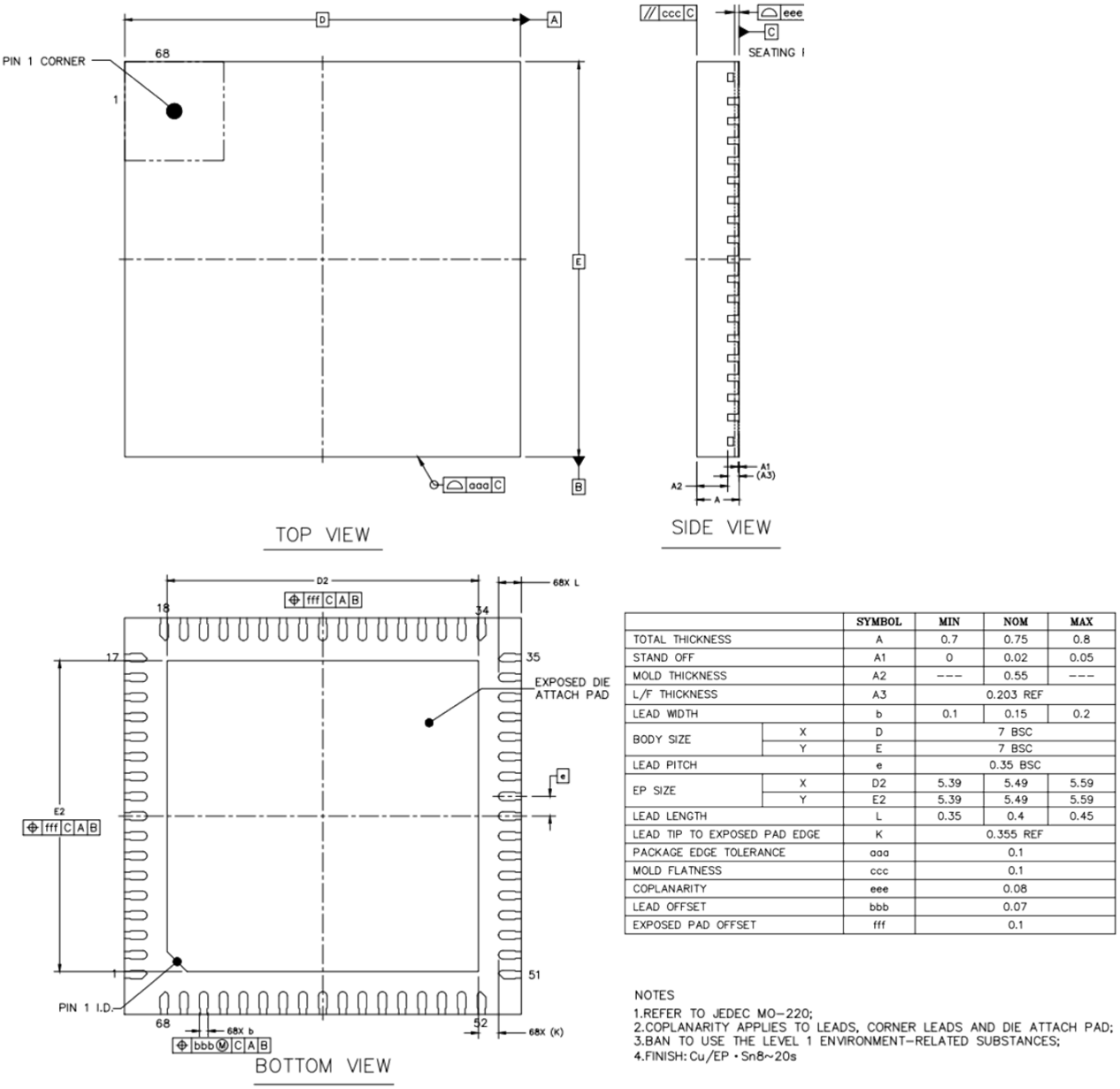


Figure 5-7: SF32LB551 (QFN68L) Pin Layout (Top View)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.1	0.15	0.2
BODY SIZE	X	D		7 BSC	
	Y	E		7 BSC	
LEAD PITCH		e		0.35 BSC	
EP SIZE	X	D2	5.39	5.49	5.59
	Y	E2	5.39	5.49	5.59
LEAD LENGTH		L	0.35	0.4	0.45
LEAD TIP TO EXPOSED PAD EDGE		K		0.355 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES;
4.FINISH: Cu/EP • Sn8~20s

Figure 5-8: SF32LB551 (QFN68L) Package Information

5.2 Pin Description

The pin types of this chip are shown in Table 5-1, and the following text will describe the big core domain GPIO, LITTLE core domain GPIO, and other dedicated pins respectively.

Table 5-1: Pin Types

Pin Type	Description
I/O	Digital input/output
I	Digital input
O	Digital output
A, I	Analog input
A, O	Analog output
A, I/O	Analog input/output
PWR	Power
GND	Ground

Notes:

- In low-power scenarios, floating inputs may cause the power consumption of digital I/Os with the input function turned on to rise, so such I/Os need to be configured with a determined voltage according to their function, either by connecting to I/Os with determined output voltages on other chips, or by connecting corresponding pull-up or pull-down resistors.

In order to effectively use the chip's I/O resources, some analog IP functions will share pins with digital GPIOs. In the subsequent list, #XXX_XX represents the analog IP functions multiplexed on the I/O at the same time. A brief list of these functions is shown in Table 5-2.

Table 5-2: Analog IP Functions Multiplexed on Digital GPIOs

GPIO#	Analog Port Name	Description
PA01	USB_DP	USB data channel+
PA03	USB_DM	USB data channel-
PA77~78	WKUP_A0~3	Key wakeup I/O A0~3 in HPSYS low-power mode
PB01	LPCOMP1_P	Comparator 1 input+
PB03	LPCOMP1_N	Comparator 1 input-
PB04	LPCOMP2_P	Comparator 2 input+
PB05	LPCOMP2_N	Comparator 2 input-
PB08	GPADC_CH0	SARADC input channel 0
PB10	GPADC_CH1	SARADC input channel 1
PB12	GPADC_CH2	SARADC input channel 2
PB13	GPADC_CH3	SARADC input channel 3
PB16	GPADC_CH4	SARADC input channel 4
PB17	GPADC_CH5	SARADC input channel 5
PB18	GPADC_CH6	SARADC input channel 6
PB19	GPADC_CH7	SARADC input channel 7
PB23	SDADC_CH0	SDADC input channel 0
PB24	SDADC_CH1	SDADC input channel 1
PB25	SDADC_CH2	SDADC input channel 2
PB26	SDADC_CH3	SDADC input channel 3
PB43~48	WKUP_B0~5	Key wakeup I/O B0~5 in HPSYS low-power mode

5.2.1 Big Core Domain GPIO (PA) List

Table 5-3: GPIO (PA) Pin List

Pin Number				Pin Name	Type	Sel #	Function
SF32LB551 QFN68L	SF32LB553 BGA125	SF32LB555 BGA145	SF32LB557 BGA169				
-	K10	K10	K11	PA00	I/O	0	GPIO_A0
						1	QSPI3_CLK
						Others	Reserved
35	L12	L12	N13	PA01	I/O	0	GPIO_A1
						1	QSPI3_CS
						3	LPTIM1_IN
						4	PDM1_CLK
						5	I2S1_BCK
						11	#USB_DP
						Others	Reserved
-	-	-	L10	PA02	I/O	0	GPIO_A2
						2	PSRAM_DQ0
						Others	Reserved
34	M13	M13	M12	PA03	I/O	0	GPIO_A3
						1	QSPI3_DIO0
						3	LPTIM1_OUT
						4	PDM1_DATA
						5	I2S1_SDI
						11	#USB_DM
						Others	Reserved
-	-	-	H9	PA04	I/O	0	GPIO_A4
						2	PSRAM_DQ1
						Others	Reserved
-	L11	L11	N12	PA05	I/O	0	GPIO_A5
						1	QSPI3_DIO1
						2	PSRAM_DQ2
						3	UART2_RXD
						4	PDM1_DATA
						Others	Reserved
-	L10	L10	H11	PA06	I/O	0	GPIO_A6
						2	PSRAM_DQ3
						Others	Reserved
-	M12	M12	M11	PA07	I/O	0	GPIO_A7
						1	QSPI3_DIO2
						2	PSRAM_CS
						3	UART2_TXD
						4	PDM1_CLK
						Others	Reserved

Continued on the next page

Table 5-3: GPIO (PA) Pin List (continued)

Pin Number				Pin Name	Type	Sel #	Function
SF32LB551 QFN68L	SF32LB553 BGA125	SF32LB555 BGA145	SF32LB557 BGA169				
-	L9	L9	K10	PA08	I/O	0	GPIO_A8
						1	QSPI3_DIO3
						2	PSRAM_CLK
						3	UART2_CTS
						4	PSRAM_CLKB
						5	I2S1_LRCK
						Others	Reserved
-	N13	N13	N11	PA09	I/O	0	GPIO_A9
						2	PSRAM_DQ4
						3	UART2_RTS
						Others	Reserved
33	J10	J10	J10	PA10	I/O	0	GPIO_A10
						3	I2C1_SCL
						Others	Reserved
-	-	-	M10	PA11	I/O	0	GPIO_A11
						2	PSRAM_DQ5
						Others	Reserved
-	-	-	J9	PA12	I/O	0	GPIO_A12
						2	PSRAM_DQ6
						Others	Reserved
-	-	-	N10	PA13	I/O	0	GPIO_A13
						2	PSRAM_DQ7
						Others	Reserved
32	K9	K9	H10	PA14	I/O	0	GPIO_A14
						3	I2C1_SDA
						10	GPTIM2_CH4
						Others	Reserved
-	-	-	J8	PA15	I/O	0	GPIO_A15
						2	PSRAM_DQS0
						Others	Reserved
-	-	-	-	PA16	I/O	0	GPIO_A16
						Others	Reserved
-	N12	N12	N9	PA17	I/O	0	GPIO_A17
						3	UART1_TXD
						9	LCDC1_DPI_CLK
						Others	Reserved
-	-	-	G8	PA18	I/O	0	GPIO_A18
						2	PSRAM_DQ8
						3	SPI2_DO
						4	SPI2_DIO
						7	LCDC1_SPI_DIO1
						9	LCDC1_DPI_DE
						Others	Reserved

Continued on the next page

Table 5-3: GPIO (PA) Pin List (continued)

Pin Number				Pin Name	Type	Sel #	Function
SF32LB551 QFN68L	SF32LB553 BGA125	SF32LB555 BGA145	SF32LB557 BGA169				
-	M11	M11	M8	PA19	I/O	0	GPIO_A19
						3	UART1_RXD
						9	LCDC1_DPI_R0
						Others	Reserved
30	J9	J9	H8	PA20	I/O	0	GPIO_A20
						2	PSRAM_CLK
						3	SPI2_CLK
						7	LCDC1_SPI_CLK
						8	LCDC1_8080_WR
						10	LCDC1_JDI_SCLK
						11	LCDC1_JDI_VCK
						Others	Reserved
-	M10	M10	N8	PA21	I/O	0	GPIO_A21
						5	I2S2_SDO
						9	LCDC1_DPI_R1
						Others	Reserved
-	-	-	L9	PA22	I/O	0	GPIO_A22
						2	PSRAM_DQ9
						5	SD2_DIO0
						6	SD1_DIO6
						7	LCDC1_SPI_CS
						9	LCDC1_DPI_R2
						Others	Reserved
-	N11	N11	L7	PA23	I/O	0	GPIO_A23
						4	PDM2_CLK
						5	I2S2_BCK
						9	LCDC1_DPI_R3
						Others	Reserved
-	-	-	M9	PA24	I/O	0	GPIO_A24
						2	PSRAM_DQ10
						5	SD2_DIO2
						6	SD1_DIO7
						9	LCDC1_DPI_R4
						Others	Reserved
-	M9	M9	J7	PA25	I/O	0	GPIO_A25
						5	I2S2_LRCK
						9	LCDC1_DPI_R5
						Others	Reserved
-	-	-	K8	PA26	I/O	0	GPIO_A26
						2	PSRAM_DQS1
						5	SD2_CLK
						9	LCDC1_DPI_R6
						Others	Reserved

Continued on the next page

Table 5-3: GPIO (PA) Pin List (continued)

Pin Number				Pin Name	Type	Sel #	Function
SF32LB551 QFN68L	SF32LB553 BGA125	SF32LB555 BGA145	SF32LB557 BGA169				
-	N8	N8	H7	PA27	I/O	0	GPIO_A27
						4	PDM2_DATA
						5	I2S2_SDI
						9	LCDC1_DPI_R7
						Others	Reserved
-	-	K8	K7	PA28	I/O	0	GPIO_A28
						2	PSRAM_DQ0
						6	SD1_DIO0
						9	LCDC1_DPI_G0
						Others	Reserved
-	-	M8	H6	PA29	I/O	0	GPIO_A29
						2	PSRAM_DQ1
						6	SD1_DIO1
						9	LCDC1_DPI_G1
						Others	Reserved
-	-	J8	L8	PA30	I/O	0	GPIO_A30
						2	PSRAM_DQ2
						6	SD1_DIO2
						9	LCDC1_DPI_G2
						Others	Reserved
29	N7	N7	J6	PA31	I/O	0	GPIO_A31
						2	PSRAM_DQ3
						6	SD1_DIO3
						7	LCDC1_SPI_CS
						8	LCDC1_8080_CS
						9	LCDC1_DPI_G3
						10	LCDC1_JDI_SCS
						11	LCDC1_JDI_VST
						Others	Reserved
-	-	-	M7	PA32	I/O	0	GPIO_A32
						2	PSRAM_DQ11
						3	SPI2_DI
						7	LCDC1_SPI_DIO0
						9	LCDC1_DPI_G4
						Others	Reserved
-	-	-	N7	PA33	I/O	0	GPIO_A33
						2	PSRAM_DQ12
						3	SPI2_CS
						7	LCDC1_SPI_DIO2
						9	LCDC1_DPI_G5
						Others	Reserved

Continued on the next page

Table 5-3: GPIO (PA) Pin List (continued)

Pin Number				Pin Name	Type	Sel #	Function
SF32LB551 QFN68L	SF32LB553 BGA125	SF32LB555 BGA145	SF32LB557 BGA169				
28	L8	L8	J5	PA34	I/O	0	GPIO_A34
						2	PSRAM_DQ4
						6	SD1_CLK
						7	LCDC1_SPI_DIO0
						8	LCDC1_8080_RD
						9	LCDC1_DPI_G6
						10	LCDC1_JDI_SO
						11	LCDC1_JDI_XRST
						Others	Reserved
-	M7	M7	M6	PA35	I/O	0	GPIO_A35
						2	PSRAM_DQS0
						4	PDM1_CLK
						5	I2S1_BCK
						7	LCDC1_SPI_TE
						8	LCDC1_8080_TE
						9	LCDC1_DPI_G7
						Others	Reserved
27	L7	L7	K6	PA36	I/O	0	GPIO_A36
						2	PSRAM_DQ5
						6	SD1_CMD
						7	LCDC1_SPI_DIO1
						8	LCDC1_8080_DC
						9	LCDC1_DPI_B0
						10	LCDC1_JDI_DISP
						11	LCDC1_JDI_HCK
						Others	Reserved
-	M6	M6	L6	PA37	I/O	0	GPIO_A37
						2	PSRAM_CS
						3	SPI2_CLK
						5	I2S1_LRCK
						7	LCDC1_SPI_RSTB
						8	LCDC1_8080_RSTB
						Others	Reserved
26	M5	M5	L5	PA38	I/O	0	GPIO_A38
						2	PSRAM_DQ6
						7	LCDC1_SPI_DIO2
						8	LCDC1_8080_DIO0
						9	LCDC1_DPI_B1
						10	LCDC1_JDI_EXTCOMIN
						11	LCDC1_JDI_HST
						Others	Reserved
-	-	-	-	PA39	I/O	0	GPIO_A39
						Others	Reserved

Continued on the next page

Table 5-3: GPIO (PA) Pin List (continued)

Pin Number				Pin Name	Type	Sel #	Function
SF32LB551 QFN68L	SF32LB553 BGA125	SF32LB555 BGA145	SF32LB557 BGA169				
-	-	-	-	PA40	I/O	0	GPIO_A40
						Others	Reserved
-	L6	L6	M5	PA41	I/O	0	GPIO_A41
						4	SPI2_DI
						9	LCDC1_DPI_B2
						Others	Reserved
25	L5	L5	N5	PA42	I/O	0	GPIO_A42
						2	PSRAM_DQ7
						7	LCDC1_SPI_DIO3
						8	LCDC1_8080_DIO1
						9	LCDC1_DPI_B3
						11	LCDC1_JDI_ENB
						Others	Reserved
-	K6	K6	K5	PA43	I/O	0	GPIO_A43
						9	LCDC1_DPI_B4
						10	GPTIM1_ETR
						Others	Reserved
24	M4	M4	H5	PA44	I/O	0	GPIO_A44
						1	QSPI3_CLK
						4	SPI2_CLK
						5	I2S2_BCK
						6	SD2_CLK
						8	LCDC1_8080_DIO2
						9	LCDC1_DPI_B5
						10	GPTIM1_CH1
						11	LCDC1_JDI_FRP
						Others	Reserved
22	N3	N3	G7	PA45	I/O	0	GPIO_A45
						1	QSPI3_CS
						4	SPI2_CS
						5	I2S2_LRCK
						6	SD2_CMD
						8	LCDC1_8080_DIO3
						9	LCDC1_DPI_B6
						10	GPTIM1_CH2
						11	LCDC1_JDI_XFRP
						Others	Reserved
-	K5	K5	F7	PA46	I/O	0	GPIO_A46
						3	I2C2_SCL
						4	UART1_CTS
						9	LCDC1_DPI_B7
						10	GPTIM1_CH3
						Others	Reserved

Continued on the next page

Table 5-3: GPIO (PA) Pin List (continued)

Pin Number				Pin Name	Type	Sel #	Function
SF32LB551 QFN68L	SF32LB553 BGA125	SF32LB555 BGA145	SF32LB557 BGA169				
21	J6	J6	G6	PA47	I/O	0	GPIO_A47
						1	QSPI3_DIO0
						2	QSPI2_DIO4
						4	SPI2_DI
						5	I2S2_SDI
						6	SD2_DIO0
						7	SD1_DIO4
						8	LCDC1_8080_DIO4
						10	GPTIM1_CH4
						11	LCDC1_JDI_VCOM
						Others	Reserved
-	H6	H6	F6	PA48	I/O	0	GPIO_A48
						3	UART2_TXD
						4	UART1_RTS
						5	I2C2_SDA
						Others	Reserved
20	L4	L4	N4	PA49	I/O	0	GPIO_A49
						1	QSPI3_DIO1
						2	QSPI2_DIO5
						3	UART2_RXD
						4	SPI2_DO
						5	SPI2_DIO
						6	SD2_DIO1
						7	SD1_DIO5
						8	LCDC1_8080_DIO5
						11	LCDC1_JDI_R1
						12	UART1_TXD
						Others	Reserved
-	N2	N2	M4	PA50	I/O	0	GPIO_A50
						3	I2C3_SCL
						4	UART1_TXD
						Others	Reserved
19	M3	M3	F5	PA51	I/O	0	GPIO_A51
						1	QSPI3_DIO2
						2	QSPI2_DIO6
						4	UART1_RXD
						6	SD2_DIO2
						7	SD1_DIO6
						8	LCDC1_8080_DIO6
						11	LCDC1_JDI_R2
						Others	Reserved

Continued on the next page

Table 5-3: GPIO (PA) Pin List (continued)

Pin Number				Pin Name	Type	Sel #	Function
SF32LB551 QFN68L	SF32LB553 BGA125	SF32LB555 BGA145	SF32LB557 BGA169				
-	N1	N1	L4	PA52	I/O	0	GPIO_A52
						2	QSPI2_DIO4
						3	SPI1_CLK
						10	GPTIM2_CH1
						Others	Reserved
-	M2	M2	G5	PA53	I/O	0	GPIO_A53
						2	QSPI2_DIO5
						3	SPI1_CS
						4	UART1_TXD
						10	GPTIM2_CH2
						Others	Reserved
-	J5	J5	K4	PA54	I/O	0	GPIO_A54
						2	QSPI2_DIO6
						3	SPI1_DI
						4	UART1_RXD
						10	GPTIM2_CH3
						Others	Reserved
18	H5	H5	J4	PA55	I/O	0	GPIO_A55
						1	QSPI3_DIO3
						2	QSPI2_DIO7
						6	SD2_DIO3
						7	SD1_DIO7
						8	LCDC1_8080_DIO7
						11	LCDC1_JDI_G1
						Others	Reserved
-	K4	K4	L3	PA56	I/O	0	GPIO_A56
						2	QSPI2_DIO7
						3	SPI1_DO
						4	SPI1_DIO
						10	GPTIM2_CH4
						Others	Reserved
-	L3	L3	N3	PA57	I/O	0	GPIO_A57
						3	I2C3_SDA
						10	GPTIM2_ETR
						Others	Reserved
17	M1	M1	L2	PA58	I/O	0	GPIO_A58
						4	LPTIM1_ETR
						Others	Reserved

Continued on the next page

Table 5-3: GPIO (PA) Pin List (continued)

Pin Number				Pin Name	Type	Sel #	Function
SF32LB551 QFN68L	SF32LB553 BGA125	SF32LB555 BGA145	SF32LB557 BGA169				
-	-	-	N2	PA59	I/O	0	GPIO_A59
						2	PSRAM_DQ13
						5	SD2_CMD
						7	LCDC1_SPI_DIO3
						9	LCDC1_DPI_HSYNC
						Others	Reserved
16	L2	L2	M2	PA60	I/O	0	GPIO_A60
						1	QSPI2_CLK
						6	SD1_CLK
						Others	Reserved
15	L1	L1	N1	PA61	I/O	0	GPIO_A61
						1	QSPI2_CS
						6	SD1_CMD
						Others	Reserved
-	-	-	M1	PA62	I/O	0	GPIO_A62
						2	PSRAM_DQ14
						5	SD2_DIO1
						6	SD1_DIO4
						9	LCDC1_DPI_VSYNC
						Others	Reserved
14	H1	H1	H4	PA63	I/O	0	GPIO_A63
						1	QSPI2_DIO0
						3	SPI2_CS
						6	SD1_DIO0
						10	GPTIM1_ETR
						Others	Reserved
-	-	-	H1	PA64	I/O	0	GPIO_A64
						2	PSRAM_DQ15
						5	SD2_DIO3
						6	SD1_DIO5
						9	LCDC1_DPI_SD
						Others	Reserved
13	G2	G2	G4	PA65	I/O	0	GPIO_A65
						1	QSPI2_DIO1
						3	SPI2_DI
						6	SD1_DIO1
						10	GPTIM1_CH1
						Others	Reserved

Continued on the next page

Table 5-3: GPIO (PA) Pin List (continued)

Pin Number				Pin Name	Type	Sel #	Function
SF32LB551 QFN68L	SF32LB553 BGA125	SF32LB555 BGA145	SF32LB557 BGA169				
12	G1	G1	F4	PA66	I/O	0	GPIO_A66
						1	QSPI2_DIO2
						3	SPI2_DO
						4	SPI2_DIO
						6	SD1_DIO2
						10	GPTIM1_CH2
						Others	Reserved
-	-	-	G3	PA67	I/O	0	GPIO_A67
						9	LCDC1_DPI_CM
						Others	Reserved
11	F4	F4	G1	PA68	I/O	0	GPIO_A68
						1	QSPI2_DIO3
						6	SD1_DIO3
						10	GPTIM1_CH3
						Others	Reserved
-	-	-	-	PA69	I/O	0	GPIO_A69
						Others	Reserved
10	F3	F3	G2	PA70	I/O	0	GPIO_A70
						2	PSRAM_CLKB
						4	PDM1_DATA
						5	I2S1_SDI
						10	GPTIM1_CH4
						Others	Reserved
-	-	-	-	PA71	I/O	0	GPIO_A71
						Others	Reserved
-	-	-	-	PA72	I/O	0	GPIO_A72
						Others	Reserved
-	-	-	-	PA73	I/O	0	GPIO_A73
						Others	Reserved
-	-	-	-	PA74	I/O	0	GPIO_A74
						Others	Reserved
-	-	-	-	PA75	I/O	0	GPIO_A75
						Others	Reserved
-	-	-	-	PA76	I/O	0	GPIO_A76
						Others	Reserved

Continued on the next page

Table 5-3: GPIO (PA) Pin List (continued)

Pin Number				Pin Name	Type	Sel #	Function
SF32LB551 QFN68L	SF32LB553 BGA125	SF32LB555 BGA145	SF32LB557 BGA169				
8	F2	F2	F3	PA77	I/O	0	GPIO_A77
						1	#WKUP_A0
						3	I2C3_SCL
						4	SPI2_CLK
						7	LCDC1_SPI_TE
						8	LCDC1_8080_TE
						10	GPTIM2_ETR
						11	LCDC1_JDI_G2
						Others	Reserved
7	E2	E2	E3	PA78	I/O	0	GPIO_A78
						1	#WKUP_A1
						3	I2C3_SDA
						4	SPI2_CS
						7	LCDC1_SPI_RSTB
						8	LCDC1_8080_RSTB
						10	GPTIM2_CH1
						11	LCDC1_JDI_B1
						Others	Reserved
6	D2	D2	E4	PA79	I/O	0	GPIO_A79
						1	#WKUP_A2
						3	I2C2_SCL
						4	SPI2_DO
						5	SPI2_DIO
						10	GPTIM2_CH2
						11	LCDC1_JDI_B2
						Others	Reserved
5	C2	C2	E5	PA80	I/O	0	GPIO_A80
						1	#WKUP_A3
						3	I2C2_SDA
						10	GPTIM2_CH3
						Others	Reserved

Notes:

- PA77-80 (WKUP_A0-3) is used for the key wakeup in HPSYS low-power mode, which can wake up HCPU directly.
- When the system is in Hibernate, PA77-80 **cannot** be used for Boot wakeup.

5.2.2 LITTLE Core Domain GPIO (PB) List

Table 5-4: GPIO (PB) Pin List

Pin Number				Pin Name	Type	Sel #	Function
SF32LB551 QFN68L	SF32LB553 BGA125	SF32LB555 BGA145	SF32LB557 BGA169				
-	-	-	-	PB00	I/O	0	GPIO_B0
						4	SPI4_CLK
						7	QSPI4_CLK
						Others	Reserved
36	K11	K11	-	PB01	I/O	0	GPIO_B1
						4	SPI4_CS
						5	LPTIM3_IN
						7	QSPI4_CS
						10	#LPCOMP1_P
						Others	Reserved
-	-	-	-	PB02	I/O	0	GPIO_B2
						4	SPI4_DI
						7	QSPI4_DIO0
						Others	Reserved
37	L13	L13	-	PB03	I/O	0	GPIO_B3
						1	GPTIM4_CH1
						4	SPI4_DO
						5	SPI4_DIO
						7	QSPI4_DIO1
						10	#LPCOMP1_N
						Others	Reserved
38	K12	K12	G9	PB04	I/O	0	GPIO_B4
						1	GPTIM4_CH2
						2	I2C4_SCL
						10	#LPCOMP2_P
						Others	Reserved
39	J11	J11	F8	PB05	I/O	0	GPIO_B5
						1	GPTIM4_CH3
						2	I2C4_SDA
						10	#LPCOMP2_N/ATEST
						Others	Reserved
-	H10	H10	F9	PB06	I/O	0	GPIO_B6
						3	UART5_TXD
						4	SPI3_DI
						Others	Reserved
-	-	H9	-	PB07	I/O	0	GPIO_B7
						3	UART5_RXD
						6	LCDC2_SPI_DIO3
						7	QSPI4_DIO3
						Others	Reserved

Continued on the next page

Table 5-4: GPIO (PB) Pin List (continued)

Pin Number				Pin Name	Type	Sel #	Function
SF32LB551 QFN68L	SF32LB553 BGA125	SF32LB555 BGA145	SF32LB557 BGA169				
40	J12	J12	D9	PB08	I/O	0	GPIO_B8
						1	GPTIM4_ETR
						4	SPI3_DO
						5	SPI3_DIO
						10	#GPADC_CH0
						Others	Reserved
-	H11	H11	G10	PB09	I/O	0	GPIO_B9
						1	GPTIM5_CH1
						3	UART3_CTS
						Others	Reserved
41	G11	G11	E10	PB10	I/O	0	GPIO_B10
						2	I2C4_SDA
						5	LPTIM3_OUT
						10	#GPADC_CH1
						Others	Reserved
-	F11	F11	C10	PB11	I/O	0	GPIO_B11
						2	I2C4_SCL
						3	UART5_RXD
						5	LPTIM3_ETR
						Others	Reserved
-	F9	F9	K13	PB12	I/O	0	GPIO_B12
						1	GPTIM3_CH1
						3	UART4_TXD
						4	SPI3_CLK
						10	#GPADC_CH2
						Others	Reserved
42	E9	E9	J11	PB13	I/O	0	GPIO_B13
						1	GPTIM3_CH2
						4	SPI3_CLK
						10	#GPADC_CH3
						Others	Reserved
-	D8	D8	D10	PB14	I/O	0	GPIO_B14
						1	GPTIM3_CH3
						3	UART4_RXD
						4	SPI3_CS
						Others	Reserved
-	C8	C8	F11	PB15	I/O	0	GPIO_B15
						1	GPTIM3_CH4
						3	UART4_CTS
						Others	Reserved

Continued on the next page

Table 5-4: GPIO (PB) Pin List (continued)

Pin Number				Pin Name	Type	Sel #	Function
SF32LB551 QFN68L	SF32LB553 BGA125	SF32LB555 BGA145	SF32LB557 BGA169				
43	D9	D9	G11	PB16	I/O	0	GPIO_B16
						3	UART3_RTS
						4	SPI3_DO
						5	SPI3_DIO
						10	#GPADC_CH4
						Others	Reserved
-	-	F10	J12	PB17	I/O	0	GPIO_B17
						1	GPTIM5_CH2
						3	UART5_RTS
						6	LCDC2_SPI_RSTB
						10	#GPADC_CH5
						Others	Reserved
-	-	E10	J13	PB18	I/O	0	GPIO_B18
						3	UART5_CTS
						6	LCDC2_SPI_TE
						10	#GPADC_CH6
						Others	Reserved
44	C9	C9	F10	PB19	I/O	0	GPIO_B19
						1	GPTIM5_ETR
						4	SPI3_DI
						10	#GPADC_CH7
						Others	Reserved
-	-	-	E11	PB20	I/O	0	GPIO_B20
						1	GPTIM3_ETR
						Others	Reserved
-	-	-	-	PB21	I/O	0	GPIO_B21
						1	GPTIM4_CH4
						7	QSPI4_DIO2
						Others	Reserved
-	D10	D10	C11	PB22	I/O	0	GPIO_B22
						3	UART4_RTS
						Others	Reserved
45	C10	C10	H12	PB23	I/O	0	GPIO_B23
						1	GPTIM5_CH1
						4	SPI3_CS
						10	#SDADC_CH0
						Others	Reserved
46	B12	B12	B12	PB24	I/O	0	GPIO_B24
						1	GPTIM5_CH2
						5	LPCOMP1_OUT
						10	#SDADC_CH1/ACTEST_P
						Others	Reserved

Continued on the next page

Table 5-4: GPIO (PB) Pin List (continued)

Pin Number				Pin Name	Type	Sel #	Function
SF32LB551 QFN68L	SF32LB553 BGA125	SF32LB555 BGA145	SF32LB557 BGA169				
47	A12	A12	A12	PB25	I/O	0	GPIO_B25
						1	GPTIM5_CH3
						5	LPCOMP2_OUT
						10	#SDADC_CH2/ACTEST_N
						Others	Reserved
-	A13	A13	A13	PB26	I/O	0	GPIO_B26
						1	GPTIM5_CH4
						3	UART5_CTS
						10	#SDADC_CH3
						Others	Reserved
-	B13	B13	B13	PB27	I/O	0	GPIO_B27
						3	UART5_RTS
						Others	Reserved
-	B10	B10	B9	PB28	I/O	0	GPIO_B28
						3	UART3_CTS
						Others	Reserved
54	A11	A11	C9	PB29	I/O	0	GPIO_B29
						2	I2C6_SCL
						3	UART3_RTS
						Others	Reserved
-	B11	B11	D8	PB30	I/O	0	GPIO_B30
						2	I2C6_SDA
						Others	Reserved
55	C11	C11	C8	PB31	I/O	0	SWCLK
						1	GPIO_B31
						3	UART3_TXD
						Others	Reserved
-	-	E8	B8	PB32	I/O	0	GPIO_B32
						4	SPI4_CLK
						6	LCDC2_SPI_CLK
						7	QSPI4_CLK
						Others	Reserved
-	-	C7	A8	PB33	I/O	0	GPIO_B33
						4	SPI4_CS
						6	LCDC2_SPI_CS
						7	QSPI4_CS
						Others	Reserved
56	B6	B6	C7	PB34	I/O	0	SWDIO
						1	GPIO_B34
						3	UART3_RXD
						Others	Reserved

Continued on the next page

Table 5-4: GPIO (PB) Pin List (continued)

Pin Number				Pin Name	Type	Sel #	Function
SF32LB551 QFN68L	SF32LB553 BGA125	SF32LB555 BGA145	SF32LB557 BGA169				
-	-	E6	E8	PB35	I/O	0	GPIO_B35
						4	SPI4_DI
						6	LCDC2_SPI_DIO0
						7	QSPI4_DIO0
						Others	Reserved
-	-	D6	D7	PB36	I/O	0	GPIO_B36
						4	SPI4_DO
						5	SPI4_DIO
						6	LCDC2_SPI_DIO1
						7	QSPI4_DIO1
						Others	Reserved
-	-	E5	E7	PB37	I/O	0	GPIO_B37
						3	UART5_TXD
						6	LCDC2_SPI_DIO2
						7	QSPI4_DIO2
						Others	Reserved
-	-	-	B5	PB38	I/O	0	GPIO_B38
						Others	Reserved
-	-	-	B7	PB39	I/O	0	GPIO_B39
						2	I2C5_SCL
						3	UART4_TXD
						Others	Reserved
-	-	-	D4	PB40	I/O	0	GPIO_B40
						2	I2C5_SDA
						3	UART4_RXD
						Others	Reserved
-	-	-	C4	PB41	I/O	0	GPIO_B41
						7	QSPI4_DIO3
						Others	Reserved
-	-	-	-	PB42	I/O	0	GPIO_B42
						1	GPTIM5_ETR
						Others	Reserved
57	C6	C6	B6	PB43	I/O	0	GPIO_B43
						1	GPTIM5_CH3
						2	I2C5_SCL
						10	#WKUP_B0
						Others	Reserved
58	D5	D5	C6	PB44	I/O	0	GPIO_B44
						1	GPTIM5_CH4
						2	I2C5_SDA
						10	#WKUP_B1
						Others	Reserved

Continued on the next page

Table 5-4: GPIO (PB) Pin List (continued)

Pin Number				Pin Name	Type	Sel #	Function
SF32LB551 QFN68L	SF32LB553 BGA125	SF32LB555 BGA145	SF32LB557 BGA169				
59	C5	C5	E6	PB45	I/O	0	GPIO_B45
						2	I2C6_SCL
						3	UART3_TXD
						10	#WKUP_B2
						Others	Reserved
60	F5	F5	D6	PB46	I/O	0	GPIO_B46
						2	I2C6_SDA
						3	UART3_RXD
						10	#WKUP_B3
						Others	Reserved
61	E4	E4	D5	PB47	I/O	0	GPIO_B47
						3	UART3_CTS
						10	#WKUP_B4
						Others	Reserved
62	D4	D4	C5	PB48	I/O	0	GPIO_B48
						3	UART3_RTS
						10	#WKUP_B5
						Others	Reserved

Notes:

- PB43-48(WKUP_B0-5) is used for the key wakeup in LPSYS low-power mode, which can wake up LCPU directly.
- When the system is in Hibernate,PB43-48 **can** be used for Boot wakeup.

5.2.3 List of Dedicated Pins (Power, RF, Analog, I/O)

Table 5-5: List of Dedicated Pins (Power, RF, Analog, I/O)

Pin Number				Pin Name	Type	Description
SF32LB551 QFN68L	SF32LB553 BGA125	SF32LB555 BGA145	SF32LB557 BGA169			
		J4		AVDD_DSI	PWR	MIPI DSI power input
		H4		AVSS_DSI	GND	MIPI DSI ground
		K3		DSI_DN0	A,I/O	MIPI DSI data channel 0-
		K2		DSI_DP0	A,I/O	MIPI DSI data channel 0+
		J3		DSI_CLKN	A,I/O	MIPI DSI clock signal -
		J2		DSI_CLKP	A,I/O	MIPI DSI clock signal +
		H3		DSI_DN1	A,I/O	MIPI DSI data channel 1-
		H2		DSI_DP1	A,I/O	MIPI DSI data channel 1+
		G3		DSI_REXT	A,I/O	MIPI DSI external resistance
67	A2	A2		VDD1	PWR	BUCK1 power input
	C3	C3		PVSS1	GND	BUCK1 ground
2	C1	C1		BUCK1_VOUT	PWR	BUCK1 output

Continued on the next page

Table 5-5: List of Dedicated Pins (Power, RF, Analog, I/O) (continued)

Pin Number				Pin Name	Type	Description
SF32LB551 QFN68L	SF32LB553 BGA125	SF32LB555 BGA145	SF32LB557 BGA169			
1	B1	B1		BUCK1_VSW	PWR	BUCK1 inductive switch
	B2	B2		VDD2	PWR	BUCK2 power input
	C4	C4		PVSS2	GND	BUCK2 ground
	B3	B3		BUCK2_VOUT	PWR	BUCK2 output
	A3	A3		BUCK2_VSW	PWR	BUCK2 inductive switch
9	F1	F1		VDD_SIP	PWR	Built-in memory chip power input
64	B5	B5		VDD_RET	PWR	RET LDO output
63	A6	A6		VDD_RTC	PWR	RTC LDO output
4	E1	E1		LDO_VOUT1	PWR	LDO1 output
3	D1	D1		LDO_VOUT2	PWR	LDO2 output
	B4	B4		LDOVCC2_VOUT	PWR	LDO2 mode output
50	E12	E12		AVDD_BRF	PWR	RF power supply
49	F12	F12		AVDD33	PWR	3.3V analog power input
	G12	G12		AVSS33	GND	3.3V analog ground
23	N6	N6		VDDIOA	PWR	GPIOA power supply
48	H12	H12		VDDIOB	PWR	GPIOB power supply
	B8	B8		AVSS1	GND	Analog ground
	C12	C12		AVSS2	GND	Analog ground
	D12	D12		AVSS3	GND	Analog ground
	C13	C13		AVSS4	GND	Analog ground
	E13	E13		AVSS5	GND	Analog ground
	F6	F6		VSS	GND	Ground
	F7	F7		VSS	GND	Ground
	F8	F8		VSS	GND	Ground
	G6	G6		VSS	GND	Ground
	G7	G7		VSS	GND	Ground
	G8	G8		VSS	GND	Ground
	H7	H7		VSS	GND	Ground
68	A1	A1		RSTN	I	Reset
31	H8	H8		MODE	I	Start mode
	F13	F13		SDMADC_VREF	A,I	SDMADC external reference source input
	G13	G13		SDMADC_VIN	A,I	SDMADC independent input
	H13	H13		SDMADC_GND	GND	SDMADC independent ground
66	B7	B7		XTAL32K_XO	A,I/O	32KHz crystal interface
65	A7	A7		XTAL32K_XI	A,I/O	32KHz crystal interface
53	A8	A8		XTAL48M_XI	A,I/O	48MHz crystal interface
52	B9	B9		XTAL48M_XO	A,I/O	48MHz crystal interface
51	D13	D13		ANT	A,I/O	Antenna interface

5.3 Ordering Information

Table 5-6: Ordering Information

Part No.	Package Size	SiP Specification	Quantity (PCS)
SF32LB551U4O5	QFN68L: 7×7×0.75mm-0.35	32Mb PSRAM + 32Mb NOR Flash	3000
SF32LB555V4O6	BGA145: 7×7×0.94mm-0.5	32Mb PSRAM + 32Mb NOR Flash	3000
SF32LB555V436	BGA145: 7×7×0.94mm-0.5	64Mb PSRAM + 32Mb NOR Flash	3000
SF32LB557VD3A6	BGA169: 7×7×0.94mm-0.5	128Mb PSRAM + 8Mb NOR Flash + 16Mb PSRAM	3000

Address: 419-13, Block B, Science and Technology Headquarters Building, No.320 Pubin Road, Nanjing Area, Jiangsu Free Trade Zone, P. R. China 200131
Email: sales@sifli.com