SF32LB52x

Datasheet

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SiFli Technologies (Nanjing) Co., Ltd.
http://www.sifli.com

Revision History

Document Status

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Revision History

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Overview

SF32LB52x is a family of highly integrated high-performance MCUs desgined for ultra-low power Artifical Intelligence of Things (AIoT) scenarios. SF32LB52x adopts the big.LITTLE architecture with Arm Cortex-M33 STAR-MC1 processors, and is embedded with 2D/2.5D GPU, dual-mode BT5.3, and audio codec. SF32LB52x can be used for a wide variety of applications such as wearables, smart HMI devices, and smart homes.

The high-performance processor ("big core") of SF32LB52x can operate at up to 240MHz for 984 CoreMark. It supports dynamic frequency power adjustment, can also serve as sensor hub and Bluetooth controller at high power efficiency of 4.8uA/CoreMark, thus delivering no-compromise user experience of both high computational performance required for feature-rich graphical HMI (Human Machine Interface) and ultra-low power sensor hub operation.

The 2D/2.5D GPU, at up to 240MHz, supports 2-layer alpha blending, hardware accelerated rotation and scaling, and conversion of common graphic formats. eZip™2.0 supports lossless compressed graphics file, saving memory bandwidth and storage capacity. The LCD controller can support interfaces of 8080/QSPI at a full-screen refresh frame rate up to 60fps, and support Always-On Display.

The dual-mode BT5.3 transceiver has a maximum Tx power of 13dBm at EDR2 mode and Rx power of 2.4mA@3.8V, and the sensitivity reaches -100dBm (1Mbps) for BLE and -95.5dBm for EDR2. SF32LB52x is embedded with high-fidelity audio ADC/DAC, supporting Bluetooth call and connecting headphones for MP3 playback.

Functional Block Diagram

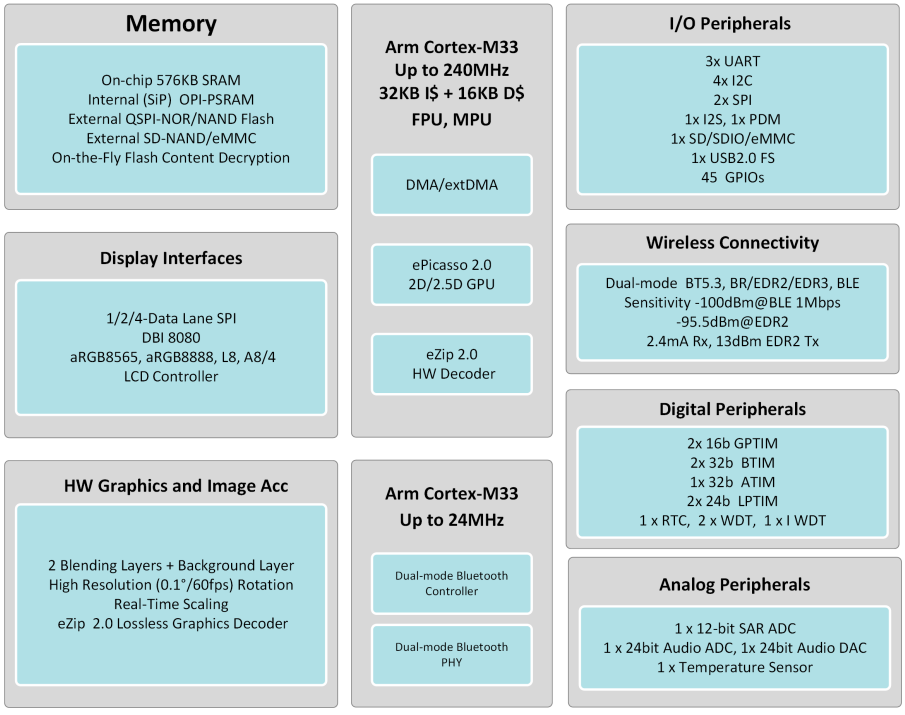

Figure 0-1: Functional Block Diagram

Features

CPU and Memory

- High Performance Processor (HCPU)
  - Arm Cortex-M33 STAR-MC1
  - Up to 240MHz clock frequency, adjustable
  - Up to 370DMIPS, 984 EEMBC CoreMark
  - I-Cache + D-Cache: 32KB(2-way)+16KB(4-way)
  - SRAM: 512KB (All Retention SRAM)
  - CoreMark power: 23uA/MHz @3.8V
  - Single Precision Floating Point Unit (FPU)
  - Memory Protection Unit (MPU)
- Ultra Low-Power Processor (LCPU)
  - Arm Cortex-M33 STAR-MC1
  - Up to 24MHz clock frequency, adjustable
  - SRAM: 64KB (All Retention SRAM)

Wireless Connectivity

- Dual-mode BT5.3, support BLE Audio
- Sensitivity: -100dBm(BLE/1Mbps), -96.3dBm(BR), -95.5dBm(EDR2)
- Max. Tx power: 13dBm（EDR2/3）, 19dBm（BR/BLE）
- Rx peak current (BR): 2.4mA@3.8V

Audio

- 1×HiFi 24-bit Audio DAC
  - Noise floor: 3.7uVrms
  - SNR(with 10kohm load and A-Weighted): 109dB, Dynamic Range: 109dB
  - Sample rate: 8k/ 16k/ 11.025k/ 22.05k/ 24k/ 32k/ 44.1k/ 48kHz
  - Support digital volume of 192 steps with zero-crossing detection
- 1×HiFi 24-bit Audio ADC
  - SNR(A-Weighted): 99dB, Dynamic Range: 99dB
  - Sample rate: 8k/ 11.025k/ 12k/ 16k/ 22.05k/ 24k/ 32k/ 44.1k/ 48kHz
  - A digital high-pass filter can be used to remove dc offsets of ADC
  - Support single-ended and fully differential input microphones
  - Micbias LDO with 1.4V~2.8V output voltage and 0~2mA output current

Graphics and Display

- 2D/2.5D GPU—ePicasso™2.0
  - Hardware-accelerated rotation, scaling, and mirroring
  - Max. resolution: 512×512
  - Support aRGB8565, aRGB8888, L8, A8/4/2,YUV, support alpha blending
- Lossless Decompression Accelerator – eZip™2.0
  - Lossless graphics decompression
  - support native animation eZip-A
  - Concatenated operation with ePicasso™2.0
- LCD Controller
  - Support 8080, SPI, Dual-SPI, Quad-SPI
  - 1 layer + 1 background layer alpha blending
  - Independent LCD controller, Always-On Display

Memory Interface

- Support（SiP）NOR-Flash, interface frequency up to 96MHz
- Support（SiP）OPI-PSRAM, interface frequency up to 144MHz
- 1×MPI(QSPI), support NOR, NAND, QPI-PSRAM
- 1×SD/SDIO, support SD3.0, SDIO3.0, eMMC

DMA

- General DMA: high efficiency data transfer between internal memory and peripherals
- extDMA: high efficiency data transfer between internal memory and external memory

Security

- AES,HASH and CRC hardware accelerators
- True random number generator (TRNG)
- PSA Certified Level 1

Timers

- 2×16b GPTIM, 2×32b BTIM, 1×32b ATIM, 2×24b LPTIM
- 1×RTC
- 2×24b WDT, 1×IWDT

Analog Peripherals

- 1×12-bit general purpose SAR ADC, 8 channels
- 1×Temperature sensor
- 1×24-bit audio ADC, 1×24-bit audio DAC

I/O Peripherals

- Up to 45 GPIOs
- 3×UART, 4× I^2C, 2×SPI
- 1× I^2S, 1× PDM
- 1×USB2.0 FS
- Peripheral Task Controller (PTC)

Power Management

- High-efficiency buck and low-power LDO
- 2 external 3.3V power supply LDOs, Max. current 150mA×2
- Sleep current: 2uA
- Built-in 560mA lithium battery linear charger, supporting 4.2V-4.45V full voltage
- VBAT voltage range: 3.2V-4.7V
- VBUS voltage range: 4.6V-5.5V

Others

- Operating Temperature Range: -40~85°C
- Package: QFN68L, 44 GPIOs, 7×7×0.85mm

Applications

Smart Wearable

- Smart watch
- Smart wristband
- Wearable medical device
- Fitness equipment

Industrial Device

- Cost-effective display solution
- Graphical Human-Machine Interface (HMI) device
- Industrial sensor hub
- Industrial equipment monitoring
- Industrial instrumentation

Vehicle Device

- Electric vehicle control center
- Car key
- Wearable car remote controls

Home Automation

- Smart home appliance
- Smart door lock

Generic Scenario

- Low-power sensor hub
- Bluetooth mesh

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1 Introduction

1.1 System Architecture

SF32LB52x is a family of highly integrated high-performance MCUs desgined for ultra-low-power Artifical Intelligence of Things (AIoT) scenarios. SF32LB52x adopts the big.LITTLE architecture with the Arm Cortex-M33 STAR-MC1 processor.

- High-Performance Processor/Big Core (HCPU): 32KB instruction cache (I-Cache) and 16KB data cache (D-Cache), 512KB SRAM (All Retention SRAM); Up to 240MHz clock frequency, it can dynamically switch between basic-working mode and enhance-working mode for efficient access to on-chip and off-chip memory. As the system master, enhance-working mode is mainly used for system control, Human-Machine Interaction, and high-performance computing; Meanwhile, as the low-power sensor hub, basic-working mode can be used for all kinds of data acquisition and processing in low-power scenarios.
- Ultra-low Power Processor/LITTLE Core (LCPU): Up to 24MHz clock frequency, 64KB SRAM (all Retention SRAM); it is mainly used for transmission control and basic data processing of Bluetooth Low Energy.

1.2 Cortex-M33 STAR-MC1 Processor

Cortex-M33 STAR-MC1 processor is the first processor of the “Star” series from Arm China. It has the key features of Cortex-M33, supporting the full functionality of the existing Arm v8-M architecture, and with an in-order three-stage pipeline, it can significantly reduce the power consumption of the system. It also has partial dual-issue 16-bit instruction capability, the coprocessor interface is further improved and support the Cache.

With the performance reaching 1.5DMIPS/MHz and 4.02Coremark/MHz, Cortex-M33 STAR-MC1 delivers a 20% performance improvement over previous-generation Arm processors at the same clock speed.

Cortex-M33 STAR-MC1 has a coprocessor interface which can further enhance the capability of customized calculation to meet the requirements of different scenarios. The MCR (Move from Coprocessor to Register) and MRC (Move from Register to Coprocessor) instructions enable the transfer of register data and computation results between Cortex-M33 STAR-MC1 and the coprocessor, making it ideal for operations with small data volumes, complex calculations but relatively fragmented and low latency. While the coprocessor computes, Cortex-M33 STAR-MC1 processor can still execute other instructions in parallel, thus significantly improving execution efficiency.

In addition, the processor supports Digital Signal Processing (DSP) instruction sets and Floating Point Unit (FPU).

Tightly Coupled Memory (TCM) and Cache technologies are adopted in Cortex-M33 STAR-MC1 processor to enhance flexibility in the use of internal and external memory systems with different characteristics, ensuring the real-time response and computational efficiency of the processor in a variety of scenarios.

1.3 High-Performance Processor (Big Core) System (HPSYS)

1.3.1 Bus Architecture

The HPSYS provides an internal bus matrix based on the AHB protocol, which supports multiple master devices to access the address spaces of multiple slave devices in parallel.

As shown in Figure 1-1, the master devices of the bus are located on the top side and the address spaces of the slave devices are located on the right side, and the black dots at the intersection represent bus connectivity.

The HCPU and DMAC1 has access to all address spaces of the HPSYS.

128KB address space is shared between DTCM and HPSYS_RAM0, and can be accessed by the HCPU and other master devices.

HP_PERI includes APB-related peripherals and AHB-related peripherals, and can be accessed by HCPU, DMAC1 and PTC1.

When multiple master devices access the address space of the same slave device at the same time, the access order will be determined based on the Round-Robin Arbitration Principle.

As shown in the figure, when multiple master devices with unconnected borders access the address spaces of different slave devices at the same time, they will not be affected by each other. When two master devices with connected borders initiate access at the same time, the access order will be decided based on the polling arbitration principle.

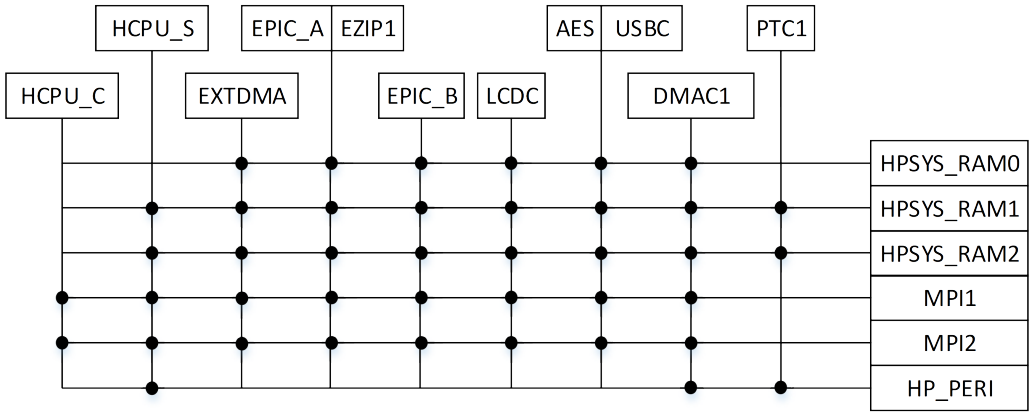


Figure 1-1: Bus Architecture of HPSYS

1.3.2 Clock Architecture

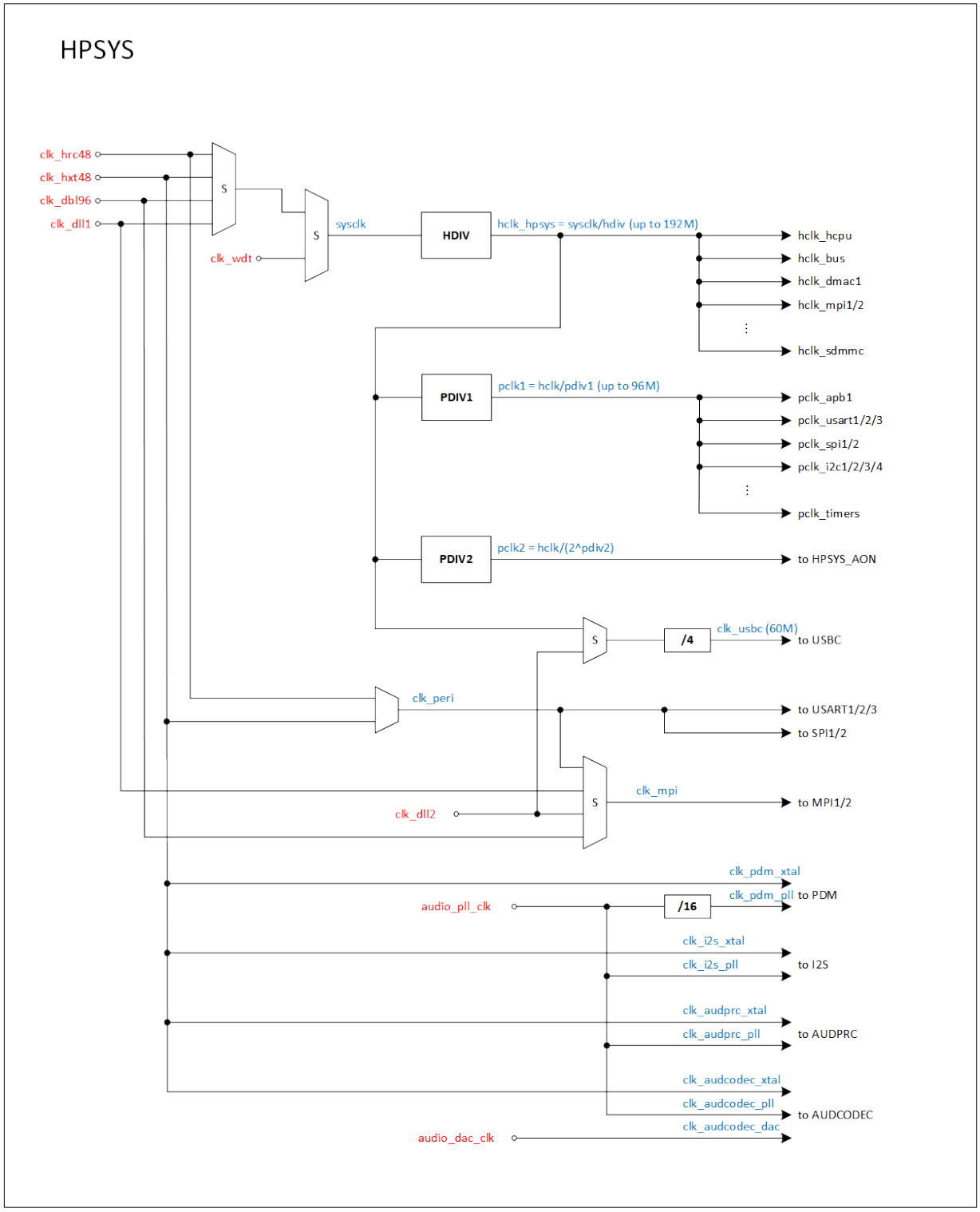


Figure 1-2: Clock Architecture of HPSYS

1.3.3 Memory Type

1.3.3.1 Cache

The HCPU has 32KB 2-way I-Cache (Level 1 instruction cache) and 16KB 4-way D-Cache (Level 1 data cache), which can greatly improve CPU execution efficiency during XIP. The MPU (Memory Protection Unit) should be configured appropriately to set the cache address segment and non-cache address segment to balance efficiency and ease of use.

1.3.3.2 TCM

The HCPU has 128KB zero-wait-cycle D-TCM with address space 0x2000_0000-0x2001_FFFF, which can be used to place codes and data with high real-time requirements. This TCM memory is connected to the bus and can be accessed by other AHB masters.

1.3.3.3 SRAM

There is a total of 512KB SRAM on the HPSYS bus, which includes:

- 0x2000_0000-0x2001_FFFF, 128KB zero-wait-cycle SRAM (shared with D-TCM), accessible to all AHB masters. Maximum frequency is 240MHz.
- 0x2002_0000-0x2007_FFFF, 384KB zero-wait-cycle SRAM, accessible to all AHB masters. Maximum frequency is 240MHz.

1.3.3.4 Off-chip RAM

The HPSYS supports combined 4-wire and 8-wire pSRAM with address space 0x6000_0000 - 0x61FF_FFFF, the actual accessible address is determined by the capacity of the external particles. The maximum interface frequency is DDR 144MHz and the data bit width is 8-bit.

1.3.3.5 Off-chip Flash

The HPSYS supports external NOR/NAND FLASHs, in which

- 0x6000_0000–0x61FF_FFFF address segment can be combined with FLASH, recommended frequency is 96MHz
- 0x6200_0000–0x9FFF_FFFF address segment can be connected to external FLASH, recommended frequency is 60MHz

1.3.4 Address Mapping

Table 1-1: Address Mapping of HPSYS

Category	Memory /IP	Address Space	HCPU				LCPU	
			Starting Address		Ending Address		Starting Address	Ending Address
HPSYS_ITCM		**64KB**	**0x0000_0000**		**0x0000_FFFF**		**NA**	**NA**
	ROM	64KB	0x0000_0000		0x0000_FFFF		-	-
	Reserved	-	-		-		-	-
External Memory		**1024MB**	**0x1000_0000**	**0x6000_0000**	**0x1FFF_FFFF**	**0x9FFF_FFFF**	**0x6000_0000**	**0x9FFF_FFFF**
	MPI1 Memory	32MB	0x1000_0000	0x6000_0000	0x11FF_FFFF	0x61FF_FFFF	0x6000_0000	0x61FF_FFFF
	MPI2 Memory	224MB/992MB	0x1200_0000	0x6200_0000	0x1FFF_FFFF	0x9FFF_FFFF	0x6200_0000	0x9FFF_FFFF
HPSYS_RAM		**512KB**	**0x2000_0000**		**0x2007_FFFF**		**0x2A00_0000**	**0x2A07_FFFF**
	RAM0 (DTCM)	128KB	0x2000_0000		0x2001_FFFF		0x2A00_0000	0x2A01_FFFF
	RAM1	128KB	0x2002_0000		0x2003_FFFF		0x2A02_0000	0x2A03_FFFF
	RAM2	256KB	0x2004_0000		0x2007_FFFF		0x2A04_0000	0x2A07_FFFF
HPSYS_APB1		**256KB**	**0x5000_0000**		**0x5003_FFFF**		**0x5000_0000**	**0x5003_FFFF**

Continued on the next page

Table 1-1: Address Mapping of HPSYS (continued)

Category	Memory /IP	Address Space	HCPU		LCPU	
			Starting Address	Ending Address	Starting Address	Ending Address
	RCC1	4KB	0x5000_0000	0x5000_0FFF	0x5000_0000	0x5000_0FFF
	EXTDMA	4KB	0x5000_1000	0x5000_1FFF	0x5000_1000	0x5000_1FFF
	SECU1	4KB	0x5000_2000	0x5000_2FFF	0x5000_2000	0x5000_2FFF
	PINMUX1	4KB	0x5000_3000	0x5000_3FFF	0x5000_3000	0x5000_3FFF
	ATIM1	4KB	0x5000_4000	0x5000_4FFF	0x5000_4000	0x5000_4FFF
	AUDPRC	4KB	0x5000_5000	0x5000_5FFF	0x5000_5000	0x5000_5FFF
	EZIP1	4KB	0x5000_6000	0x5000_6FFF	0x5000_6000	0x5000_6FFF
	EPIC	4KB	0x5000_7000	0x5000_7FFF	0x5000_7000	0x5000_7FFF
	LCDC1	4KB	0x5000_8000	0x5000_8FFF	0x5000_8000	0x5000_8FFF
	I2S1	4KB	0x5000_9000	0x5000_9FFF	0x5000_9000	0x5000_9FFF
	Reserved	4KB	0x5000_A000	0x5000_AFFF	0x5000_A000	0x5000_AFFF
	SYSCFG1	4KB	0x5000_B000	0x5000_BFFF	0x5000_B000	0x5000_BFFF
	EFUSEC	4KB	0x5000_C000	0x5000_CFFF	0x5000_C000	0x5000_CFFF
	AES	4KB	0x5000_D000	0x5000_DFFF	0x5000_D000	0x5000_DFFF
	Reserved	4KB	0x5000_E000	0x5000_EFFF	0x5000_E000	0x5000_EFFF
	TRNG	4KB	0x5000_F000	0x5000_FFFF	0x5000_F000	0x5000_FFFF
	Reserved	4KB	0x5001_0000	0x5001_0FFF	0x5001_0000	0x5001_0FFF
	Reserved	4KB	0x5001_1000	0x5001_1FFF	0x5001_1000	0x5001_1FFF
	Reserved	4KB	0x5001_2000	0x5001_2FFF	0x5001_2000	0x5001_2FFF
	Reserved	4KB	0x5001_3000	0x5001_3FFF	0x5001_3000	0x5001_3FFF
	Reserved	4KB	0x5001_4000	0x5001_4FFF	0x5001_4000	0x5001_4FFF
	Reserved	4KB	0x5001_5000	0x5001_5FFF	0x5001_5000	0x5001_5FFF
	Reserved	4KB	0x5001_6000	0x5001_6FFF	0x5001_6000	0x5001_6FFF
	Reserved	4KB	0x5001_7000	0x5001_7FFF	0x5001_7000	0x5001_7FFF
	Reserved	4KB	0x5001_8000	0x5001_8FFF	0x5001_8000	0x5001_8FFF
	Reserved	4KB	0x5001_9000	0x5001_9FFF	0x5001_9000	0x5001_9FFF
	Reserved	4KB	0x5001_A000	0x5001_AFFF	0x5001_A000	0x5001_AFFF
	Reserved	4KB	0x5001_B000	0x5001_BFFF	0x5001_B000	0x5001_BFFF
	Reserved	4KB	0x5001_C000	0x5001_CFFF	0x5001_C000	0x5001_CFFF
	Reserved	4KB	0x5001_D000	0x5001_DFFF	0x5001_D000	0x5001_DFFF
	Reserved	4KB	0x5001_E000	0x5001_EFFF	0x5001_E000	0x5001_EFFF
	Reserved	4KB	0x5001_F000	0x5001_FFFF	0x5001_F000	0x5001_FFFF
	Reserved	128KB	0x5002_0000	0x5003_FFFF	0x5002_0000	0x5003_FFFF
HPSYS_AHB1		**256KB**	**0x5004_0000**	**0x5007_FFFF**	**0x5004_0000**	**0x5007_FFFF**
	Reserved	4KB	0x5004_0000	0x5004_0FFF	0x5004_0000	0x5004_0FFF
	MPI1	4KB	0x5004_1000	0x5004_1FFF	0x5004_1000	0x5004_1FFF
	MPI2	4KB	0x5004_2000	0x5004_2FFF	0x5004_2000	0x5004_2FFF
	Reserved	4KB	0x5004_3000	0x5004_3FFF	0x5004_3000	0x5004_3FFF
	Reserved	4KB	0x5004_4000	0x5004_4FFF	0x5004_4000	0x5004_4FFF
	SDMMC1	4KB	0x5004_5000	0x5004_5FFF	0x5004_5000	0x5004_5FFF
	Reserved	4KB	0x5004_6000	0x5004_6FFF	0x5004_6000	0x5004_6FFF
	USBC	4KB	0x5004_7000	0x5004_7FFF	0x5004_7000	0x5004_7FFF
	CRC1	4KB	0x5004_8000	0x5004_8FFF	0x5004_8000	0x5004_8FFF
	Reserved	28KB	0x5004_9000	0x5004_FFFF	0x5004_9000	0x5004_FFFF
	GFX_RAM	64KB	0x5005_0000	0x5005_FFFF	0x5005_0000	0x5005_FFFF
	Reserved	128KB	0x5006_0000	0x5007_FFFF	0x5006_0000	0x5007_FFFF
HPSYS_APB2		**128KB**	**0x5008_0000**	**0x5009_FFFF**	**0x5008_0000**	**0x5009_FFFF**
	PTC1	4KB	0x5008_0000	0x5008_0FFF	0x5008_0000	0x5008_0FFF
	DMAC1	4KB	0x5008_1000	0x5008_1FFF	0x5008_1000	0x5008_1FFF
	MAILBOX1	4KB	0x5008_2000	0x5008_2FFF	0x5008_2000	0x5008_2FFF
	Reserved	4KB	0x5008_3000	0x5008_3FFF	0x5008_3000	0x5008_3FFF
	USART1	4KB	0x5008_4000	0x5008_4FFF	0x5008_4000	0x5008_4FFF
	USART2	4KB	0x5008_5000	0x5008_5FFF	0x5008_5000	0x5008_5FFF
	USART3	4KB	0x5008_6000	0x5008_6FFF	0x5008_6000	0x5008_6FFF
	GPADC	4KB	0x5008_7000	0x5008_7FFF	0x5008_7000	0x5008_7FFF
	AUDCODEC	4KB	0x5008_8000	0x5008_8FFF	0x5008_8000	0x5008_8FFF
	TSEN	4KB	0x5008_9000	0x5008_9FFF	0x5008_9000	0x5008_9FFF
	Reserved	4KB	0x5008_A000	0x5008_AFFF	0x5008_A000	0x5008_AFFF
	Reserved	4KB	0x5008_B000	0x5008_BFFF	0x5008_B000	0x5008_BFFF
	Reserved	4KB	0x5008_C000	0x5008_CFFF	0x5008_C000	0x5008_CFFF
	Reserved	4KB	0x5008_D000	0x5008_DFFF	0x5008_D000	0x5008_DFFF
	Reserved	4KB	0x5008_E000	0x5008_EFFF	0x5008_E000	0x5008_EFFF
	Reserved	4KB	0x5008_F000	0x5008_FFFF	0x5008_F000	0x5008_FFFF
	GPTIM1	4KB	0x5009_0000	0x5009_0FFF	0x5009_0000	0x5009_0FFF
	Reserved	4KB	0x5009_1000	0x5009_1FFF	0x5009_1000	0x5009_1FFF
	BTIM1	4KB	0x5009_2000	0x5009_2FFF	0x5009_2000	0x5009_2FFF
	Reserved	4KB	0x5009_3000	0x5009_3FFF	0x5009_3000	0x5009_3FFF
	WDT1	4KB	0x5009_4000	0x5009_4FFF	0x5009_4000	0x5009_4FFF
	SPI1	4KB	0x5009_5000	0x5009_5FFF	0x5009_5000	0x5009_5FFF
	SPI2	4KB	0x5009_6000	0x5009_6FFF	0x5009_6000	0x5009_6FFF
	Reserved	4KB	0x5009_7000	0x5009_7FFF	0x5009_7000	0x5009_7FFF
	Reserved	4KB	0x5009_8000	0x5009_8FFF	0x5009_8000	0x5009_8FFF
	Reserved	4KB	0x5009_9000	0x5009_9FFF	0x5009_9000	0x5009_9FFF
	PDM1	4KB	0x5009_A000	0x5009_AFFF	0x5009_A000	0x5009_AFFF
	Reserved	4KB	0x5009_B000	0x5009_BFFF	0x5009_B000	0x5009_BFFF
	I2C1	4KB	0x5009_C000	0x5009_CFFF	0x5009_C000	0x5009_CFFF
	I2C2	4KB	0x5009_D000	0x5009_DFFF	0x5009_D000	0x5009_DFFF
	I2C3	4KB	0x5009_E000	0x5009_EFFF	0x5009_E000	0x5009_EFFF
	I2C4	4KB	0x5009_F000	0x5009_FFFF	0x5009_F000	0x5009_FFFF
HPSYS_AHB2		**64KB**	**0x500A_0000**	**0x500A_FFFF**	**0x500A_0000**	**0x500A_FFFF**
	GPIO1	4KB	0x500A_0000	0x500A_0FFF	0x500A_0000	0x500A_0FFF
	Reserved	60KB	0x500A_1000	0x500A_FFFF	0x500A_1000	0x500A_FFFF
HPSYS_APB3		**64KB**	**0x500B_0000**	**0x500B_FFFF**	**0x500B_0000**	**0x500B_FFFF**
	GPTIM2	4KB	0x500B_0000	0x500B_0FFF	0x500B_0000	0x500B_0FFF
	BTIM2	4KB	0x500B_1000	0x500B_1FFF	0x500B_1000	0x500B_1FFF

Continued on the next page

Table 1-1: Address Mapping of HPSYS (continued)

Category	Memory /IP	Address Space	HCPU		LCPU	
			Starting Address	Ending Address	Starting Address	Ending Address
	Reserved	56KB	0x500B_2000	0x500B_FFFF	0x500B_2000	0x500B_FFFF
HPSYS_APB4		**256KB**	**0x500C_0000**	**0x500F_FFFF**	**0x500C_0000**	**0x500F_FFFF**
	HPSYS_AON	4KB	0x500C_0000	0x500C_0FFF	0x500C_0000	0x500C_0FFF
	LPTIM1	4KB	0x500C_1000	0x500C_1FFF	0x500C_1000	0x500C_1FFF
	LPTIM2	4KB	0x500C_2000	0x500C_2FFF	0x500C_2000	0x500C_2FFF
	Reserved	4KB	0x500C_3000	0x500C_3FFF	0x500C_3000	0x500C_3FFF
	Reserved	24KB	0x500C_4000	0x500C_9FFF	0x500C_4000	0x500C_9FFF
	PMUC	4KB	0x500C_A000	0x500C_AFFF	0x500C_A000	0x500C_AFFF
	RTC	4KB	0x500C_B000	0x500C_BFFF	0x500C_B000	0x500C_BFFF
	IWDT	4KB	0x500C_C000	0x500C_CFFF	0x500C_C000	0x500C_CFFF
	Reserved	12KB	0x500C_D000	0x500C_FFFF	0x500C_D000	0x500C_FFFF
	Reserved	64KB	0x500D_0000	0x500D_FFFF	0x500D_0000	0x500D_FFFF
	Reserved	64KB	0x500E_0000	0x500E_FFFF	0x500E_0000	0x500E_FFFF
	Reserved	4KB	0x500F_0000	0x500F_0FFF	0x500F_0000	0x500F_0FFF
	Reserved	60KB	0x500F_1000	0x500F_FFFF	0x500F_1000	0x500F_FFFF

1.3.5 Interrupt List

Table 1-2: Interrupt List of HCPU

IRQ #	IRQ Source
NMI	WDT1
IRQ[0]	AON
IRQ[1]	LCPU_IRQ[1]
IRQ[2]	LCPU_IRQ[2]
IRQ[3]	LCPU_IRQ[3]
IRQ[4]	LCPU_IRQ[4]
IRQ[5]	LCPU_IRQ[5]
IRQ[6]	LCPU_IRQ[6]
IRQ[7]	LCPU_IRQ[7]
IRQ[8]	LCPU_IRQ[8]
IRQ[9]	LCPU_IRQ[9]
IRQ[10]	LCPU_IRQ[10]
IRQ[11]	LCPU_IRQ[11]
IRQ[12]	LCPU_IRQ[12]
IRQ[13]	LCPU_IRQ[13]
IRQ[14]	LCPU_IRQ[14]
IRQ[15]	LCPU_IRQ[15]
IRQ[16]	LCPU_IRQ[16]
IRQ[17]	LCPU_IRQ[17]
IRQ[18]	LCPU_IRQ[18]
IRQ[19]	LCPU_IRQ[19]
IRQ[20]	LCPU_IRQ[20]
IRQ[21]	LCPU_IRQ[21]
IRQ[22]	LCPU_IRQ[22]
IRQ[23]	LCPU_IRQ[23]
IRQ[24]	rsvd
IRQ[25]	rsvd
IRQ[26]	rsvd
IRQ[27]	rsvd
IRQ[28]	rsvd
IRQ[29]	rsvd
IRQ[30]	rsvd
IRQ[31]	rsvd
IRQ[32]	rsvd
IRQ[33]	rsvd
IRQ[34]	rsvd

Continued on the next page

Table 1-2: Interrupt List of HCPU (continued)

IRQ #	IRQ Source
IRQ[35]	rsvd
IRQ[36]	rsvd
IRQ[37]	rsvd
IRQ[38]	rsvd
IRQ[39]	rsvd
IRQ[40]	rsvd
IRQ[41]	rsvd
IRQ[42]	rsvd
IRQ[43]	rsvd
IRQ[44]	rsvd
IRQ[45]	rsvd
IRQ[46]	LPTIM1
IRQ[47]	LPTIM2
IRQ[48]	PMUC
IRQ[49]	RTC
IRQ[50]	DMAC1_CH1
IRQ[51]	DMAC1_CH2
IRQ[52]	DMAC1_CH3
IRQ[53]	DMAC1_CH4
IRQ[54]	DMAC1_CH5
IRQ[55]	DMAC1_CH6
IRQ[56]	DMAC1_CH7
IRQ[57]	DMAC1_CH8
IRQ[58]	MAILBOX2_CH1
IRQ[59]	USART1
IRQ[60]	SPI1
IRQ[61]	I2C1
IRQ[62]	EPIC
IRQ[63]	LCDC1
IRQ[64]	I2S1
IRQ[65]	GPADC
IRQ[66]	EFUSEC
IRQ[67]	AES
IRQ[68]	PTC1
IRQ[69]	TRNG
IRQ[70]	GPTIM1
IRQ[71]	GPTIM2
IRQ[72]	BTIM1
IRQ[73]	BTIM2
IRQ[74]	USART2
IRQ[75]	SPI2
IRQ[76]	I2C2
IRQ[77]	EXTDMA
IRQ[78]	I2C4
IRQ[79]	SDMMC1
IRQ[80]	MAILBOX2_CH2
IRQ[81]	rsvd
IRQ[82]	PDM1
IRQ[83]	rsvd
IRQ[84]	GPIO1
IRQ[85]	MPI1
IRQ[86]	MPI2

Continued on the next page

Table 1-2: Interrupt List of HCPU (continued)

IRQ #	IRQ Source
IRQ[87]	rsvd
IRQ[88]	rsvd
IRQ[89]	EZIP1
IRQ[90]	AUDPRC
IRQ[91]	TSEN
IRQ[92]	USBC
IRQ[93]	I2C3
IRQ[94]	ATIM1
IRQ[95]	USART3
IRQ[96]	AUD_HP
IRQ[97]	rsvd
IRQ[98]	SECU1
IRQ[99]	rsvd

1.4 Power Management

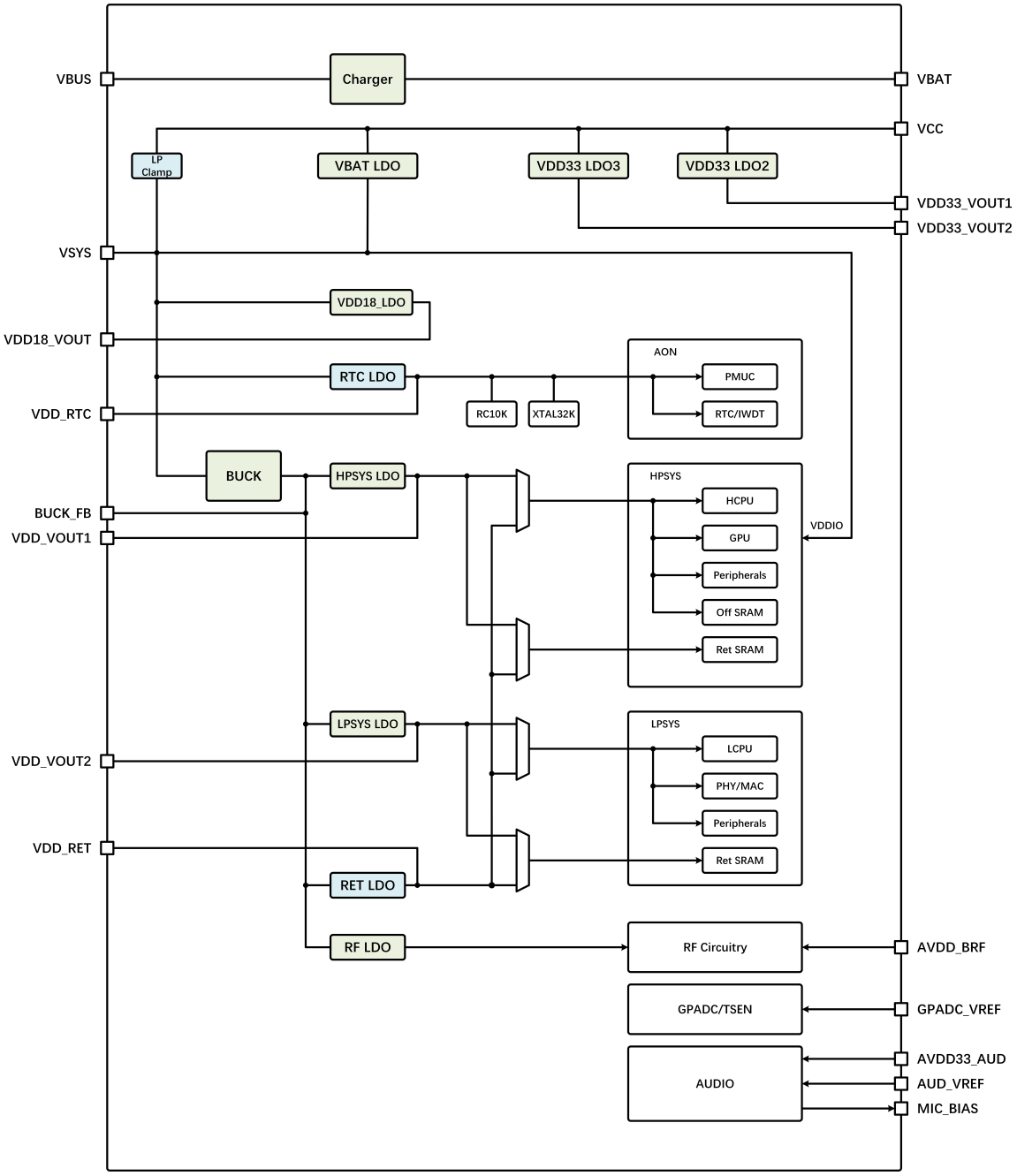


Figure 1-3: Power Management Architecture of QFN Package

1.4.1 Charger

The chip integrates a lithium battery charging module. The charging current and full voltage can be adjusted, and the charging current supports up to 560 mA. Customers can set the corresponding parameters according to the battery specifications and the wire resistance of VBUS.

The following figure 1-4 is the charging curve of the battery. When the battery voltage is lower than V_{cc}, the charging

module is in Trickle Charge mode, which will charge the battery with a lower current I_{tri}. When the battery voltage is higher than V_{cc}, the charging module is in Constant Charge mode and charged with constant current I_{cc} until the battery voltage is close to the set full voltage V_{cv}. After that, the charging module enters the Constant Voltage mode. In this mode, the charging current will slowly drop until the current is less than the cut-off charging current I_{end}, the charging loop is automatically disconnected and enters the Charger Full mode. After the battery is fully charged, if the power adapter is not disconnected, the battery voltage is reduced to the Re-Charge Threshold after a period of time, and the charging program will automatically start until the battery is fully charged.

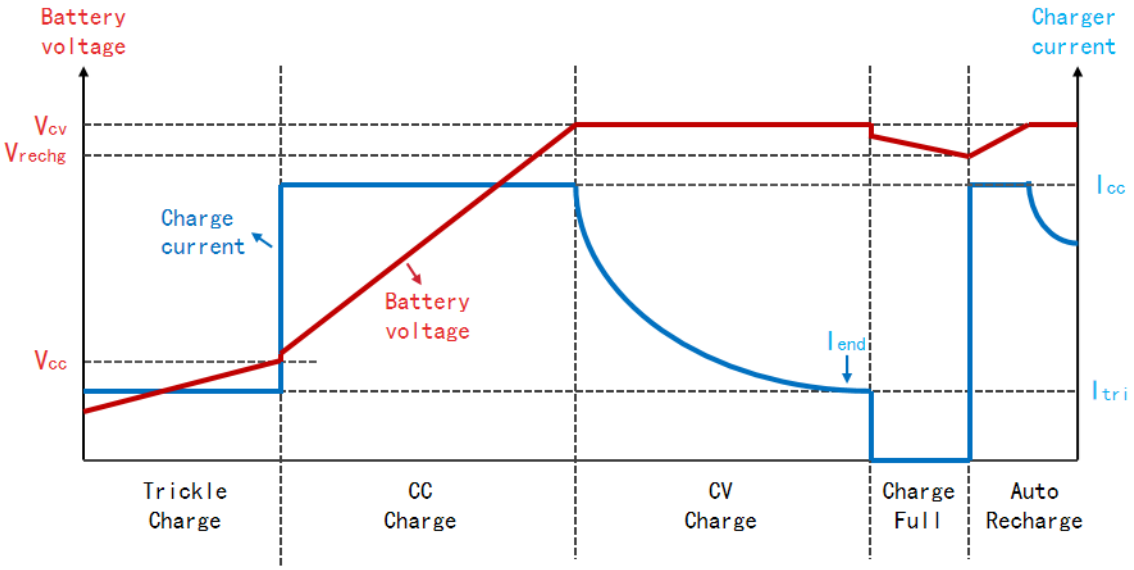


Figure 1-4: Charging Curve

2 High-Performance Dedicated Computing

2.1 ePicasso™ High-Performance 2.5D GPU

In 2.5D image processing, many common image operations will consume a lot of CPU computing resources. ePicasso™ is an acceleration GPU designed specifically for 2.5D image operations. It can provide exponential speed improvements for common 2.5D image operations such as layer overlay, scaling, and rotation. In addition, ePicasso™ is compatible with various common RGB image formats, simplifying the conversion of different image formats in the system.

2.1.1 Layer Overlay

ePicasso™ supports two foreground layers, one dedicated mask layer, and one monochrome background layer. The input and output formats include commonly used RGB565, RGB888, ARGB8565, ARGB8888, L8, A8, A4, A2 and YUV. Each foreground layer has a separate overlay mode and overlay area, and the mask layer is mainly used to extract specific shapes of the image. In addition, each layer also has a separate filter configuration option, which can make the layer filter out a specific color. This function can be used for simple image capture.

2.1.2 Graphics Scaling

ePicasso™ has a layer called functional layer, which, in addition to supporting overlays, enables the scaling of graphics up to 1024 times, with an accuracy of 1/65536. The scaling can be configured separately in the X and Y directions to suit different requirements.

2.1.3 Graphics Rotation

In addition to scaling, the functional layer of ePicasso™ can support high-precision rotation of images. Users can customize the sin/cos values of the rotation angle to meet the rotation requirements of any angle. Rotation and scaling can be enabled at the same time to complete two operations of the image at one time, which improves the performance of image processing.

2.2 LCD Controller

The LCD controller is mainly used to output data from the Framebuffer to the external display, and the existing LCD controller can support common screen interfaces, including DBI and DPI. In addition, the LCD controller also supports images of compressed format, which can significantly reduce the memory usage bandwidth and improve system performance.

2.2.1 Display Interface

The LCD controller is mainly used for the adaptation between the data for display and the mainstream display interfaces, and the following display interfaces are supported by this chip.

2.2.1.1 MIPI-DBI

The LCD controller can support serial SPI mode and parallel 8080 mode in the DBI interface. For SPI mode, the LCD controller can support both 3-wire and 4-wire modes, as well as dual/quad data line operations. It supports 8-bit RGB332, 16-bit RGB565 and 24-bit RGB888 in color format. For the 8080 mode, the LCD controller supports bus widths of 8-bit, 16-bit and 24-bit, and also supports color formats of RGB332, RGB444, RGB565, RGB666 and RGB888.

2.2.1.2 JDI Reflective Display

To meet the low-power requirements of wearable products, JDI has developed an ultra-low-power reflective display that uses the sun's rays to present images. Compared with the traditional LCD screen, the power consumption can be reduced by more than 95%. It can be used in wearable products to achieve long battery life. The LCD controller also added support for JDI reflective display interface, including serial interface and parallel interface. The two interfaces can support up to 64-color display, and support partial refresh and full-screen refresh, thereby further reducing the power consumption of screen refresh and meeting the needs of long battery life.

2.3 eZip™ Lossless Compression Decoder

The eZip™ decoder is a real-time lossless decompression module based on proprietary algorithm, with a compression rate equivalent to that of the Zip format. It can be used to decode the general data before saving it, which will improve the real-time loading capability of the data. If the data is transferred from outside the chip, the transfer after compression will help shorten the transfer time and reduce the power consumption.

In addition, eZip™ also supports image compression of proprietary formats, with a compression rate equivalent to that of the PNG format, and supports independent DMA operations or reading linked with ePicasso™. When operating independently, eZip™ can flexibly decompress and transport the compressed pictures stored in Flash or RAM to the target cache through the DMA mechanism. In the linkage mode, ePicasso™ reads pictures from the memory in real time and decompresses them in real time through the eZip™ module, and then performs the required 2.5D calculations according to the general graphics process, thereby saving the cache for temporary storage of decompressed pictures.

Through the above mechanism, eZip™ can effectively reduce the demand for storage capacity of image materials, maximize the richness of materials in limited storage, and reduce the bandwidth requirements for off-chip storage, thereby greatly improving the overall operating efficiency of the system.

The eZip™ module is a module for decoding the eZip™ compressed images and outputting them. The module reads compressed data through the AHB bus, and the decoded image data can be configured to be output through the AHB bus or directly sent to the epic module for subsequent processing.

The module has the following characteristics:

- The data address input/output via the AHB bus can be configured
- Output image data can be sent directly to the epic module
- Can output image data for a specified area
- Support decoding parameter cache function, which can shorten decoding time in case of cache hit

3 Peripherals

3.1 Dual-mode Bluetooth 5.3

3.1.1 RF and Baseband

BLE RF and baseband include the transmitter and the receiver. The transmitter modulates the baseband signal to the 2.4G frequency band and transmits it, and the receiver receives the over-the-air 2.4G frequency band signal and demodulates it to the baseband signal.

The main features are:

- Support Bluetooth 5.3 protocol: 1M PHY (1Mbps), 2M PHY (2Mbps), BR PHY（1Mbps）, EDR2 PHY（2Mbps）, EDR3 PHY（3Mbps）
- Integrated AGC
- Support RSSI
- The receiver supports automatic frequency offset correction
- Adjustable transmit power, BLE/BR PHY max. Tx 19dBm, EDR2/EDR3 max. Tx 13dBm
- Integrated Balun and antenna matching network, no off-chip matching required

3.1.2 BT MAC

The BT MAC is a dual-mode baseband controller that fully supports Bluetooth protocol v5.3 and is compatible with v4.2, v4.1, and 4.0. It is mainly used for packet encoding and decoding as well as event scheduling.

The main functions are as follows:

- BLE mode:
  1. Support rate (1M/2M);
  2. Support all packet formats (broadcast packet/expanded broadcast packet/data packet, etc.);
  3. Support data encryption and decryption;
  4. Support data stream processing (redundancy checking, whitening);
  5. Support two frequency hopping modes;
- Classic Bluetooth mode:
  1. Support all packet types of ACL, CSB, SCO and eSCO;
  2. Support data encryption and decryption (E0 encryption and AES-CCM encryption);
  3. Support data stream processing (HEC, CRC, Whitening, FEC2/3, FEC1/3);
  4. Support coding and decoding of audio data (CVSD and a/μ-Law);
  5. Support adaptive frequency hopping;
- And
  - Support AMBA AHB bus access;
  - Support WLAN/MWS coexistence mechanism.

3.2 Analog Peripherals

3.2.1 12Bit Analog/Digital Converter

GPADC contains a SARADC, and the basic function is to convert the external input voltages into digital signals.

The main features of GPADC are:

- 12-bit resolution
- Maximum sampling rate 4MS/s
- Single-ended input voltage: 0 ~ 3.3V
- Differential input voltage: -2.1V ~ +2.1V
- Support 7 single-ended analog inputs and 1 additional measurement battery voltage, or 3 pairs of differential analog inputs
- Support single measurement mode and cyclic measurement mode
- Each measurement can be divided into 8 time slots, and each time slot can be individually configured with analog input channels
- Support software (write register) and hardware (e.g. timer) triggering
- Support DMA channels
- Sampling frequency can be configured

Table 3-1: 12-bit GPADC Specifications

	Min.	Typ.	Max.	Unit	Comments
Resolution		12		bit	
T_{sample} (Differential)	125n		2/3	s	fs=1/(T_{sample}+$T_{conversion}$)
T_{sample} (Single-Ended)	166.66n		2/3	s	
$T_{conversion}$	125n		10.67u	s	
Sample rate (fs)			4	Msps	
ENOB (Differential)		10.6		bit	V_{in}=-1dBFs, no averaging
ENOB (Single-Ended)		10		bit	V_{in}=-3dBFs, no averaging
SNDR (Differential)		65.6		dB	V_{in}=-1dBFs, no averaging
SNDR (Single-Ended)		61.96		dB	V_{in}=-3dBFs, no averaging
Current Consumption		466		uA	fs=4Msps
		130		uA	fs=500ksps
		90		uA	fs=100ksps

The relationship between GPADC source resistance R_{AIN} and the sampling time is as follows:

Resolution (bit)	Number of T_{PCLK} Cycle @24MHz	T_{sample} (ns)	Maximum source resistance R_{AIN} (kOhm)
12	4	166	1
	15	625	5
	30	1250	10
	150	6250	50
	300	12500	100
	1500	62500	500
	15000	625000	5000

3.2.2 Temperature Sensor

The temperature sensor converts the temperature into a voltage that changes with the temperature, and then converts the voltage into a number through the ADC. The system calls the temperature sensor through the software.

The main features are as follows:

- Temperature sensor resolution 0.2°C
- Support temperature range from -40°C to 125°C
- Temperature sensor accuracy -3°C to 3°C
- Support polling or interrupt mode reading

3.2.3 Audio DAC

Audio DAC is a module that converts digital audio signals into analog voltage output. The chip integrates one 24-bit DAC, supporting audio sampling rates from 8KHz to 48KHz, and supports differential output.

3.2.4 Audio PLL

The main function of audio PLL is to provide high-precision clock for the audio system. It supports the fractional frequency division function with an adjustment accuracy of 48MHz/2^18, and can meet the needs of different sampling rates such as 48KHz, 32KHz and 44.1KHz.

3.2.5 Audio ADC

Audio ADC is a module that converts external analog singals into internal digital audio signals. The chip integrates one 24-bit ADC, supporting audio sampling rates from 8KHz to 48KHz, and each ADC has separate gain adjustments.

3.3 DMA

3.3.1 ExtDMA

The ExtDMA (Extended Direct Memory Access) enables efficient data transfer between two different address ranges on the bus.Compared to DMAC, ExtDMA is more efficient in accessing external memory (e.g. FLASH, PSRAM), but it has only one channel, supports only 4-byte aligned handling, and does not respond to peripheral requests.

Main features of ExtDMA:

- Single AHB master controller,access SRAM PSRAM FLASH,etc.,support burst transmission
- Single transmission channel, built-in FIFO with a depth of 16 and a bit width of 32 bits
- Both the source address and the destination address are accessed in 4 bytes, and support automatic address increment
- The maximum number of transmission units in a single configuration is 2^20-1, with a fixed 4-byte transmission per unit, i.e., a maximum of 4M bytes in a single transmission
- Each channel supports transmission completion, half transmission, and transmission error event flags, and can generate interrupt requests independently

3.3.2 DMAC

The DMAC (Direct Memory Access Controller) is used to carry out data transfer between two different address ranges on the bus. DMAC has a total of 8 independent channels. Each channel can be configured with a source address range and a target address range, which are respectively mapped to the address range of each memory or peripheral, so as to achieve high-efficiency transmission between memory-memory, memory-peripheral, peripheral-memory, and peripheral-peripheral, which can effectively alleviate the workload of the CPU.

The DMAC supports peripheral response mode and memory handling mode: In the peripheral response mode, the DMAC performs handling based on the DMA request of the peripheral, thereby adapting the bandwidth of the peripheral; In the memory handling mode, the DMAC does not wait for the DMA request of the peripheral, and will complete data transfer as soon as possible. When multiple channels are enabled at the same time, the DMAC will transport in order of priority from high to low; and in the process of transporting lower priority channels, the higher priority channels can carry out the preemption handling. Each channel can generate an interrupt or PTC trigger when the transmission is halfway or complete.

DMAC1 and DMAC2 is located in HPSYS and can respond to DMA requests from HPSYS peripherals. DMAC3 is located in LPSYS and can respond to DMA requests from LPSYS peripherals.

Main features of DMAC:

- Single AHB master controller,access SRAM PSRAM FLASH,AHB,APB,etc.
- 8 independent configurable channels
- The DMA request for each channel can be selected from up to 64 peripheral DMA requests, or can be requested by software
- Each channel supports 4 levels of priority configuration, when the priority is the same, it is judged according to the channel number
- Support peripheral-memory, memory-peripheral, memory-memory, peripheral-peripheral transfer
- Support single-byte/ double-byte/ 4-byte access to both source and destination addresses independently.The addresses of the source and target must be aligned according to the size of the transmission data unit, and support automatic address increment
- The number of single transmission units can be configured from 0 to 65536.
- Support cyclic buffering mode, which will automatically restart after a single transfer is completed
- Each channel supports 3 types of event flags,i.e. transmission completed, half-transmission, transmission error, and can independently generate interrupts or PTC triggers
- Each channel supports block transfer mode with configurable block size

3.4 AUDPRC

The audio processing module performs sampling rate conversion, mixing and equalization for audio data from different sources, and sends the processed audio data to the corresponding playback or storage device. It mainly includes two main data paths, the DAC path for processing playback data and the ADC path for processing audio acquisition data.

3.4.1 DAC Path

DAC path audio data comes from memory, and AUDPRC supports up to four channels of 24bit audio data. The DAC path in AUDPRC supports sampling rate conversion for two channels of data. The sampling rate conversion range is 1/8~8 times,

and the singal-to-noise ratio is not less than 96dB. After the converted data is mixed with data of the other two channels, it enters the 10-level audio equalizer, the parameters of which can be configured by users according to needs. Finally, the two-channel audio data passing through the equalizer can be sent to the analog DAC module or the I2S interface as output.

3.4.2 ADC Path

ADC path audio data comes from analog ADC or the I2S interface, and supports up to two channels of 24bit audio data. The data through the sampling rate conversion module can be stored in memory by DMA.

3.5 I/O Peripherals

3.5.1 General Purpose Input/ Output (GPIO)

The system supports up to 45 GPIOs. Different functions can be assigned to these pins by configuring the corresponding registers.

When configured as an output function, the output value can be configured through the register.

When configured as an input function, the input value can be queried through the corresponding register, and support the input signal interrupt trigger at the same time. The interrupt trigger mode can be set to level trigger and edge trigger, which includes upper and lower dual-edge trigger.

3.5.2 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous Receiver/Transmitter (UART) supports full-duplex mode and offers baud rates up to 6Mbps and a variety of configurable data formats, providing a flexible and efficient means of data interaction for communication with external standardized devices. It also supports DMA for multi-packet transceiving.

UART1、UART2 and UART3 are located in HPSYS。UART4 and UART5 are located in LPSYS。

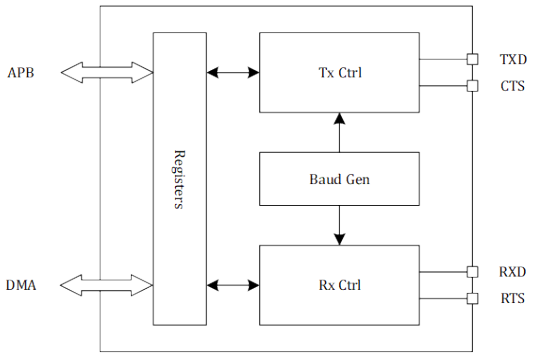


Figure 3-1: UART

Main features of UART:

- Full-duplex asynchronous communication
- Configurable 16 times oversampling or 8 times oversampling, select frequency priority or clock tolerance priority

- Flexible baud rate configuration, when the input clock is 48MHz and the oversampling rate is 16, the baud rate is 3Mbps
- Configurable packet length (7/8/9 bits)
- Configurable stop bit (1/2 bits)
- Hardware flow control (CTS/RTS)
- DMA multi-packet sending and receiving
- Receiving parity check and sending parity generation
- Receiving and sending interrupts, and other error interrupts

Baud rate calculation instructions

Assuming that the input clock is fixed at 48MHz, the baud rate calculation formula is as follows:

$$Baud\ Rate = \frac{48MHz}{(BRR_{INT} + \frac{BRR_{FRAC}}{16})(16\ or\ 8)} \tag{3.1}$$

3.5.3 I2C

The I2C (Inter-Integrated Circuit) interface supports both the roles of master and slave. It can be used as a master to communicate with I2C slave peripherals, or as a slave to respond to an external I2C master. I2C has a built-in 8-byte FIFO, which can perform single read and write, or batch data read and write through DMA. I2C supports standard mode, fast mode, fast mode plus, and high-speed mode, with a maximum speed of 3.4Mbps.

Main features of I2C:

- Can be used as master and slave at the same time
- Support bus multi-master
- Support standard mode (up to 100kbps)
- Support fast mode (up to 400kbps)
- Support fast mode + (up to 1Mbps)
- Support high-speed mode (up to 3.4Mbps)
- As a master, it supports access to 7-bit or 10-bit addressing
- As a slave, it supports access to 7-bit addressing
- Configurable bus timing
- Support clock stretching
- 8-byte FIFO, support DMA
- Configurable digital anti-jitter circuit
- Independent functional clock, support system clock dynamic adjustment

3.5.4 PDM

The PDM (Pulse Density Modulation) interface is mainly used to convert the PDM audio signal captured by the PDM microphone into PCM (Pulse Code Modulation) signal for subsequent audio processing.

Main features of PDM:

- Support left and right stereo signals at the same time, and can also collect mono signals separately
- Available PDM microphone clock rates: 3.072MHz, 1.536MHz, 0.768MHz, 1.024MHz, 2.4MHz, 1.6MHz, 0.8MHz

- Support PCM data rates: 48kHz, 32kHz, 24kHz, 16kHz, 12kHz, 8kHz
- Support 32bit, 24bit, 16bit and 8bit PCM signals
- Support resolution of 0.5dB and gain adjustable from -15dB to 45dB

3.5.5 I2S

The I2S interface is used for audio input and output, and can be used to connect external audio chips, digital microphones and other devices. Compared with the analog audio interface, the I2S digital audio interface has a better anti-interference ability and a more streamlined interface protocol.

Main features of I2S:

- Support both master and slave modes
- Support full duplex mode
- Configurable I2S data format, including left-justified, right-justified and standard format
- Support multiple audio data formats, including 8-bit and 16-bit mono and stereo formats
- Configurable I2S PCM signal bit width, up to 24-bit

3.5.6 Serial Peripheral Interface (SPI)

The SPI supports 3 communication formats: SSP/ SPI/ Microwire. SSP/ SPI is a full-duplex communication protocol, and the controller can be configured in Master or Slave mode. Microwire is a half-duplex communication protocol, and the controller can only be configured in Master mode. The SPI controller has a built-in transmit/receive FIFO. The transmit FIFO and the receive FIFO share the same address. The receive FIFO is accessed when the address is read, and the transmit FIFO is accessed when the address is written.

The features of SPI are as follows:

- Support 8 to 32Bit data width
- In SPI format, the clock polarity and phase can be set by register SPO and SPH
- Chip select signal polarity can be configured
- FIFO depth can be set to 32Bits×16Entry or 4Bits/ 8Bits×32Entry
- Both receive and transmit support DMA mode
- The maximum clock frequency of SPI in HPSYS is 48MHz

The working sequences of various communication formats are as follows:

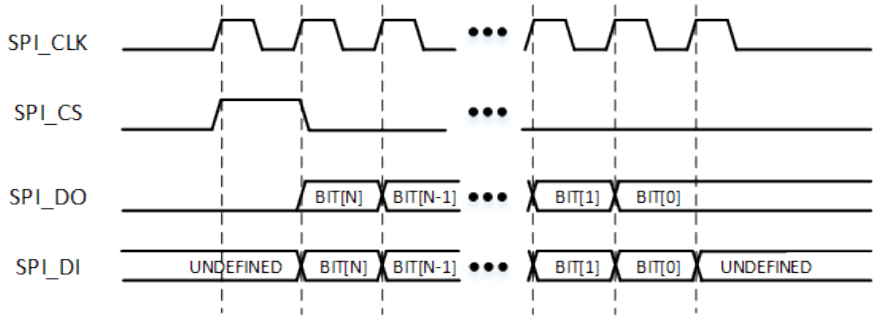


Figure 3-2: Single Transmit and Receive Sequence of SSP Format

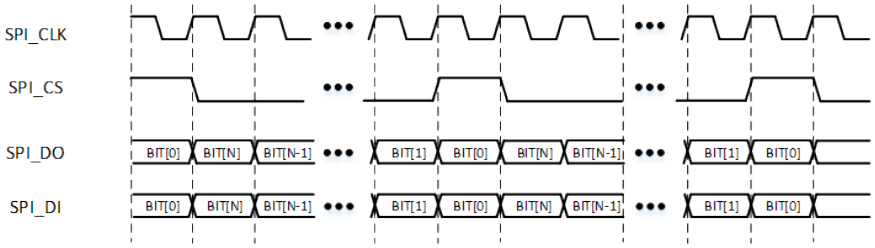


Figure 3-3: Continuous Transmit and Receive Sequence of SSP Format

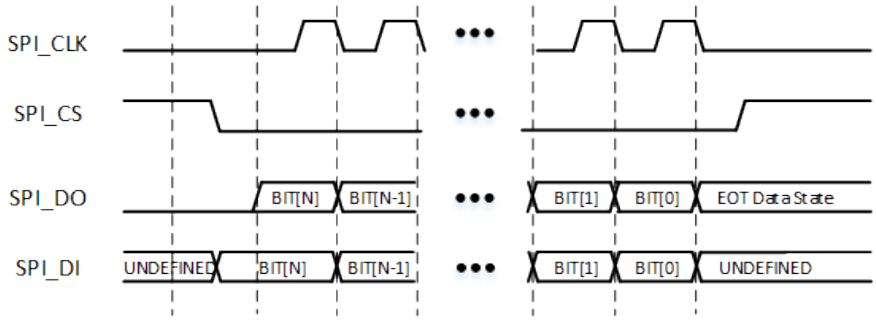


Figure 3-4: Single Transmit and Receive Sequence of SPI Format

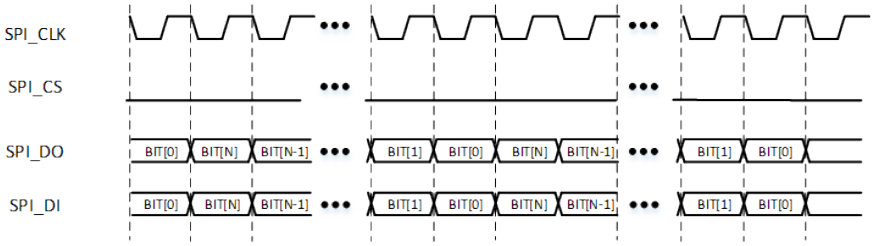


Figure 3-5: Continuous Transmit and Receive Sequence of SPI Format

The following figures illustrate the effect of SPH/SPO settings in SPI format:

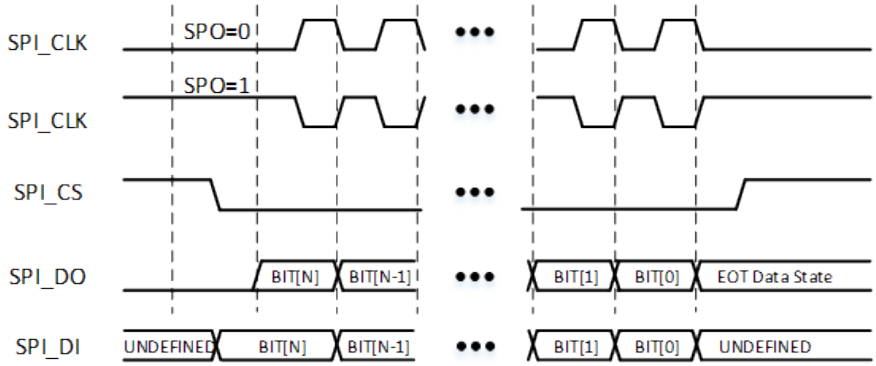


Figure 3-6: SPI Sequence at SPH=0

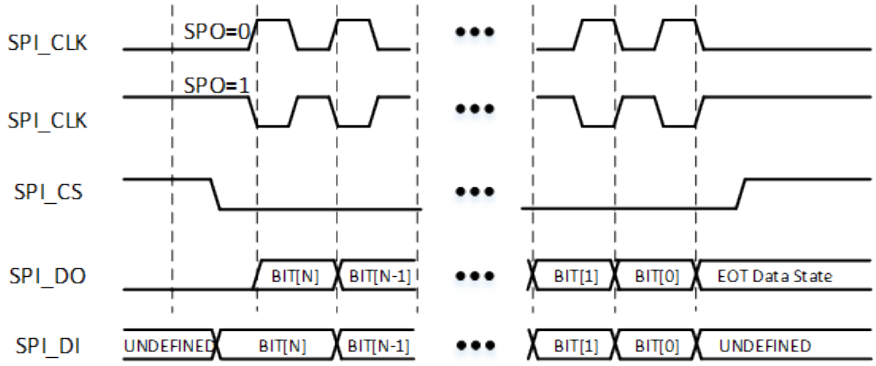


Figure 3-7: SPI Sequence at SPH=1

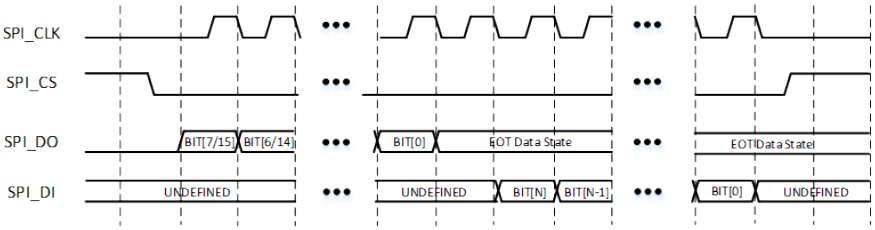


Figure 3-8: Single Transmit and Receive Sequence of Microwire Format

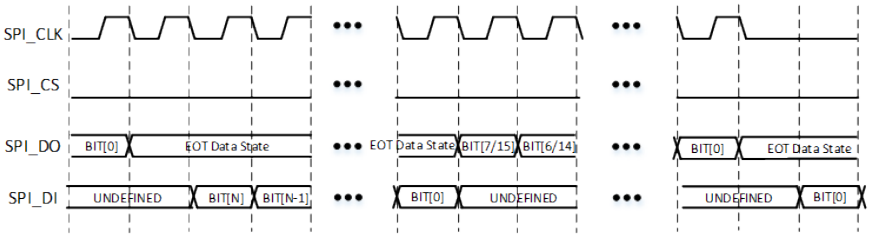


Figure 3-9: Multiple Transmit and Receive Sequence of Microwire Format

3.5.7 Peripheral Task Controller (PTC)

The PTC (Peripheral Task Controller) is a stand-alone peripheral controller, which can automatically complete the mutual scheduling and control tasks of each peripheral without waking up the CPU. Based on the event triggering of the selected peripherals, the PTC can automatically rewrite the working mode or working state of each peripheral, and can chain these tasks together to form an automatically triggered task sequence, thus completing a complex and fast response task chain. In the process of the task chain, the CPU can stay asleep all the time, thereby effectively saving power.

The PTC has a total of 8 channels, independent trigger source can be selected for each channel and independent task can be can be configured. The tasks that can be performed include two types: write the specified data directly to the specified address; read out the contents of the specified address, perform XOR/ and/ or/ addition with the specified data and then write it back. When the task of each channel is completed, a trigger signal can be generated to trigger the tasks of other channels. The number of triggers can be configured for each channel. Some channel support a configurable delay before executing the task after triggering.

Main features of PTC:

- 8 independently configured channels can work at the same time

- Each channel trigger can be selected from 128 trigger sources, including PTC's own trigger sources
- Access to AHB and APB peripheral address space, word-aligned access only
- Support directly writing data, or rewriting after reading
- Support 32-bit XOR/ and/ or/ addition operations
- Configurable trigger times 1 ~ 1023, or unlimited trigger times
- Configurable trigger delay 0 ~ 65535 HCLK cycles
- Fixed priority arbitration, the smaller the channel number, the higher the priority
- The register space of 4 words is used for data cache

3.5.8 USB2.0 FS

This chip integrates a full-speed (FS) USB 2.0 Host/Device interface with the following functions.

- Software configurable endpoint settings, support suspend/ resume
- Support dynamic FIFO size
- Support session request protocol and host negotiation protocol
- Support full speed and slow speed modes
- On-chip integrated USB2.0 FS PHY

3.5.9 SIM Card Controller

The SIM card interface is a half-duplex serial interface. The SIM card controller in this chip supports the sending and receiving of SIM card data packet. The controller can support polling mode and DMA mode. Combined with the upper software, the protocol layer communication function of SIM card can be realized.

3.6 Timers

3.6.1 General-Purpose Timer

The GPTIM (General-Purpose Timer) is based on a 16-bit counter, and can realize functions such as timing, measuring the pulse length of the input signal (input capture) or generating output waveforms (output comparison and PWM). The counter itself can count up, down or up/down. The counting clock can be the system PCLK, IO input signal or cascaded input signal, and can be prescaled from 1 to 65536 times. The GPTIM has 4 channels in total, which can be independently configured as input capture or output mode. The results of counting, input capture and output comparison can generate interrupts, DMA requests or PTC events. The GPTIM has a Master-Slave Mode interface, which can be multi-level cascaded to realize functions such as multi-level counting or synchronous triggering.

Main features of GPTIM:

- 16-bit increment, decrement, increment/ decrement auto-reload counter, the maximum count is 65535
- 16-bit programmable (can be modified in real time) prescaler, the clock division is any value between 1~65536
- 8-bit configurable repeat count
- Support One Pulse Mode (OPM), the counter will stop automatically when the repeated counting is completed
- 4 independent channels, which can be configured as input or output modes respectively
- Input mode
  - Rising edge/ falling edge capture

  - PWM pulse width and period capture (requires two channels)
  - Optional one of 4 input ports or 1 external trigger port, supporting anti-jitter filtering and pre-frequency reduction
- Output mode
  - Forced output high/ low level
  - Output high/ low/ toggle level when counting to the comparison value
  - PWM output, pulse width and period can be configured
  - Multi-channel PWM combined output to generate multiple PWMs with interrelationships
  - Single pulse/ retrigger single pulse mode output
- Master-Slave Mode
  - Support multi-counter interconnection, which can be used as a slave device to be controlled by external input or other master devices while generating control signals as a master device
  - Control modes include reset, trigger, gate control, etc.
  - Support synchronous start and reset of multiple counters
- Encoding mode input, control the incremental/ decremental counting of the counter
- An interrupt/ DMA request/ PTC trigger is generated when the following events occur:
  - Update: Counter increment overflow /decrement overflow, counter initialization (by software or internal/external trigger)
  - Trigger event (counter start, stop, initialization or counting triggered internally/ externally)
  - Input capture
  - Output comparison

3.6.2 Advanced Timer

The ATIM (Advanced Timer) is based on a 32-bit counter, and can realize functions such as timing, measuring the pulse length of the input signal (input capture) or generating output waveforms (output comparison and PWM). ATIM supports 6 complementary PWM outputs with dead zone protection, multiple PWMs with simultaneous phase change, and 2 brake inputs to quickly switch the outputs to a safe state. The counter itself can count up, down or up/down. The counting clock can be the system PCLK, IO input signal or cascaded input signal, and can be prescaled from 1 to 65536 times. The ATIM has 6 channels in total, which can be independently configured as input capture or output mode. The results of counting, input capture and output comparison can generate interrupts, DMA requests or PTC events. The ATIM has a Master-Slave Mode interface, which can be multi-level cascaded to realize functions such as multi-level counting or synchronous triggering.

Main features of ATIM:

- 32-bit increment, decrement, increment/ decrement auto-reload counter
- 16-bit programmable (can be modified in real time) prescaler, the clock division is any value between 1~65536
- 16-bit configurable repeat count
- Support One Pulse Mode (OPM), the counter will stop automatically when the repeated counting is completed
- 6 independent channels
  - Channel 1~3 can be configured as input or output modes respectively, each channel can output 2 complementary PWMs with dead zone protection
  - Channel 4 can be configured to input or output mode, it can output single PWM
  - Channel 5 and 6 can be configured to output comparison mode
- Input mode

  - Rising edge/ falling edge capture
  - PWM pulse width and period capture (requires two channels)
  - Optional one of 4 input ports or 1 external trigger port, supporting anti-jitter filtering and pre-frequency reduction
- Output mode
  - Forced output high/ low level
  - Output high/ low/ toggle level when counting to the comparison value
  - PWM output, pulse width and period can be configured
  - Multi-channel PWM combined output to generate multiple PWMs with interrelationships
  - Single pulse/ retrigger single pulse mode output
- Master-Slave Mode
  - Support multi-counter interconnection, which can be used as a slave device to be controlled by external input or other master devices while generating control signals as a master device
  - Control modes include reset, trigger, gate control, etc.
  - Support synchronous start and reset of multiple counters
- Encoding mode input, control the incremental/ decremental counting of the counter
- Support Hall sensor circuit for positioning
- 2 brake inputs with anti-jilter filter to quickly place the outputs in a safe state. The brake singal sources include
  - CPU lockup
  - External input
  - Software trigger
- An interrupt/ DMA request/ PTC trigger is generated when the following events occur:
  - Update: Counter increment overflow /decrement overflow, counter initialization (by software or internal/external trigger)
  - Trigger event (counter start, stop, initialization or counting triggered internally/ externally)
  - Input capture
  - Output comparison
  - Brake
  - Phase change

3.6.3 Basic Timer

The BTIM (Basic Timer) is based on a 32-bit incremental counter and can realize the timing function. The counter clock can be the system PCLK or cascaded input signal, and can be prescaled from 1 to 65536 times. The timing results can generate interrupts, DMA requests, or PTC events. The BTIM has a Master-Slave Mode interface, which can be multi-level cascaded to realize functions such as multi-level counting or synchronous triggering.

Main features of BTIM:

- 32-bit incremental auto-reload counter
- 16-bit programmable prescaler, the clock division is any value between 1~65536
- Support One Pulse Mode (OPM), the counter will stop automatically when the counting is completed
- Master-Slave Mode
  - Support interconnection with BTIM and GPTIM, which can be used as a slave device to be controlled by external input or other master devices while generating control signals as a master device
  - Control modes include reset, trigger, gate control, etc.

  - Support multiple timers to start and reset simultaneously
- Interrupt， DMA request and PTC trigger will be generated in case of counter overflow or initialization

3.6.4 Low-Power Timer

The LPTIM (Low-Power Timer) is based on a 24-bit incremental counter, and can realize functions such as timing, generating output waveform (output comparison and PWM), and waking up the system. The counter clock can be the system clk, low-power clock, IO input signal or comparator output, and can be prescaled up to 128 times and cycle counting up to 256 times. Depending on the counting results, the PWM output as well as the interrupt can be generated,or the wake-up signal can be generated to wake up the system from the low-power mode. When the IO input signal is used as the count clock, it supports counting independent of the internal clock and generates the wake-up signal, allowing the system to turn off the internal clock.

Main features of LPTIM:

- 24-bit upward automatic reload counter, the maximum count is 16777215 (2^24-1)
- Counting clock selection
  - Internal clock, PCLK2 or low-power clock
  - IO input signal or comparator output with selectable edges, can use the internal clock for anti-jitter, and can also count independently without relying on the internal clock
- 8-level prescaling, clock division is 0 to the 7th power of 2
- 1~256 cycles
- Counting mode
  - Continuous counting mode
  - One Pulse Mode, counting ends after the number of cycles is completed
- Configurable polarity output mode
  - PWM output, can be configured with pulse width and period
  - Single toggle output
  - Single pulse or specified number of pulse output
- Trigger mode
  - Software trigger
  - IO input signal edge trigger, support anti-jitter filtering
- Timeout detection, the counter will be reset on each external trigger
- The interrupt or wake-up signal will be generated when the following events occur:
  - Update
  - Counter overflow
  - Output comparison
  - External trigger

3.6.5 Watchdog

The watchdog timer, as a counter, is mainly used to reset the system after the set time is reached to prevent the software from hanging up.

Basic functions of watchdog timer:

- Support two working modes:

  - Mode0
    - wdt will not generate interruption, and will reset the system directly after the set time is reached
    - Support up to 24-bit counter
  - Mode1
    - Divided into two periods. After reaching the set time of the first period, the interrupt will be generated. After reaching the set time of the second period, the system will be reset
    - Support up to 24-bit counter for each period
- Support write protection to prevent software from misoperation of wdt

3.7 Encryption

3.7.1 AES

The AES accelerator is an arithmetic accelerator for symmetric encryption algorithms. Users can configure the encryption and decryption algorithm keys and initial vectors to perform encryption and decryption operations on the data in the memory, and store the results in the designated memory area.

Compared with software encryption and decryption, the AES accelerator has higher computing speed, more flexible configuration, and better access efficiency to peripheral storage devices. In addition, in bypass mode, the AES accelerator can also be used as a DMA for data transmission.

Features of AES:

- Support AES-128, AES-192, AES-256 and State Secrets SM4 algorithm standard
- Support ECB, CTR and CBC modes
- RootKey can be called to perform encryption and decryption operations, while ensuring that RootKey cannot be read by external programs

3.7.2 HASH

HASH is an operational accelerator for hash sequence algorithms. User can choose different hash algorithms to calculate the hash values of specific data in memory. HASH is faster than the software algorithm, and the configuration is also flexible. Users can also customize the initial vector to achieve multi-threaded HASH operations. The algorithms supported by HASH include SHA1, SHA224, SHA256 and SM3.

3.7.3 CRC

The CRC (Cyclic Redundancy Check) can perform CRC calculations with a specific bit width, any generated polynomial, and any initial value. Data can be input via CPU or DMA with a minimum input unit of a single byte and no maximum byte limit. A single HCLK cycle is sufficient for a single byte input calculation. The check result will be obtained instantly after all data inputs are completed. It supports input data high/ low bit reversal and output data high/ low bit reversal. It supports input data with different valid bit widths.

Features of CRC:

- 7/8/16/32-bit CRC calculation
- Any custom polynomial

- Any initial value
- Supports single byte/ double byte/ triple byte/ quadruple byte valid bit width for input data
- Supports byte/ double byte/ quadruple byte high and low bit reversal for input data
- Supports high and low bit reversal for output data
- Calculation speed is 1 byte per HCLK cycle

3.7.4 True Random Number Generator (TRNG)

The TRNG (True Random Number Generator) is a module that generates random numbers based on the instability of oscillation circuits. No external random entropy source is required for this module, and the random numbers can be generated by activating multiple internal oscillation circuits with a certain entropy source processing logic.

Features of TRNG:

- Independent internal entropy source
- Generate 256-bit seeds and 256-bit random numbers in a single pass
- Deadlock check against entropy source

3.8 Memory Interfaces

3.8.1 MPI

MPI (Memory Peripheral Interface) controller is a dedicated memory communication interface which supports a variety of off-chip memory particles, including:

- SPI NOR Flash, support 1-wire/ 2-wire/ 4-wire, support DTR mode
- SPI NAND Flash, support 1-wire/ 2-wire/ 4-wire
- pSRAM, support x8 and x16 data width, support Xccela standard interface, compatible with Legacy interface
- HyperRAM, support x8 and x16 data width, support HyperBus standard interface

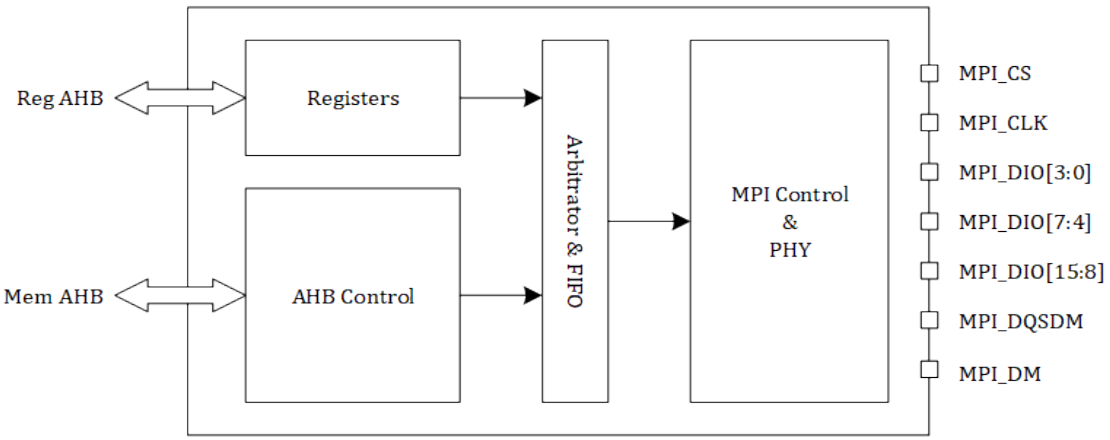


Figure 3-10: MPI Controller Block Diagram

The MPI controller supports two modes of operation: (1) register mode and (2) address-mappping mode. The switching between the two modes is automatically completed by the hardware and can be dynamically interspersed for execution. In either mode, highly customizable interface timing is supported for compatibility with various memory particles.

Register Mode:

- Send a command timing via register operation. The command can also be set as a status query command to be sent repeatedly until the read back data meets a preset status
- Support sending a sequence of two command timings, the second of which can be set as a status query command to be sent repeatedly until the read back data meets a preset status
- Support DMA channels, data handling is completed through the register FIFO interface

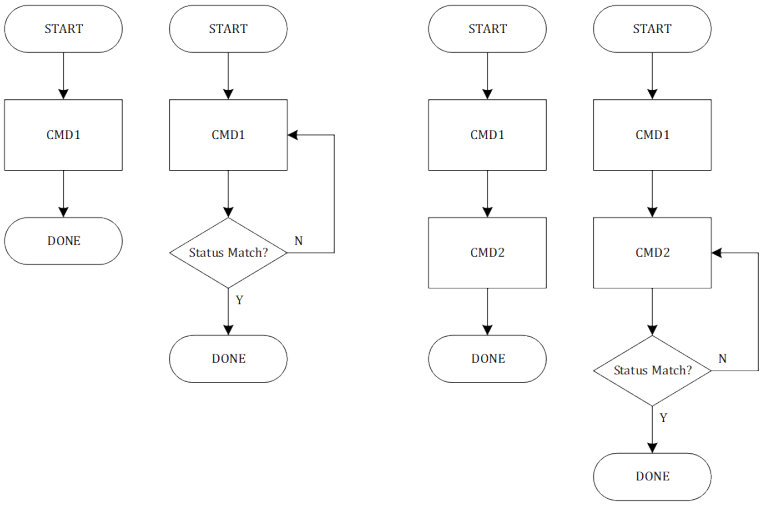


Figure 3-11: Sequence of Single and Multiple Command Timings in Register Mode

Address mapping mode:

- Map the external memory to the AHB address space, and convert the bus read and write to the preset Memory interface timing, realize XIP function
- Support Byte (8-bit), Half-word (16-bit) and Word (32-bit) AHB access
- Efficient conversion of AHB Wrap operations, independent of whether the particles support Wrap or not
- Support XIP real-time (On-The-Fly) decryption, the mode is AES128-CTR or AES256-CTR
- Support continuous read and write function, if the read and write address of the current AHB is continuous with the previous one, the data transmission will be started directly, and the command and address part will be omitted. This feature can greatly increase the effective bandwidth when handling large blocks of data.
- For the internal dynamic refresh feature of pSRAM and HyperRAM, the maximum CS pull-down time of particles, the nearest CS access interval, the maximum burst data length and other restrictions are automatically processed without software processing.

3.8.2 SD/SDIO/eMMC

SDMMC supports SD protocol 3.0 and eMMC standard 4.51, which can interact with SD/SDIO/eMMC devices as host, and read and write data via DMAC. SDMMC supports SDR single-wire and 4-wire modes. It does not support DDR.

Features of SDMMC:

- Compatible with SD Host Controller Standard Specification Version 3.0
- Compatible with SD 3.0 Physical Layer Specification Version 3.01
- Compatible with SDIO Specification Version 3.0

- Compatible with JEDEC JESD84-B451 eMMC 4.51 Specification
- Support SDSC/SDHC/SDXC/SDHS card
- Support SDR12/SDR25/SDR50
- Support SDR single-wire, 4-wire modes
- Built-in 21K byte FIFO, support up to 512 bytes in a single block
- Configurable clock
- Cooperate with DMAC for migration

3.9 Summary of Peripheral Interface Rates

Table 3-2: Common Interface Rates

Controller	Max. Rate	Unit	Remarks
MPI1	144	MHz	SiP OPI-PSRAM
	96	MHz	SiP QSPI-NOR Flash (support DTR)
MPI2	96	MHz	External QSPI-NOR, QSPI-NAND Flash
SDMMC	48	MHz	External eMMC
I2C	3.4	MHz	
SPI	48	MHz	
UART	3	Mbaud	
I2S	48	KHz	Sampling rate 48KHz， 32-bit×2 channel
PDM	3.072	MHz	
GPADC	4	Msps	

4 Electrical Characteristics

4.1 Basic Electrical Characteristics

Table 4-1: Operating Conditions

Symbol	Description	Min	Typ	Max	Unit
VBUS	VBUS power input	4.6	5	5.5	V
VBAT	VBAT power output	3.2		4.7	V
VCC	System power input	3.2		4.7	V
T_{amb}	Ambient temperature	-40		85	°C
V_{IL}	CMOS low level input voltage	0		$0.3\times V_{IO}$	V
V_{IH}	CMOS high level input voltage	$0.7\times V_{IO}$		V_{IO}	V
V_{TH}	CMOS threshold voltage		$0.5\times V_{IO}$		V

Table 4-2: Absolute Max. Ratings

Symbol	Description	Min	Typ	Max	Unit
VBUS	VBUS power input			5.5	V
VBAT	VBAT power output			4.7	V
VCC	System power input			4.7	V
$T_{Storage}$	Storage temperature	-40		125	°C
V_{IN}	Input voltage	0		V_{IO}+0.3	V
V_{LNA}	LNA input level			0	dBm
I_{IN}	Input current			20	mA

Table 4-3: I/O characteristics @3.3V

Symbol	Description	Min	Typ	Max	Unit
C_{IN}	pipe foot capacitor	2.5	3	3.5	pF
V_{IH}	high-level input voltage	0.7*VDDIOA	-	VDDIOA	V
V_{IL}	low-level input voltage	VSS	-	0.3*VDDIOA	V
I_{IH}	high-level input current	-	10	40	nA
I_{IL}	low-level input current	-	10	40	nA
V_{OH}	high-level output voltage (high-resistance load)	0.8*VDDIOA	-	VDDIOA	V
V_{OL}	low-level output voltage (high-resistance load)	VSS	-	0.2*VDDIOA	V
I_{OH}	high-level driving current (V_{OH}=0.8*VDDIOA,max driver)	12	30	38	mA
I_{OL}	low-level driving current (V_{OH}=0.2*VDDIOA,max driver)	12	30	38	mA
R_{PU}	internal pull-up resistance	7	10	20	kΩ
R_{PD}	internal pull-down resistance	7	10	20	kΩ
V_{IH_nRST}	chip reset release voltage	0.7*VDD	-	VDD	V
V_{IL_nRST}	chip reset voltage	VSS	-	0.3*VDD	V

4.2 Reliability

Table 4-4: Reliability Test

Test Item	Test Condition	Applicable Product	Test Criteria
HTOL	Tj=125°C, 1000 hours	SF32LB52x QFN68L	JESD22-A108
ESD	HBM（Human Body Mode）± 4000 V	SF32LB52x QFN68L	JS-001-2017
	CDM（Charge Device Mode）±1000V	SF32LB52x QFN68L	JS-002-2018
Latch-up	I-Test: ± 200mA	SF32LB52x QFN68L	JESD78E
	OVT: +1.5×Vdd_{MAX}	SF32LB52x QFN68L	
MSL3	Baking: 125°C, 24 hours Soaking: 30°C, 60% RH, 192 hours Reflow Soldering: 260 + 0°C, 20 seconds, 3 times	SF32LB52x QFN68L	JESD22-A113
TCT	-65°C~150°C, Dwell=15min, 1000 cycles	SF32LB52x QFN68L	JESD22-A104
uHAST	130°C, 85% RH, 33.3psig, 96 hours	SF32LB52x QFN68L	JESD22-A118
HTSL	150°C, 1000 hours	SF32LB52x QFN68L	JESD22-A103
PCT	121°C, 100% RH, 205kPa, 96 hours	SF32LB52x QFN68L	JESD22-A102
Solderability	245°C, steam aging 8 hours	SF32LB52x QFN68L	J-STD-002

4.2.1 Processor Power Consumption

Table 4-5: Processor Power Consumption

	Clock Frequency	@3.8V Current (uA)	@3.8V Current Increment (uA/MHz)
CoreMark	192MHz	7360	35
	168MHz	6520	
	144MHz	4930	30
	120MHz	4200	
	48MHz	1550	27
	24MHz	810	23
	12MHz	530	
WhileLoop	192MHz	5490	27
	168MHz	4840	
	144MHz	3730	22
	120MHz	3200	
	48MHz	1250	20
	24MHz	690	18
	12MHz	470	
Shutdown	Key wake-up (sending shutdown)	2.0	

4.2.2 BT & BLE Power Consumption

Table 4-6: BT & BLE Power Consumption

Mode	Condition	3.8V @TXpower = 0dBm	3.8V @TXpower = 4dBm	3.8V @TXpower = 10dBm	3.8V @TXpower = 13dBm	Unit
△BT Sniff Mode	240ms (attempt=1)	21.8	22.8	30.0	92.5	uA
	500ms (attempt=4)	23.8	24.8	38.6	158.6	uA
△BLE ADV	200ms	40	43.3	78.9	380	uA
	500ms	16	17.3	31.6	152	uA
	1s	8	8.7	15.8	76	uA
△BLE Connection	200ms	23	23.3	28.1	78.7	uA
	500ms	10	10.2	12.3	32.8	uA
	1s	5.6	5.9	7.1	17.6	uA
△Both Scan	Inquiry Scan and Page Scan	60.4	60.4	60.4	60.4	uA
Sleep		18				uA

* 1. Scan receives 11.25ms per 1.28s, Both Scan receives 22.5ms per 1.28s
2. bt 500ms sniff@TXpower10dBm: =38.6+18=56.6uA

4.3 Bluetooth RF

4.3.1 BLE RF

4.3.1.1 BLE Transmitter Characteristics

Table 4-7: BLE Transmitter Characteristics – 1Mbps

Parameter	Condition	Min	Typ	Max	Unit
Maximum RF transmit power			19		dBm
RF power control range		-20		19	dBm
Adjacent channel transmit power (@+19dBm)	F = F_0+2MHz		-27	-20	dBm
	F = F_0-2MHz		-27	-20	dBm
	F = F_0+3MHz		-31	-30	dBm
	F = F_0-3MHz		-31	-30	dBm
	F = F_0+>3MHz		-38	-30	dBm
	F = F_0->3MHz		-38	-30	dBm
Δf_{1avg} Maximum modulation		225	250	275	kHz
Δf_{2max} Minimum modulation		185	210		kHz
$\Delta f_{2avg}/\Delta f_{1avg}$		0.8	0.89		
ICFT		-150	±20	150	kHz
Drift rate		-20	±4	20	kHz/50us
Drift		-50	±4	50	kHz
Harmonic spur (@+19dBm transmit power)	Second harmonic		-50*		dBm
	Third harmonic		-40*		dBm

* With external π type matching network

Table 4-8: BLE Transmitter Characteristics – 2Mbps

Parameter	Condition	Min	Typ	Max	Unit
Maximum RF transmit power			19		dBm
RF power control range		-20		19	dBm
Adjacent channel transmit power (@+19dBm)	F = F_0+4MHz		-37	-20	dBm
	F = F_0-4MHz		-37	-20	dBm
	F = F_0+5MHz		-38	-20	dBm
	F = F_0-5MHz		-38	-20	dBm
	F = F_0+>5MHz		-42	-30	dBm
	F = F_0->5MHz		-42	-30	dBm
Δf_{1avg} Maximum modulation		450	500	550	kHz
Δf_{2max} Minimum modulation		370	420		kHz
$\Delta f_{2avg}/\Delta f_{1avg}$		0.8	0.89		
ICFT		-150	±20	150	kHz
Drift rate		-20	±4	20	kHz/50us
Drift		-50	±4	50	kHz
Harmonic Spur (@+19dBm transmit power)	Second harmonic		-50*		dBm
	Third harmonic		-40*		dBm

* With external π type matching network

4.3.1.2 BLE Receiver Characteristics

Table 4-9: BLE Receiver Characteristics – 1Mbps

Parameter	Condition	Min	Typ	Max	Unit
Frequency Range		2402		2480	MHz
Sensitivity with dirty transmit off@30.8% PER & 37bytes		/	-100	/	dBm
Sensitivity with dirty transmit on@30.8% PER & 37bytes		/	-99.3	/	dBm
Maximun received signal@30.8% PER & 37bytes		/	0	/	dBm
C/I Co-channel			7		dB
Adjacent channel selectivity C/I	F=F_0+1MHz		-10		dB
	F=F_0-1MHz		-7		dB
	F=F_0+2MHz		-43		dB
	F=F_0-2MHz		-40		dB
	F=F_0+3MHz		-50		dB
	F=F_0-3MHz		-40		dB
	F=F_0+>3MHz		<-40		dB
	F=F_0->3MHz		<-40		dB
	F=F_{image}(F_0-4MHz)		-24		dB
Intermodulation			-24		dBm
Out of band blocking performance	30MHz~2000MHz	-11	-11		dBm
	2000MHz~2400MHz	-25	-10		dBm
	2500MHz~3000MHz	-25	-10		dBm
	3000MHz~12.5GHz	-10	-10		dBm

Table 4-10: BLE Receiver Characteristics – 2Mbps

Parameter	Condition	Min	Typ	Max	Unit
Sensitivity with dirty transmit off@30.8% PER & 37bytes		/	-97	/	dBm
Sensitivity with dirty transmit on@30.8% PER & 37bytes		/	-96.5	/	dBm
Maximun received signal@30.8% PER & 37bytes		/	0	/	dBm
C/I co-channel			7		dB
Adjacent channel selectivity C/I	F = F_0+2MHz		-10		dB
	F = F_0-2MHz		-8		dB
	F = F_0+4MHz		-44		dB
	F = F_0-4MHz		-34		dB
	F = F_0+6MHz		-50		dB
	F = F_0-6MHz		-24		dB
	F = F_{image}(F_0-6MHz)		-24		dB
Intermodulation			-25		dBm
Out of band blocking performance	30MHz~2000MHz	-11	-11		dBm
	2000MHz~2400MHz	-25	-25		dBm
	2500MHz~3000MHz	-25	-25		dBm
	3000MHz~12.5GHz	-10	-10		dBm

4.3.2 Classic Bluetooth

4.3.2.1 Transmitter Characteristics

Table 4-11: Transmitter Characteristics – Basic Data Rate

Parameter	Condition	Min	Typ	Max	Unit
Maximum RF transmit power	RF output power	/	18	/	dBm
RF power control step		2	4	8	dB
Adjacent channel transmit power	F = F_0+2MHz	/	-37	-20	dBm
	F = F_0-2MHz	/	-37	-20	dBm
	F = F_0+3MHz	/	-41	-40	dBm
	F = F_0-3MHz	/	-41	-40	dBm
	F = F_0+>3MHz	/	-44	-40	dBm
	F = F_0->3MHz	/	-44	-40	dBm
Δf_{1avg} modulation		140	160	175	kHz
Δf_{2max} modulation		120	150	175	kHz
$\Delta f_{2avg}/\Delta f_{1avg}$		0.8	0.9	/	
ICFT		-75	0	75	kHz
Drift (1 slot packet)		-25	0	25	kHz
Drift (5 slot packet)		-40	0	40	kHz
Harmonic spur(@ +18dbm transimit power)	3G-20GHz	/	-35		dBm

Table 4-12: Transmitter Characteristics – Enhanced Data Rate

Parameter	Condition	Min	Typ	Max	Unit
Maximum RF transimit power	RF output power	/	13	/	dBm
DPSK Power - GFSK Power	2-DH5		0		dB
π/4 DQPSK max w_0		-10	0	10	kHz
π/4 DQPSK max w_i		-75	0	+75	kHz
π/4 DQPSK max $\|w_i + w_0\|$		-75	0	+75	kHz
8DPSK max w_0		-10	0	10	kHz
8DPSK max w_i		-75	0	+75	kHz
8DPSK max $\|w_i + w_0\|$		-75	0	+75	kHz
π/4 DQPSK modulation accuracy	RMS DEVM	/	6	20	%
	99% DEVM	/	11	30	%
	Peak DEVM	/	16	35	%
8DPSK modulation accuracy	RMS DEVM	/	6	13	%
	99% DEVM	/	11	20	%
	Peak DEVM	/	16	25	%
In-band spurious emissions	F=F_0+1MHz		-39	-26	dBm
	F=F_0-1MHz		-41	-26	dBm
	F=F_0+2MHz		-28	-20	dBm
	F=F_0-2MHz		-29	-20	dBm
	F=F_0+3MHz		-41	-40	dBm
	F=F_0-3MHz		-41	-40	dBm
	F=F_0+>3MHz		-41	-40	dBm
	F=F_0->3MHz		-41	-40	dBm
EDR differential phase encoding			99	100	%

4.3.2.2 Receiver Characteristics

Table 4-13: Receiver Characteristics – Basic Data Rate

Parameter	Condition	Min	Typ	Max	Unit
Sensitivity with dirty transmit off@0.1% BER		/	-96.3	/	dBm
Sensitivity with dirty transmit on@0.1% BER		/	-95	/	dBm
Maximum received signal@0.1% BER		0	/	/	dBm
C/I co-channel			10		dB
Adjacent channel selectivity C/I	F = F_0+1MHz		-13		dB
	F = F_0-1MHz		-10		dB
	F = F_0+2MHz		-42		dB
	F = F_0-2MHz		-43		dB
	F = F_0+3MHz		-48		dB
	F = F_0-3MHz		-45		dB
	F = F_{image}(F_0-5MHz)		-31		dB
Intermodulation			-23		dBm
Out of band blocking performance	30MHz~2000MHz	-10	-10		dBm
	2000MHz~2400MHz	-27	-10		dBm
	2500MHz~3000MHz	-27	-10		dBm
	3000MHz~12.5GHz	-10	-10		dBm

Table 4-14: Receiver Characteristics – Enhanced Data Rate-π/4 DQPSK

Parameter	Condition	Min	Typ	Max	Unit
Sensitivity with dirty transmit off@0.01% BER		/	-95.5	/	dBm
Sensitivity with dirty transmit on@0.01% BER		/	-95	/	dBm
Maximum received signal@0.01% BER		/	0	/	dBm
C/I co-channel			11		dB
Adjacent channel selectivity C/I	F = F_0+1MHz		-13		dB
	F = F_0-1MHz		-9		dB
	F = F_0+2MHz		-40		dB
	F = F_0-2MHz		-30		dB
	F = F_0+3MHz		-41		dB
	F = F_0-3MHz		-41		dB
	F = F_{image}(F_0-5MHz)		-30		dB

Table 4-15: Receiver Characteristics – Enhanced Data Rate-8DPSK

Parameter	Condition	Min	Typ	Max	Unit
Sensitivity with dirty transmit off@0.01% BER		/	-88.5	/	dBm
Sensitivity with dirty transmit on@0.01% BER		/	-87	/	dBm
Maximum received signal@0.01% BER		/	0	/	dBm
C/I co-channel			17		dB
Adjacent channel selectivity C/I	F = F_0+1MHz		-4		dB
	F = F_0-1MHz		-5		dB
	F = F_0+2MHz		-29		dB
	F = F_0-2MHz		-29		dB
	F = F_0+3MHz		-38		dB
	F = F_0-3MHz		-38		dB
	F = F_{image}(F_0-5MHz)		-28		dB

4.4 Audio Characteristics

Table 4-16: Audio ADC Characteristics

Analogue to Digital Converter under 3.3V

Parameter	Test Condition	Min	Typ	Max	Unit
Resolution		/	/	24	Bits
Sample Frequency		8	/	48	kHz
Analog Gain Range	6dB/Step	-6		18	dB
Input Resistance	Analog Gain = 0dB, @48kHz Sample Frequency	/	23	/	KΩ
Dynamic Range	1kHz -60dBFS Input, @48kHz Sample Frequency, Output A-Weighted	/	99	/	dB
Signal to Noise Ratio	1kHz Input, @48kHz Sample Frequency, Output A-Weighted	/		/	dB
Total Harmonic Distortion+Noise	Analog Gain = 0dB, 1kHz Input, @48kHz Sample Frequency	/	-76	/	dB

Table 4-17: Audio DAC Characteristics

Digital to Analogue Converter under 3.3V

Parameter	Test Condition	Min	Typ	Max	Unit
Resolution		/	/	24	Bits
Output Swing			1.1		Vrms
Sample Frequency		8	/	48	kHz
Total Harmonic Distortion+Noise	1kHz Output, 0dBFS, with 10kOhm Loading, @48kHz Sample Frequency, Output A-Weighted	/	-102	/	dB
Dynamic Range	1kHz Output, -60dBFS, with 10kOhm Loading, @48kHz Sample Frequency, Output A-Weighted	/	109	/	dB
Noise Floor		/	3.7	/	μV rms
Signal to Noise Ratio	1kHz Output, 0dBFS, with 10kOhm Loading, @48kHz Sample Frequency, Output A-Weighted	/	109	/	dB

4.5 Charger Characteristics

Table 4-18: Charger Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Charger Input Voltage	Vbus	4.6	5	5.5	V
BAT Leakage Current	Ileak		30		nA
Constant Charging Current	Icc	5		560	mA
Trickle Charging Current	Itri	0.5	56	56	mA
Battery Charge Full, Termination Current Ratio	Iend		10		%, of Icc
Battery Charge Full, Termination Voltage	Vcv		4.2	4.45	V
Fully-Charged Voltage Accuracy			±1.5		%, of Vcv
Trickle to Constant Charging Transition Threshold	Vcc		3		V
Re-Charge Threshold	Vrechg		Vcv-0.15		V
Over-Charge Protection	Vhigh		4.5		V

4.6 IO Drive Strength

Table 4-19: IO Drive Strength

DS0	DS1	Driving Capability
0	0	2mA
0	1	4mA
1	0	8mA
1	1	12mA

5 Packaging and Hardware

5.1 Pin Layout

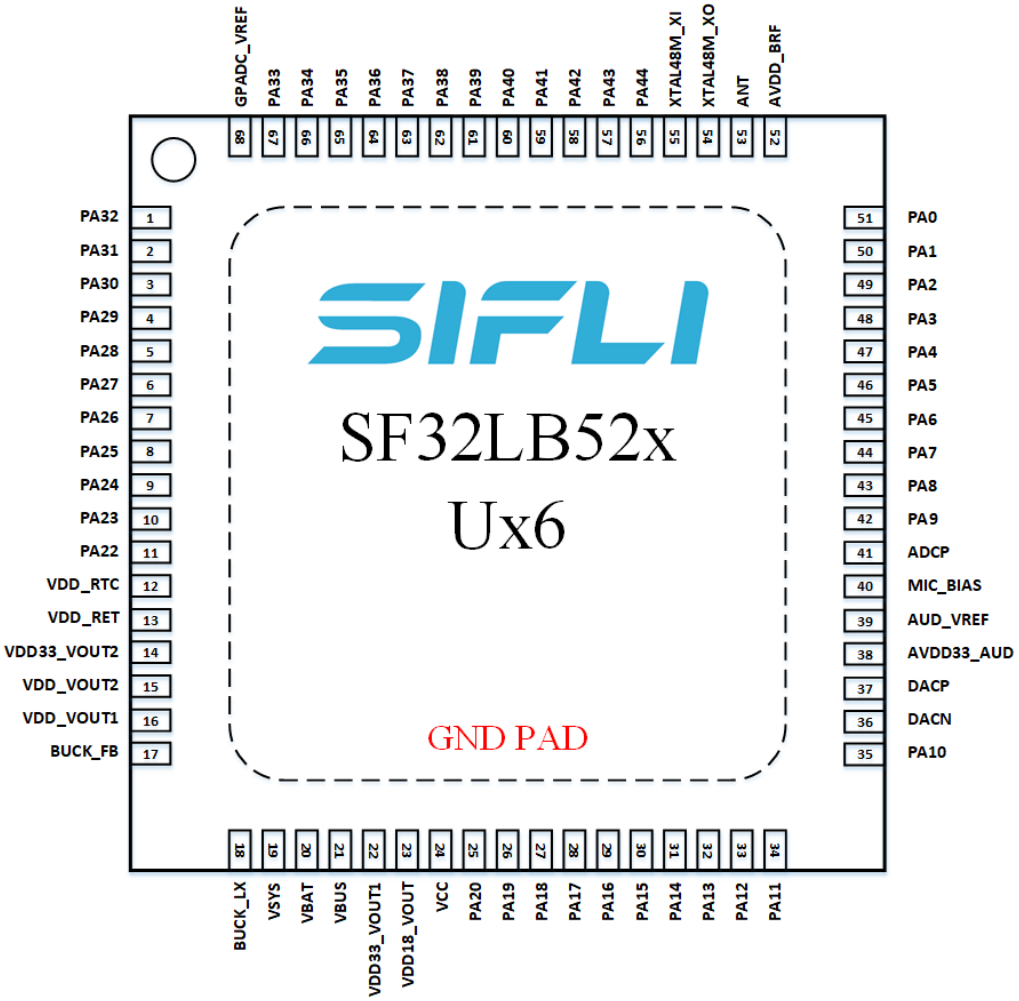


Figure 5-1: SF32LB52x Pin Layout

5.2 Pin Description

The pin types of this chip are shown in Table 5-1, and the following text will describe the big core domain GPIO and other dedicated pins respectively.

Table 5-1: Pin Types

Pin Type	Description
I/O	Digital input/output
I	Digital input
O	Digital output
A, I	Analog input
A, O	Analog output
A, I/O	Analog input/output
PWR	Power
GND	Ground

Notes:

- In low-power scenarios, floating inputs may cause the power consumption of digital I/Os with the input function turned on to rise, so such I/Os need to be configured with a determined voltage according to their function, either by connecting to I/Os with determined output voltages on other chips, or by connecting corresponding pull-up or pull-down resistors.

5.2.1 Big Core Domain GPIO (PA) List

Table 5-2: GPIO (PA) Pin List

Pin Number SF32LB52x (QFN68L)	Pin Name	Type	Sel #	Function
51	PA00	I/O	0	GPIO_A0
			1	LCDC1_SPI_RSTB
			4	PA_I2C_UART
			5	PA_TIM
			7	LCDC1_8080_RSTB
			Others	Reserved
50	PA01	I/O	0	GPIO_A1
			4	PA_I2C_UART
			5	PA_TIM
			Others	Reserved
49	PA02	I/O	0	GPIO_A2
			1	LCDC1_SPI_TE
			3	I2S1_MCLK
			4	PA_I2C_UART
			5	PA_TIM
			6	LCDC1_JDI_B2
			7	LCDC1_8080_TE
			Others	Reserved
48	PA03	I/O	0	GPIO_A3
			1	LCDC1_SPI_CS
			3	I2S1_SDO
			4	PA_I2C_UART
			5	PA_TIM
			6	LCDC1_JDI_B1
			7	LCDC1_8080_CS
			Others	Reserved
47	PA04	I/O	0	GPIO_A4
			1	LCDC1_SPI_CLK
			3	I2S1_SDI
			4	PA_I2C_UART
			5	PA_TIM
			6	LCDC1_JDI_G1
			7	LCDC1_8080_WR
			Others	Reserved
46	PA05	I/O	0	GPIO_A5
			1	LCDC1_SPI_DIO0
			3	I2S1_BCK
			4	PA_I2C_UART
			5	PA_TIM
			6	LCDC1_JDI_R1
			7	LCDC1_8080_RD
			Others	Reserved

Continued on the next page

Table 5-2: GPIO (PA) Pin List (continued)

Pin Number SF32LB52x (QFN68L)	Pin Name	Type	Sel #	Function
45	PA06	I/O	0	GPIO_A6
			1	LCDC1_SPI_DIO1
			3	I2S1_LRCK
			4	PA_I2C_UART
			5	PA_TIM
			6	LCDC1_JDI_HST
			7	LCDC1_8080_DC
			Others	Reserved
44	PA07	I/O	0	GPIO_A7
			1	LCDC1_SPI_DIO2
			3	PDM1_CLK
			4	PA_I2C_UART
			5	PA_TIM
			6	LCDC1_JDI_ENB
			7	LCDC1_8080_DIO0
			Others	Reserved
43	PA08	I/O	0	GPIO_A8
			1	LCDC1_SPI_DIO3
			3	PDM1_DATA
			4	PA_I2C_UART
			5	PA_TIM
			6	LCDC1_JDI_VST
			7	LCDC1_8080_DIO1
			Others	Reserved
42	PA09	I/O	0	GPIO_A9
			4	PA_I2C_UART
			5	PA_TIM
			Others	Reserved
35	PA10	I/O	0	GPIO_A10
			4	PA_I2C_UART
			5	PA_TIM
			Others	Reserved
34	PA11	I/O	0	GPIO_A11
			4	PA_I2C_UART
			5	PA_TIM
			Others	Reserved
33	PA12	I/O	0	GPIO_A12
			1	MPI2_CS
			2	SD1_DIO2
			4	PA_I2C_UART
			5	PA_TIM
			Others	Reserved

Continued on the next page

Table 5-2: GPIO (PA) Pin List (continued)

Pin Number SF32LB52x (QFN68L)	Pin Name	Type	Sel #	Function
32	PA13	I/O	0	GPIO_A13
			1	MPI2_DIO1
			2	SD1_DIO3
			4	PA_I2C_UART
			5	PA_TIM
			Others	Reserved
31	PA14	I/O	0	GPIO_A14
			1	MPI2_DIO2
			2	SD1_CLK
			4	PA_I2C_UART
			5	PA_TIM
			Others	Reserved
30	PA15	I/O	0	GPIO_A15
			1	MPI2_DIO0
			2	SD1_CMD
			4	PA_I2C_UART
			5	PA_TIM
			Others	Reserved
29	PA16	I/O	0	GPIO_A16
			1	MPI2_CLK
			2	SD1_DIO0
			4	PA_I2C_UART
			5	PA_TIM
			Others	Reserved
28	PA17	I/O	0	GPIO_A17
			1	MPI2_DIO3
			2	SD1_DIO1
			4	PA_I2C_UART
			5	PA_TIM
			Others	Reserved
27	PA18	I/O	0	GPIO_A18
			2	SWDIO
			4	PA_I2C_UART
			5	PA_TIM
			Others	Reserved
26	PA19	I/O	0	GPIO_A19
			2	SWCLK
			4	PA_I2C_UART
			5	PA_TIM
			Others	Reserved

Continued on the next page

Table 5-2: GPIO (PA) Pin List (continued)

Pin Number SF32LB52x (QFN68L)	Pin Name	Type	Sel #	Function
25	PA20	I/O	0	GPIO_A20
			4	PA_I2C_UART
			5	PA_TIM
			Others	Reserved
-	PA21	I/O	0	GPIO_A21
			4	PA_I2C_UART
			5	PA_TIM
			Others	Reserved
11	PA22	I/O	0	GPIO_A22
			3	PDM1_CLK
			4	PA_I2C_UART
			5	PA_TIM
			8	#XTAL32K_XI
			Others	Reserved
10	PA23	I/O	0	GPIO_A23
			3	PDM1_DATA
			4	PA_I2C_UART
			5	PA_TIM
			8	#XTAL32K_XO
			Others	Reserved
9	PA24	I/O	0	GPIO_A24
			2	SPI1_DIO
			3	I2S1_MCLK
			4	PA_I2C_UART
			5	PA_TIM
			8	#WKUP_PIN0
			Others	Reserved
8	PA25	I/O	0	GPIO_A25
			2	SPI1_DI
			3	I2S1_SDO
			4	PA_I2C_UART
			5	PA_TIM
			7	#XTAL32K_EXT
			8	#WKUP_PIN1
			Others	Reserved
7	PA26	I/O	0	GPIO_A26
			4	PA_I2C_UART
			5	PA_TIM
			8	#WKUP_PIN2
			Others	Reserved

Continued on the next page

Table 5-2: GPIO (PA) Pin List (continued)

Pin Number SF32LB52x (QFN68L)	Pin Name	Type	Sel #	Function
6	PA27	I/O	0	GPIO_A27
			4	PA_I2C_UART
			5	PA_TIM
			8	#WKUP_PIN3
			Others	Reserved
5	PA28	I/O	0	GPIO_A28
			2	SPI1_CLK
			3	I2S1_SDI
			4	PA_I2C_UART
			5	PA_TIM
			7	#GPADC_CH0
			Others	Reserved
4	PA29	I/O	0	GPIO_A29
			2	SPI1_CS
			3	I2S1_BCK
			4	PA_I2C_UART
			5	PA_TIM
			7	#GPADC_CH1
			Others	Reserved
3	PA30	I/O	0	GPIO_A30
			2	#EFUSE_PWR
			3	I2S1_LRCK
			4	PA_I2C_UART
			5	PA_TIM
			7	#GPADC_CH2
			Others	Reserved
2	PA31	I/O	0	GPIO_A31
			4	PA_I2C_UART
			5	PA_TIM
			7	#GPADC_CH3
			Others	Reserved
1	PA32	I/O	0	GPIO_A32
			4	PA_I2C_UART
			5	PA_TIM
			7	#GPADC_CH4
			Others	Reserved

Continued on the next page

Table 5-2: GPIO (PA) Pin List (continued)

Pin Number SF32LB52x (QFN68L)	Pin Name	Type	Sel #	Function
67	PA33	I/O	0	GPIO_A33
			4	PA_I2C_UART
			5	PA_TIM
			7	#GPADC_CH5
			Others	Reserved
66	PA34	I/O	0	GPIO_A34
			4	PA_I2C_UART
			5	PA_TIM
			7	#GPADC_CH6
			8	#WKUP_PIN10
			Others	Reserved
65	PA35	I/O	0	GPIO_A35
			2	#USB11_DP
			4	PA_I2C_UART
			5	PA_TIM
			8	#WKUP_PIN11
			Others	Reserved
64	PA36	I/O	0	GPIO_A36
			2	#USB11_DM
			4	PA_I2C_UART
			5	PA_TIM
			8	#WKUP_PIN12
			Others	Reserved
63	PA37	I/O	0	GPIO_A37
			2	SPI2_DIO
			4	PA_I2C_UART
			5	PA_TIM
			7	LCDC1_8080_DIO2
			8	#WKUP_PIN13
			Others	Reserved
62	PA38	I/O	0	GPIO_A38
			2	SPI2_DI
			4	PA_I2C_UART
			5	PA_TIM
			8	#WKUP_PIN14
			Others	Reserved

Continued on the next page

Table 5-2: GPIO (PA) Pin List (continued)

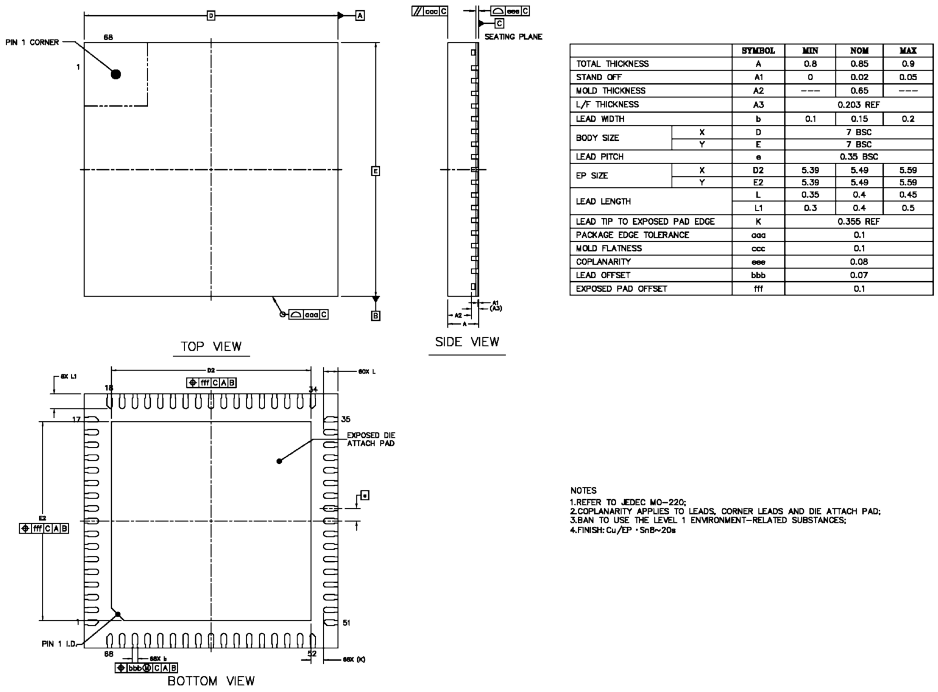
Pin Number SF32LB52x (QFN68L)	Pin Name	Type	Sel #	Function
61	PA39	I/O	0	GPIO_A39
			2	SPI2_CLK
			4	PA_I2C_UART
			5	PA_TIM
			6	LCDC1_JDI_VCK
			7	LCDC1_8080_DIO3
			8	#WKUP_PIN15
			Others	Reserved
60	PA40	I/O	0	GPIO_A40
			2	SPI2_CS
			4	PA_I2C_UART
			5	PA_TIM
			6	LCDC1_JDI_XRST
			7	LCDC1_8080_DIO4
			8	#WKUP_PIN16
			Others	Reserved
59	PA41	I/O	0	GPIO_A41
			4	PA_I2C_UART
			5	PA_TIM
			6	LCDC1_JDI_HCK
			7	LCDC1_8080_DIO5
			8	#WKUP_PIN17
			Others	Reserved
58	PA42	I/O	0	GPIO_A42
			4	PA_I2C_UART
			5	PA_TIM
			6	LCDC1_JDI_R2
			7	LCDC1_8080_DIO6
			8	#WKUP_PIN18
			Others	Reserved
57	PA43	I/O	0	GPIO_A43
			4	PA_I2C_UART
			5	PA_TIM
			6	LCDC1_JDI_G2
			7	LCDC1_8080_DIO7
			8	#WKUP_PIN19
			Others	Reserved
56	PA44	I/O	0	GPIO_A44
			4	PA_I2C_UART
			5	PA_TIM
			8	#WKUP_PIN20
			Others	Reserved

5.2.2 List of Dedicated Pins (Power, RF, Analog, I/O)

Table 5-3: List of Dedicated Pins (Power, RF, Analog, I/O)

Pin Number SF32LB52x (QFN68L)	Pin Name	Type	Description
21	VBUS	PWR	VBUS input
20	VBAT	PWR	VBAT output
19	VSYS	PWR	VSYS output
18	BUCK_LX	A,I/O	Buck inductive switch
17	BUCK_FB	PWR	Buck output
16	VDD_VOUT1	PWR	Internal LDO1 output
15	VDD_VOUT2	PWR	Internal LDO2 output
13	VDD_RET	PWR	RET LDO output
12	VDD_RTC	PWR	RTC LDO output
24	VCC	PWR	System power input
23	VDD18_VOUT	PWR	SIP power*
22	VDD33_VOUT1	PWR	3.3V LDO output1
14	VDD33_VOUT2	PWR	3.3V LDO output2
68	GPADC_VREF	A,I	GPADC VREF input
55	XTAL48M_XI	A,I	48MHz crystal port
54	XTAL48M_XO	A,O	48MHz crystal port
53	BRF_ANT	A,I/O	Antenna interface
52	AVDD_BRF	PWR	RF power input
41	ADCP	A,I	Audio ADC input
40	MIC_BIAS	PWR	MIC power output
39	AUD_VREF	A,I	Audio reference voltage input
38	AVDD33_AUD	PWR	Audio power input
37	DACP	A,O	Audio DAC output
36	DACN	A,O	Audio DAC output
69	EPAD	GND	Ground

5.3 Package Dimensions



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	----	0.65	----
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.1	0.15	0.2
BODY SIZE	X	D		7 BSC	
	Y	E		7 BSC	
LEAD PITCH		e		0.35 BSC	
EP SIZE	X	D2	5.39	5.49	5.59
	Y	E2	5.39	5.49	5.59
LEAD LENGTH		L	0.35	0.4	0.45
		L1	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.355 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES;
4.FINISH: Cu/EP · SnB~20u

Figure 5-2: QFN68L Package Dimensions

5.4 Carrier Tape Dimensions

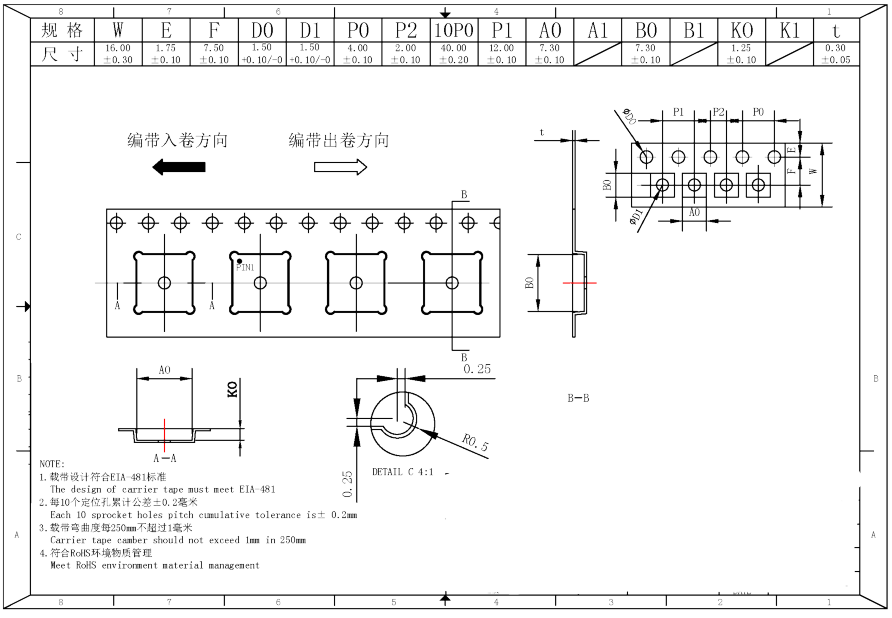
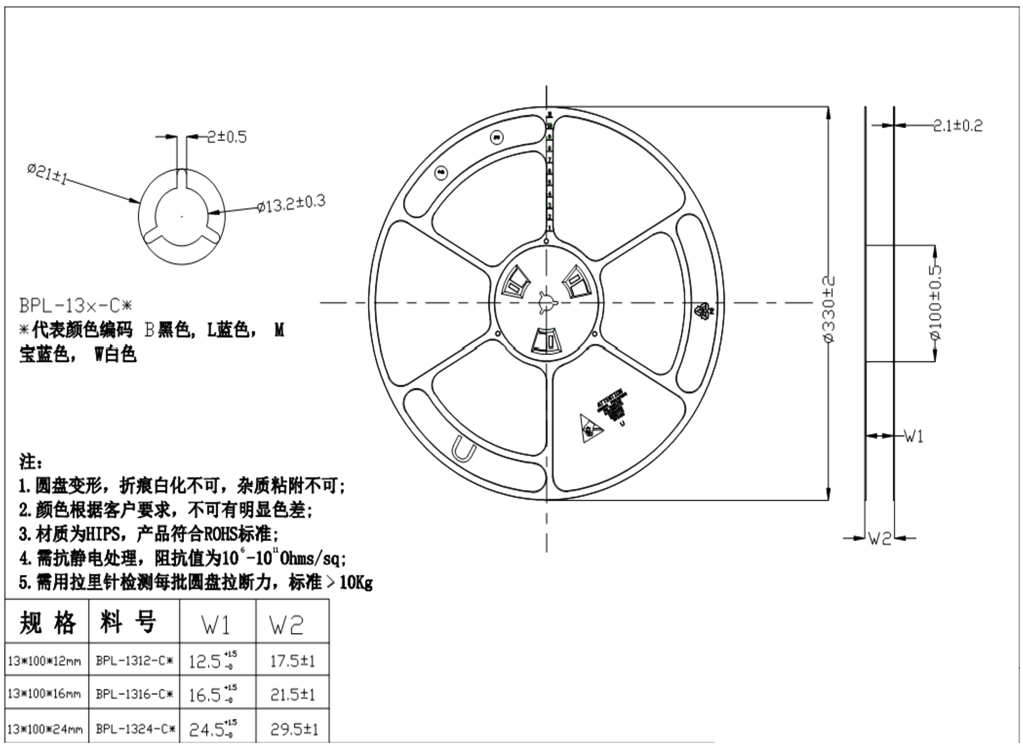


Figure 5-3: Carrier Tape Dimensions

5.5 Reel Dimensions



规 格	料 号	W1	W2
13*100*12mm	BPL-1312-C*	12.5 +1.5 +0	17.5±1
13*100*16mm	BPL-1316-C*	16.5 +1.5 +0	21.5±1
13*100*24mm	BPL-1324-C*	24.5 +1.5 +0	29.5±1

Figure 5-4: Reel Dimensions

5.6 Graded Reflow Soldering

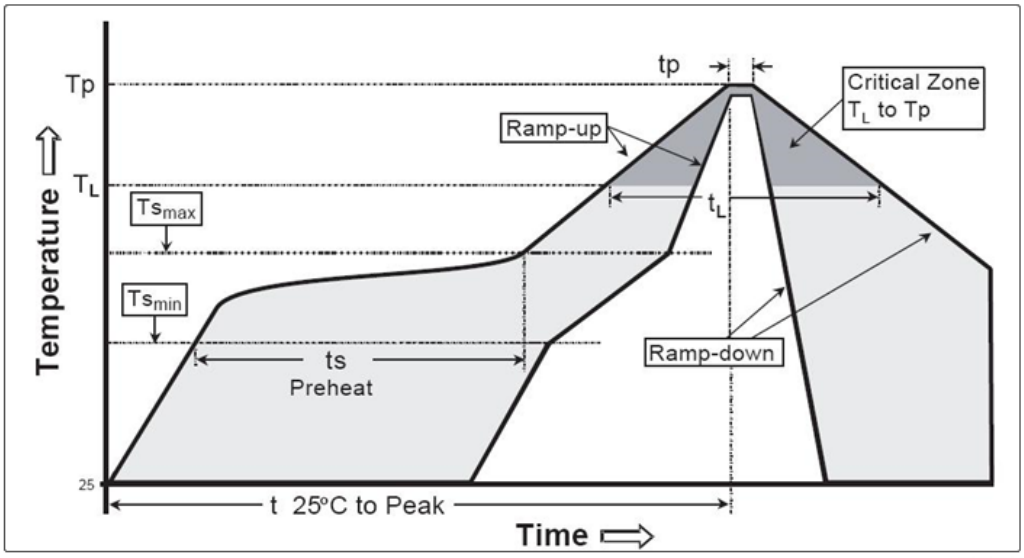


Figure 5-5: Graded Reflow Soldering

Table 5-4: Comparison Table of Graded Reflow Soldering

Item	Tin-lead Process	Lead-free Process
Average Ramp-up Rate (Ts_{max} to T_p)	Max. 3°C/s	Max. 3°C/s
Preheat Temperature Min.(Ts_{min}) Preheat Temperature Max. (Ts_{max}) Preheat Time (Ts_{min} to Ts_{max})	100°C 100°C 60-120s	150°C 200°C 60-180s
Temperature_Time Maintained above (T_L) Time_Time Maintained above (t_L)	183°C 60-150s	217°C 60-150s
Peak Temperature （T_p）	225+0/-5°C	240+0/-5°C
Time of Peak Temperature （tp）	10-30s	20-40s
Ramp-down Rate	Max. 6°C/s	Max. 6°C/s
Time_25°C to Peak Temperature (t)	Max. 6 mins	Max. 8 mins

Table 5-5: Peak Reflow Temperature – Lead-free

Packaging Thickness	Volume (mm^3) <350	Volume (mm^3) ≥350
<2.5mm	240 + 0/-5°C	225 + 0/-5°C
≥2.5mm	225 + 0/-5°C	225 + 0/-5°C

Table 5-6: Graded Reflow Temperature – Lead-free

Packaging Thickness	Volume (mm^3) <350	Volume (mm^3) 350-2000	Volume (mm^3) >2000
<1.6mm	260 + 0 °C	260 + 0 °C	260 + 0 °C
1.6mm –2.5mm	260 + 0 °C	250 + 0 °C	245 + 0 °C
≥2.5mm	250 + 0 °C	245 + 0 °C	245 + 0 °C

5.7 Ordering Information

Table 5-7: Ordering Information

Part No.	Package Size	SiP Specification	Pack Quantity (PCS)
SF32LB520U36	QFN68L: 7×7×0.85mm-0.35	8Mb NOR Flash	3000
SF32LB523UB6	QFN68L: 7×7×0.85mm-0.35	32Mb OPI-pSRAM	3000
SF32LB525UC6	QFN68L: 7×7×0.85mm-0.35	64Mb OPI-pSRAM	3000
SF32LB527UD6	QFN68L: 7×7×0.85mm-0.35	128Mb OPI-pSRAM	3000

Address: 419-13, Block B, Science and Technology Headquarters Building, No.320 Pubin Road, Nanjing Area, Jiangsu Free Trade Zone, P. R. China 200131

Email: sales@sifli.com