SF32LB55x

big.LITTLE Arm Cortex-M33 STAR-MC1@240MHz/48MHz
2.5D GPU, 1.4MB SRAM, BLE5.2, NN Matrix Accelerator

Product Brief

Key Features

- Bluetooth MCU with dual-core Arm Cortex-M33 STAR-MC1, up to 240MHz/48MHz, 432 DMIPS, 1158 CoreMark, no-compromise experience with both feature-rich graphical HMI and ultra-low power
- ePicasso™ 2.5D GPU supports rotation, scaling, and alpha blending with hardware acceleration; eZip™ lossless graphics decompression; LCD controller supports 8080/QSPI/MIPI- DSI
- Bluetooth Low Energy 5.2, world-leading -100dBm sensitivity and Rx power of 2mA
- 1.4MB on-chip SRAM, and interfaces for NOR, NAND, eMMC, QSPI/OPI-PSRAM
- Multiple package options with up to 119 GPIOs to support a wide variety of peripherals

Applications

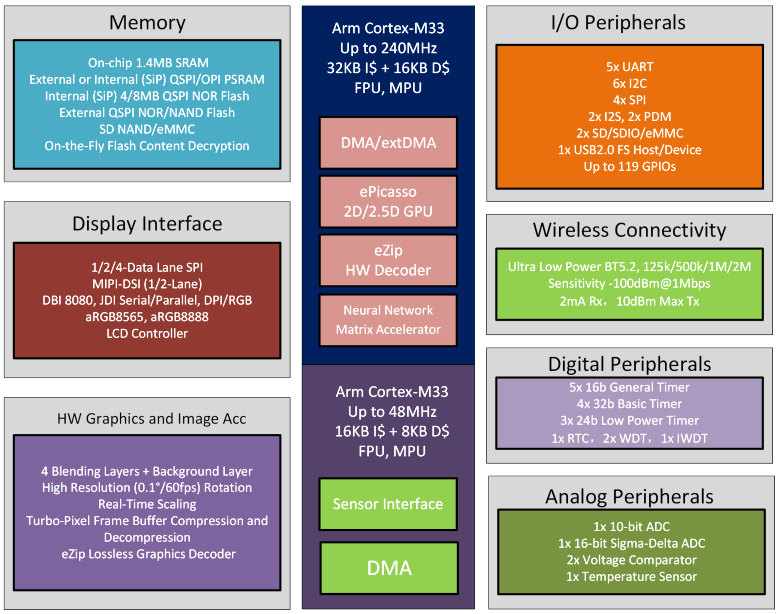
- Smart watches and bands
- Activity and fitness monitors
- Location and motion trackers
- Cost-effective display solution
- Graphical HMI device
- Industrial sensor control
- Smart home appliances
- Smart door lock
- Voice and gesture remotes
- Smart stylus pen
- Low-power sensor hub

SF32LB55x is a family of highly integrated high-performance SoC MCUs for ultra-low power AIoT scenarios. It adopts a big.LITTLE architecture based on dual Arm Cortex-M33 STAR-MC1 processors, and is embedded with a best-in-class 2.5D GPU, a neural network matrix accelerator, and BLE5.2. SF32LB55x can be used for a wide variety of applications such as smart wearables, smart HMI devices, and smart home appliances, etc.

The high performance application processor can operate at up to 240MHz, delivering up to 965 CoreMark. The low power processor can operate at up to 48MHz for 193 CoreMark and serves as both sensor hub and Bluetooth controller at high energy efficiency of 2.93uA/CoreMark. This architecture delivers no-compromise user experience of both high performance computing required for rich HMI and always-on ultra-low power sensor control and wireless connectivity.

The ePicasso™ 2.5D GPU supports hardware accelerated rotation and scaling as well as 4-layer alpha blending, and can be concatenated with eZip™ lossless graphics decompression engine without intermediate frame buffer. The LCD controller can support 8080/QSPI/MIPI-DSI interface at a full-screen refresh frame rate up to 60fps.

The world-class BLE5.2 transceiver supports 125K/500K/1M/2Mbps modes with a maximum Tx power of 10dBm. The receiver consumes peak current of 2mA@3.3V and has a sensitivity at -100dBm (1Mbps).



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CPU and Memory

- High Performance Application Processor
  - Arm Cortex-M33 STAR-MC1, FPU, MPU
  - Clock up to 240MHz, adjustable
  - Up to 360DMIPS, 965 EEMBC CoreMark
  - I/D-Cache: 32KB (2-way)+16KB (4-way)
  - SRAM: 1088KB (64 KB retention SRAM)
  - CoreMark power: 34μA/MHz @3.3V
- Ultra Low-Power Processor
  - Arm Cortex-M33 STAR-MC1, FPU, MPU
  - Clock up to 48MHz, adjustable
  - Max. 72DMIPS, 193 EEMBC CoreMark
  - I/D-Cache: 16KB (2-way)+8KB (4-way)
  - SRAM: 224KB (all retention SRAM)
  - CoreMark power: 11.8μA/MHz @3.3V

Wireless Connectivity

- BLE 5.2: 125Kbps, 500Kbps, 1Mbps, 2Mbps
- Sensitivity: -100dBm at 1Mbps mode
- Maximum Tx power: 10dBm
- Rx peak current: 2.0mA@3.3V

Graphics and Display

- 2.5D Graphics Engine – ePicasso™
  - 4-layer alpha blending + 1 background layer
  - Hardware-accelerated rotation, scaling, mirroring
  - Maximum resolution up to 640×640
  - aRGB8565, aRGB888
- Lossless Decompression Accelerator – eZip™
  - Hardware lossless graphics decompression
  - Concatenated operation with ePicasso™
- LCD Controller
  - Support 8080, SPI, Dual-SPI, Quad-SPI, MIPI-DSI
  - 2-layer alpha blending + 1 background layer
  - TurboPixel™ FB compression and decompression
  - aRGB8565, aRGB8888
  - Dual LCD controllers for always-on display

Neural Network Matrix Accelerator

- Matrix convolution acceleration for TinyML scenarios
- Processing power up to 1.92GOPS
- Energy efficiency up to 5.73TOPS/W

Memory Interface

- 4×QSPI, for NOR, NAND, QSPI-PSRAM
- 1×OPI-PSRAM at up to 120MHz in DDR mode
- 2×SD/SDIO/eMMC, one 4-bit and one 8-bit, SD3.0, SDIO3.0 and eMMC4.51

Others

- DMA
  - General DMA: high efficiency data transfer between internal memory and peripherals
  - extDMA: high efficiency data transfer between internal memory and external memory
- Security
  - AES, CRC hardware accelerator
  - True random number generator (TRNG)
  - PSA Certified Level 1
- Timers
  - 5×16b GPTIM, 4×32b BTIM, 3×24b LPTIM
  - 1×RTC
  - 2×24b WDT，1×IWDT
- Analog Peripherals
  - 1×10-bit general purpose SAR ADC, 8 channels
  - 1×16-bit Sigma-Delta ADC, 5 channels
  - 1×Temperature sensor
  - 2×Low power voltage comparator
- I/O Peripherals
  - 5×UART, 6× I^2C, 4×SPI
  - 2× I^2S, 2× PDM
  - 1×USB2.0 FS Host/Device
  - Peripheral Task Controller (PTC)
- Power Management
  - Power supply: 1.7 to 3.6V, -40 to 85°C
  - Two high-efficiency bucks and low-power LDO
  - Sleep current with RTC wake-up: 600nA
  - Sleep current with pin wake-up: 280nA

Package

- BGA169, 119 (HP71+LP48) GPIOs
- BGA145, 95 (HP55+LP40) GPIOs
- BGA125, 84 (HP52+LP32) GPIOs
- QFN68L, 49 (HP28+LP21) GPIOs