思 澈 科 技

SF32LB57x

用户手册

V0.1

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更新历史

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草稿	0.0.0 ~0.9.9	初稿，非正式发布，信息为初步数据，反映量产前产品的规格与性能，不能保证准确性，随时可能更改，思澈科技将不会主动通知
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产品概述

SF32LB57x 是一系列用于超低功耗人工智能物联网（AIoT）场景下的高集成度、高性能 MCU 芯片。芯片采用了基于 Arm Cortex-M33 STAR-MC1 处理器的多核架构，集成高性能 2D/2.5D 图形引擎，双模蓝牙 6.3，以及音频 codec，可广泛用于可穿戴电子设备、便携式智能移动终端、智能家居等各种应用场景。

芯片中主系统配备两个 Cortex-M33 STAR-MC1 处理器，最高工作频率达 240MHz，双大核性能达 1968 CoreMark，支持动态频率功耗调节，功耗效率最高可达 5uA/CoreMark，在用于提供丰富应用和流畅人机交互所需的高性能算力的同时，还可作为 Sensor Hub 控制多种传感器以及运行蓝牙协议栈，从而很好地兼顾流畅人机交互所需的高计算性能与长待机时间所需的超低功耗运行之间的平衡关系。

芯片内集成 2D/2.5D GPU，主频最高达到 240MHz，支持多图层叠加，alpha 混叠，硬件加速的实时旋转/缩放/投影变换，以及各种常用图形格式转换。支持硬件加速无损压缩图形解压缩，支持原生动画，可以大幅提高带宽利用率，降低存储成本。芯片内置 LCD 控制器，支持 8080/QSPI/RGB/EPD/JDI 等多种接口，可不依赖于 CPU 自主实现最高 60fps 的全屏刷新帧率，并支持低功耗息屏常显。

集成世界水平的双模蓝牙 6.3 收发机，经典蓝牙 EDR2 模式最高发射功率 13dBm，接收峰值功耗低至 2.0mA@3.8V，低功耗蓝牙接收灵敏度达到-100dBm（1Mbps），经典蓝牙 EDR2 模式灵敏度-95dBm。集成高保真音频 ADC 和 DAC，支持蓝牙通话和连接耳机 MP3 播放。

功能框图

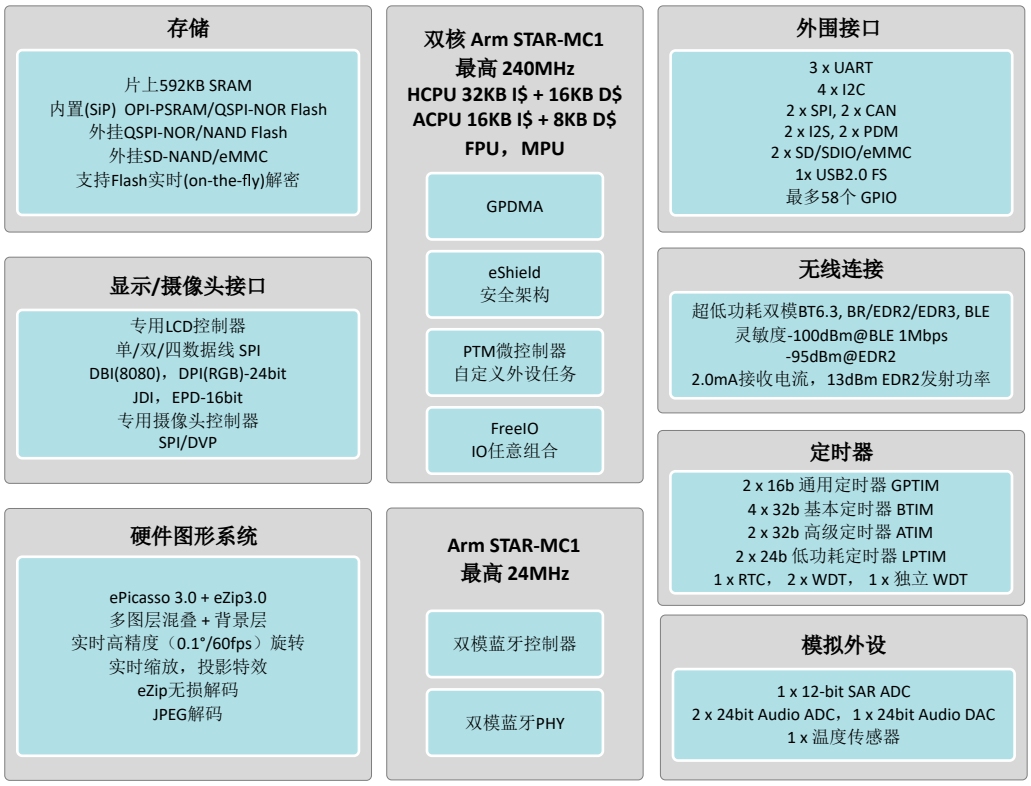


图 0-1: 功能框图

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产品特性

CPU 与内存

- 高性能系统/双性能核（HPSYS）
  - 处理器：Dual Arm Cortex-M33 STAR-MC1
  - 主频：最高 240MHz，可调节，1968 CoreMark
    - HCPU:32KB(2-way) I$ + 16KB(4-way) D$
    - ACPU:16KB(2-way) I$ + 8KB(4-way) D$
  - SRAM：512KB（全部为 Retention SRAM）
  - CoreMark 功耗效率：低至 23uA/MHz @3.8V
  - 单精度浮点运算单元（FPU）
  - 内存保护单元（MPU）
- 低功耗系统/能效核（LPSYS）
  - 处理器：Arm Cortex-M33 STAR-MC1
  - 主频：最高 24MHz，可调节
  - SRAM：80KB（全部为 Retention SRAM）

无线连接

- 双模蓝牙 6.3，支持 BLE Audio，支持 LE LR
- 灵敏度：-100dBm（BLE/1Mbps），-107.5dBm（BLE/125Kbps），-96dBm（BR），-95dBm（EDR2）
- 最大发射功率：13dBm（EDR2/3），17dBm（BR/BLE）
- 接收机峰值功耗（BR）：2.0mA@3.8V

音频

- 1× 高保真 24-bit 音频 DAC
  - Noise floor: 3.7uVrms
  - SNR(with 10kohm load and A-Weighted): 109dB
  - Sample rate: 8k/ 16k/ 11.025k/ 22.05k/ 24k/ 32k/ 44.1k/ 48k/ 88.2k/ 96kHz
  - 支持 192 级数字音量，具有过零检测功能
- 2× 高保真 24-bit 音频 ADC
  - SNR(A-Weighted): 97dB
  - Sample rate: 8k/ 11.025k/ 12k/ 16k/ 22.05k/ 24k/ 32k/ 44.1k/ 48k/ 88.2k/ 96kHz
  - 数字高通滤波器可用于消除 ADC 的直流偏置
  - 支持单端和全差分输入麦克风
  - Micbias LDO，输出电压为 1.4V~2.8V，输出电流为 0~2mA

图形显示

- 2D/2.5D 图形引擎—ePicasso™3.0
  - 支持硬件加速的旋转、缩放，投影和镜像
  - 最大解析度 2048×2048
  - 支持 RGB 色彩格式包括 RGB888，RGB565，aRGB8888，aRGB8565
  - 支持其他色彩格式 L8/4，G8/4/2，A8/4/2，YUV
  - 支持多种 alpha 混叠方式
- 通用解压缩加速器—eZip™3.0
  - 支持无损压缩 eZip 格式和 eZip-A 动画
  - 支持有损压缩 JPEG 格式图片和 MJPEG 动画
  - 支持与 ePicasso™3.0 联动，无需中间缓存
- LCD 控制器
  - 支持 8080，SPI/Dual-SPI/Quad-SPI，DPI/RGB，JDI，8/16b-EPD（电子纸）显示接口
- 摄像头控制器 DCMI
  - 支持 DVP，SPI/Dual-SPI/Quad-SPI，摄像头接口

存储接口

- 支持合封（SiP）NOR-Flash，接口最高频率 104MHz
- 支持合封（SiP）OPI-PSRAM，接口最高频率 156MHz
- 3×MPI(QSPI)，支持 NOR、NAND、QPI-PSRAM
- 2×SD/SDIO，支持 SD3.0，SDIO3.0，eMMC

DMA

- GPDMA：通用高效率 DMA，支持链表模式

安全

- AES/HASH/CRC 加速器
- 真随机数发生器（TRNG）
- eShield 安全架构
- PSA Certified Level 1 认证

定时器

- 2×16b GPTIM，4×32b BTIM，2×32b ATIM
- 2×24b LPTIM，1×PWM
- 1×RTC
- 2× 看门狗 24b WDT，1× 独立看门狗 IWDT

模拟

- 1×12-bit 通用 SAR ADC，共 12 通道
- 1× 片上温度传感器

连接外设

- 最多 58 个 GPIO + 6 个 GPO 或 MPI 接口 IO
- FreeIO 功能，支持 GPIO 灵活配置
- 3×UART，4× I^2C，2×SPI
- 2× I^2S，2× PDM

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- 1×USB2.0 FS，2×CAN
- 外设任务控制器（PTM）

电源管理

- 内置高效率 Buck 及低功耗 LDO
- 提供两路对外 3.3V 供电，每路最大电流 150mA
- 休眠功耗：2.8uA@3.8V 电池供电
- 内置 400mA 锂电池线性充电器，支持 4.2V-4.45V 满电电压
- VBAT 电压范围：3.0V-4.7V
- VBUS 电压范围：4.5V-5.5V

其它

- 工作温度：-40 到 85°C
- 封装：
  - QFN68H，7mm×7mm，锂电池供电，46 个 GPIO
  - QFN80H，8mm×8mm，锂电池供电，58 个 GPIO
  - BGA112，5.4mm×4.4mm，锂电池供电，最多 58 个 GPIO + 6 个 GPO 或 MPI 接口 IO

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应用场景

智能穿戴

- 高端智能手表
- 智能手环
- 可穿戴医疗器材
- 健身器材

工业

- 高性价比显示方案
- 图形化人机交互设备
- 工业传感器控制中心
- 工业设备监测
- 工业仪器仪表

车载

- 电动车中控设备
- 汽车钥匙
- 穿戴式汽车遥控设备

家庭自动化

- 智能家居中控
- 中小型智能家电
- 智能门锁

智能设备

- 智能录音卡
- 智能蓝牙对讲机
- 电子纸阅读器
- 电子相框

通用

- 低功耗传感器中心
- 蓝牙 mesh

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1 芯片总览

1.1 系统架构

SF32LB57x 是一系列用于超低功耗人工智能物联网（AIoT）场景下的高集成度、高性能 MCU 芯片。芯片采用了基于 Arm Cortex-M33 STAR-MC1 处理器的大小核架构，其中：

- 高性能系统/双性能核（HPSYS）：HCPU 配备 32KB 指令缓存（I-Cache）和 16KB 数据缓存（D-Cache），ACPU 配备 16KB 指令缓存（I-Cache）和 8KB 数据缓存（D-Cache），512KB SRAM（全部为 Retention SRAM）。最高主频 240MHz，可动态切换基础工作模式和增强工作模式，高效访问片内和片外存储。作为系统主控，增强工作模式主要用于系统控制、人机交互、高性能计算等；同时作为低功耗传感器中心，基础工作模式可用于低功耗场景下的各种数据采集和处理。
- 低功耗系统/能效核（LPSYS）：最高主频 24MHz，80KB SRAM（全部为 Retention SRAM），用于低功耗蓝牙的传输控制和基本数据处理。

1.2 Cortex-M33 STAR-MC1 “星辰”处理器

Cortex-M33 STAR-MC1 处理器是安谋中国（Arm China）推出的“星辰”系列产品的第一款处理器，该处理器继承了 Cortex-M33 的主要特点，支持现有的 Arm v8-M 架构的全部功能，具有有序（in order）三级流水线，可显著降低系统功耗，具有部分双发射 16 位指令能力，并进一步改进了协处理器接口，增加了对缓存（Cache）的支持。

Cortex-M33 STAR-MC1 性能达到 1.5DMIPS/MHz 和 4.02Coremark/MHz，与上一代同档位 Arm 处理器相比，在相同主频下，Cortex-M33 STAR-MC1 的性能提升 20%。

Cortex-M33 STAR-MC1 提供了协处理器（Coprocessor）接口，以便根据不同场景需求进一步提高定制计算的能力。通过 MCR（Move from Coprocessor to Register）和 MRC（Move from Register to Coprocessor）指令，可以在 Cortex-M33 STAR-MC1 和协处理器之间转移寄存器数据和计算结果数据，非常适合所需数据量不大、计算复杂但相对碎片化、延迟较小的运算。在协处理器计算的同时，Cortex-M33 STAR-MC1 处理器仍然可以并行执行其它指令，从而明显提高执行效率。

此外，该处理器还支持数字信号处理（DSP）指令集和浮点数运算单元（FPU）。

Cortex-M33 STAR-MC1 引入了紧耦合内存（TCM）和缓存（Cache）技术，增强了各种不同特点的内置和外置存储系统的使用灵活性，确保在各种不同场景下处理器响应的实时性和计算效率。

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1.3 高性能（双性能核）系统（HPSYS）

1.3.1 总线架构

HPSYS 内部提供了基于 AHB 协议的总线矩阵，支持多个主设备并行访问多个从设备地址空间。

如图1-1所示，总线主设备位于上侧，从设备地址空间位于右侧，交叉处的黑色圆点代表总线连通。

HCPU 与 DMAC1 能够访问 HPSYS 的所有地址空间。

DTCM 与 HPSYS_RAM0 共享 128KB 地址空间，可由 HCPU 及其它主设备访问。

HP_PERI 包含 APB 相关外设以及 AHB 相关外设，可由 HCPU、DMAC1 以及 PTM1 访问。

多个主设备同时访问同一个从设备地址空间时，基于轮询仲裁原则决定访问次序。

图中边框不相连的多个主设备同时访问不同从设备地址空间时，互相不受影响。边框相连的两个主设备同时发起访问时，基于固定优先级或轮询仲裁原则决定访问次序。

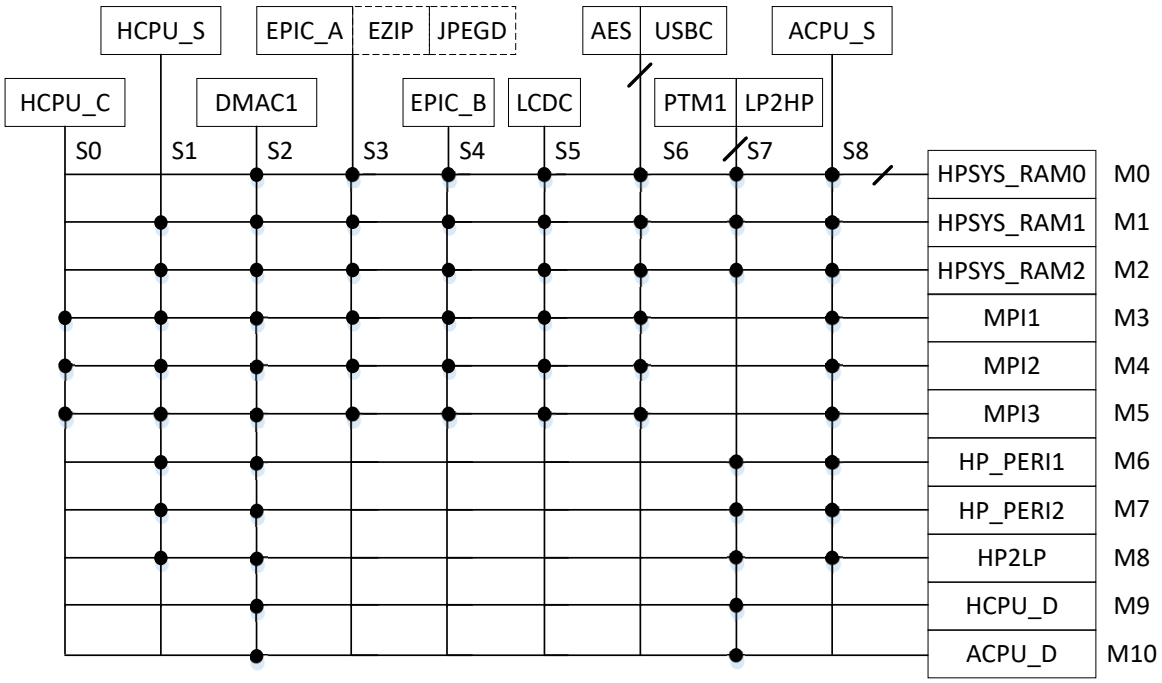


图 1-1: 高性能系统总线架构

1.3.2 存储器类型

1.3.2.1 Cache

HCPU 配置有 32KB 2-way I-Cache（一级指令缓存）和 16KB 4-way D-Cache（一级数据缓存），可大幅提升 XIP 时 CPU 执行效率。软件需合理配置 MPU（Memory Protection Unit）设置 cache 地址段和非 cache 地址段，兼顾效率和易用性。

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1.3.2.2 TCM

HCPU 配置有 128KB zero-wait-cycle D-TCM，地址空间为 0x2000_0000-0x2001_FFFF，可用于放置对实时性要求较高的代码和数据。该 TCM memory 挂在总线上，可以被其他 AHB master 访问。

1.3.2.3 SRAM

HPSYS 总线上共有 512KB SRAM，其中包括：

- 0x2000_0000-0x2001_FFFF，128KB zero-wait-cycle SRAM（与 D-TCM 共享），所有 AHB master 均可访问，最高频率为 240MHz。
- 0x2002_0000-0x2007_FFFF，384KB zero-wait-cycle SRAM，所有 AHB master 均可访问，最高频率为 240MHz。

1.3.2.4 片外 RAM

HPSYS 支持合封四线和八线 pSRAM，地址空间为 0x6000_0000-0x63FF_FFFF(0x1000_0000-0x13FF_FFFF)，实际可访问地址由外挂颗粒容量决定。接口最高频率为 DDR 156MHz，数据位宽为 8-bit。

1.3.2.5 片外 Flash

HPSYS 支持外挂 NOR/NAND FLASH，其中：

- 0x6000_0000-0x63FF_FFFF(0x1000_0000-0x13FF_FFFF) 地址段可挂合封 FLASH，推荐使用频率为 DTR 104MHz
- 0x6400_0000-0x9FFF_FFFF(0x1400_0000-0x9FFF_FFFF) 地址段可挂外置 FLASH，推荐使用频率为 SDR 104MHz

1.3.3 地址映射

表 1-1: HPSYS 地址映射

Category	Memory /IP	Address Space	HCPU				LCPU	
			Starting Address		Ending Address		Starting Address	Ending Address
HPSYS_ITCM		**64KB**	**0x0000_0000**		**0x0000_FFFF**		**NA**	**NA**
	ROM	64KB	0x0000_0000		0x0000_FFFF		-	-
	Reserved	-	-		-		-	-
External Memory		**1024MB**	**0x1000_0000**	**0x6000_0000**	**0x1FFF_FFFF**	**0x9FFF_FFFF**	**0x6000_0000**	**0x9FFF_FFFF**
	MPI1 Memory	32MB	0x1000_0000	0x6000_0000	0x11FF_FFFF	0x61FF_FFFF	0x6000_0000	0x61FF_FFFF
	MPI2 Memory	32MB	0x1200_0000	0x6200_0000	0x13FF_FFFF	0x63FF_FFFF	0x6200_0000	0x63FF_FFFF
	MPI3 Memory	192MB/960MB	0x1400_0000	0x6400_0000	0x1FFF_FFFF	0x9FFF_FFFF	0x6400_0000	0x9FFF_FFFF
HPSYS_RAM		**512KB**	**0x2000_0000**		**0x2007_FFFF**		**0x2A00_0000**	**0x2A07_FFFF**
	RAM0 (DTCM)	128KB	0x2000_0000		0x2001_FFFF		0x2A00_0000	0x2A01_FFFF
	RAM1	128KB	0x2002_0000		0x2003_FFFF		0x2A02_0000	0x2A03_FFFF
	RAM2	256KB	0x2004_0000		0x2007_FFFF		0x2A04_0000	0x2A07_FFFF
HPSYS_APB1		**256KB**	**0x5000_0000**		**0x5003_FFFF**		**0x5000_0000**	**0x5003_FFFF**
	RCC1	4KB	0x5000_0000		0x5000_0FFF		0x5000_0000	0x5000_0FFF
	JPEGD	4KB	0x5000_1000		0x5000_1FFF		0x5000_1000	0x5000_1FFF
	SECU1	4KB	0x5000_2000		0x5000_2FFF		0x5000_2000	0x5000_2FFF
	PINMUX1	4KB	0x5000_3000		0x5000_3FFF		0x5000_3000	0x5000_3FFF
	ATIM1	4KB	0x5000_4000		0x5000_4FFF		0x5000_4000	0x5000_4FFF
	ATIM2	4KB	0x5000_5000		0x5000_5FFF		0x5000_5000	0x5000_5FFF
	EZIP1	4KB	0x5000_6000		0x5000_6FFF		0x5000_6000	0x5000_6FFF
	EPIC	4KB	0x5000_7000		0x5000_7FFF		0x5000_7000	0x5000_7FFF
	LCDC1	4KB	0x5000_8000		0x5000_8FFF		0x5000_8000	0x5000_8FFF
	I2S1	4KB	0x5000_9000		0x5000_9FFF		0x5000_9000	0x5000_9FFF
	CAN1	4KB	0x5000_A000		0x5000_AFFF		0x5000_A000	0x5000_AFFF
	SYSCFG1	4KB	0x5000_B000		0x5000_BFFF		0x5000_B000	0x5000_BFFF
	EFUSEC	4KB	0x5000_C000		0x5000_CFFF		0x5000_C000	0x5000_CFFF
	AES	4KB	0x5000_D000		0x5000_DFFF		0x5000_D000	0x5000_DFFF
	CAN2	4KB	0x5000_E000		0x5000_EFFF		0x5000_E000	0x5000_EFFF
	TRNG	4KB	0x5000_F000		0x5000_FFFF		0x5000_F000	0x5000_FFFF
	Reserved	192KB	0x5002_0000		0x5001_0000		0x5001_0000	0x5003_FFFF

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表 1-1: HPSYS 地址映射（续）

Category	Memory /IP	Address Space	HCPU		LCPU	
			Starting Address	Ending Address	Starting Address	Ending Address
HPSYS_AHB1		**256KB**	**0x5004_0000**	**0x5007_FFFF**	**0x5004_0000**	**0x5007_FFFF**
	DCMI	4KB	0x5004_0000	0x5004_0FFF	0x5004_0000	0x5004_0FFF
	MPI1	4KB	0x5004_1000	0x5004_1FFF	0x5004_1000	0x5004_1FFF
	MPI2	4KB	0x5004_2000	0x5004_2FFF	0x5004_2000	0x5004_2FFF
	MPI3	4KB	0x5004_3000	0x5004_3FFF	0x5004_3000	0x5004_3FFF
	Reserved	4KB	0x5004_4000	0x5004_4FFF	0x5004_4000	0x5004_4FFF
	SDMMC1	4KB	0x5004_5000	0x5004_5FFF	0x5004_5000	0x5004_5FFF
	SDMMC1	4KB	0x5004_6000	0x5004_6FFF	0x5004_6000	0x5004_6FFF
	USBC	4KB	0x5004_7000	0x5004_7FFF	0x5004_7000	0x5004_7FFF
	CRC1	4KB	0x5004_8000	0x5004_8FFF	0x5004_8000	0x5004_8FFF
	Reserved	28KB	0x5004_9000	0x5004_FFFF	0x5004_9000	0x5004_FFFF
	Reserved	192KB	0x5005_0000	0x5007_FFFF	0x5005_0000	0x5007_FFFF
HPSYS_APB2		**128KB**	**0x5008_0000**	**0x5008_FFFF**	**0x5008_0000**	**0x5008_FFFF**
	Reserved	4KB	0x5008_0000	0x5008_0FFF	0x5008_0000	0x5008_0FFF
	DMAC1	4KB	0x5008_1000	0x5008_1FFF	0x5008_1000	0x5008_1FFF
	MAILBOX1	4KB	0x5008_2000	0x5008_2FFF	0x5008_2000	0x5008_2FFF
	Reserved	4KB	0x5008_3000	0x5008_3FFF	0x5008_3000	0x5008_3FFF
	USART1	4KB	0x5008_4000	0x5008_4FFF	0x5008_4000	0x5008_4FFF
	USART2	4KB	0x5008_5000	0x5008_5FFF	0x5008_5000	0x5008_5FFF
	USART3	4KB	0x5008_6000	0x5008_6FFF	0x5008_6000	0x5008_6FFF
	AUDPRC	4KB	0x5008_7000	0x5008_7FFF	0x5008_7000	0x5008_7FFF
	AUDCODEC	4KB	0x5008_8000	0x5008_8FFF	0x5008_8000	0x5008_8FFF
	TSEN	4KB	0x5008_9000	0x5008_9FFF	0x5008_9000	0x5008_9FFF
	I2S2	4KB	0x5008_A000	0x5008_AFFF	0x5008_A000	0x5008_AFFF
	Reserved	20KB	0x5008_B000	0x5008_FFFF	0x5008_B000	0x5008_FFFF
HPSYS_APB3		**64KB**	**0x5009_0000**	**0x5009_FFFF**	**0x5009_0000**	**0x5009_FFFF**
	GPTIM1	4KB	0x5009_0000	0x5009_0FFF	0x5009_0000	0x5009_0FFF
	Reserved	4KB	0x5009_1000	0x5009_1FFF	0x5009_1000	0x5009_1FFF
	BTIM1	4KB	0x5009_2000	0x5009_2FFF	0x5009_2000	0x5009_2FFF
	Reserved	4KB	0x5009_3000	0x5009_3FFF	0x5009_3000	0x5009_3FFF
	WDT1	4KB	0x5009_4000	0x5009_4FFF	0x5009_4000	0x5009_4FFF
	SPI1	4KB	0x5009_5000	0x5009_5FFF	0x5009_5000	0x5009_5FFF
	SPI2	4KB	0x5009_6000	0x5009_6FFF	0x5009_6000	0x5009_6FFF
	Reserved	4KB	0x5009_7000	0x5009_7FFF	0x5009_7000	0x5009_7FFF
	Reserved	4KB	0x5009_8000	0x5009_8FFF	0x5009_8000	0x5009_8FFF
	Reserved	4KB	0x5009_9000	0x5009_9FFF	0x5009_9000	0x5009_9FFF
	PDM1	4KB	0x5009_A000	0x5009_AFFF	0x5009_A000	0x5009_AFFF
	PDM2	4KB	0x5009_B000	0x5009_BFFF	0x5009_B000	0x5009_BFFF
	I2C1	4KB	0x5009_C000	0x5009_CFFF	0x5009_C000	0x5009_CFFF
	I2C2	4KB	0x5009_D000	0x5009_DFFF	0x5009_D000	0x5009_DFFF
	I2C3	4KB	0x5009_E000	0x5009_EFFF	0x5009_E000	0x5009_EFFF
	I2C4	4KB	0x5009_F000	0x5009_FFFF	0x5009_F000	0x5009_FFFF
HPSYS_AHB2		**64KB**	**0x500A_0000**	**0x500A_FFFF**	**0x500A_0000**	**0x500A_FFFF**
	GPIO1	4KB	0x500A_0000	0x500A_0FFF	0x500A_0000	0x500A_0FFF
	PTM1	4KB	0x500A_1000	0x500A_1FFF	0x500A_1000	0x500A_1FFF
	Reserved	56KB	0x500A_2000	0x500A_FFFF	0x500A_2000	0x500A_FFFF
HPSYS_APB4		**64KB**	**0x500B_0000**	**0x500B_FFFF**	**0x500B_0000**	**0x500B_FFFF**
	GPTIM2	4KB	0x500B_0000	0x500B_0FFF	0x500B_0000	0x500B_0FFF
	BTIM2	4KB	0x500B_1000	0x500B_1FFF	0x500B_1000	0x500B_1FFF
	GPADC	4KB	0x500B_2000	0x500B_2FFF	0x500B_2000	0x500B_2FFF
	PWM1	4KB	0x500B_3000	0x500B_3FFF	0x500B_3000	0x500B_3FFF
	Reserved	48KB	0x500B_4000	0x500B_FFFF	0x500B_4000	0x500B_FFFF
HPSYS_APB5		**256KB**	**0x500C_0000**	**0x500F_FFFF**	**0x500C_0000**	**0x500F_FFFF**
	HPSYS_AON	4KB	0x500C_0000	0x500C_0FFF	0x500C_0000	0x500C_0FFF
	LPTIM1	4KB	0x500C_1000	0x500C_1FFF	0x500C_1000	0x500C_1FFF
	LPTIM2	4KB	0x500C_2000	0x500C_2FFF	0x500C_2000	0x500C_2FFF
	Reserved	4KB	0x500C_3000	0x500C_3FFF	0x500C_3000	0x500C_3FFF
	Reserved	24KB	0x500C_4000	0x500C_9FFF	0x500C_4000	0x500C_9FFF
	PMUC	4KB	0x500C_A000	0x500C_AFFF	0x500C_A000	0x500C_AFFF
	RTC	4KB	0x500C_B000	0x500C_BFFF	0x500C_B000	0x500C_BFFF
	IWDT	4KB	0x500C_C000	0x500C_CFFF	0x500C_C000	0x500C_CFFF
	Reserved	12KB	0x500C_D000	0x500C_FFFF	0x500C_D000	0x500C_FFFF
	Reserved	64KB	0x500D_0000	0x500D_FFFF	0x500D_0000	0x500D_FFFF
	Reserved	64KB	0x500E_0000	0x500E_FFFF	0x500E_0000	0x500E_FFFF
	EUROPA	4KB	0x500F_0000	0x500F_0FFF	0x500F_0000	0x500F_0FFF
	Reserved	60KB	0x500F_1000	0x500F_FFFF	0x500F_1000	0x500F_FFFF

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1.3.4 中断列表

表 1-2: HCPU IRQ

NMI	WDT1	IRQ[26]	rsvd	IRQ[53]	DMAC1_CH4	IRQ[80]	MAILBOX2_CH2
IRQ[0]	AON	IRQ[27]	rsvd	IRQ[54]	DMAC1_CH5	IRQ[81]	SDMMC2
IRQ[1]	LCPU_IRQ[1]	IRQ[28]	rsvd	IRQ[55]	DMAC1_CH6	IRQ[82]	PDM1
IRQ[2]	LCPU_IRQ[2]	IRQ[29]	rsvd	IRQ[56]	DMAC1_CH7	IRQ[83]	CAN1
IRQ[3]	LCPU_IRQ[3]	IRQ[30]	rsvd	IRQ[57]	DMAC1_CH8	IRQ[84]	GPIO1
IRQ[4]	LCPU_IRQ[4]	IRQ[31]	rsvd	IRQ[58]	MAILBOX2_CH1	IRQ[85]	MPI1
IRQ[5]	LCPU_IRQ[5]	IRQ[32]	PTM1_CORE0_IRQ	IRQ[59]	USART1	IRQ[86]	MPI2
IRQ[6]	LCPU_IRQ[6]	IRQ[33]	PTM1_CORE1_IRQ	IRQ[60]	SPI1	IRQ[87]	MPI3
IRQ[7]	LCPU_IRQ[7]	IRQ[34]	PTM1_CORE2_IRQ	IRQ[61]	I2C1	IRQ[88]	PDM2
IRQ[8]	LCPU_IRQ[8]	IRQ[35]	PTM1_CORE3_IRQ	IRQ[62]	EPIC	IRQ[89]	EZIP1
IRQ[9]	LCPU_IRQ[9]	IRQ[36]	PTM1_CORE4_IRQ	IRQ[63]	LCDC1	IRQ[90]	AUDPRC
IRQ[10]	LCPU_IRQ[10]	IRQ[37]	PTM1_CORE5_IRQ	IRQ[64]	I2S1	IRQ[91]	TSEN
IRQ[11]	LCPU_IRQ[11]	IRQ[38]	PTM1_CORE6_IRQ	IRQ[65]	GPADC	IRQ[92]	USBC
IRQ[12]	LCPU_IRQ[12]	IRQ[39]	PTM1_CORE7_IRQ	IRQ[66]	EFUSEC	IRQ[93]	I2C3
IRQ[13]	LCPU_IRQ[13]	IRQ[40]	rsvd	IRQ[67]	AES	IRQ[94]	ATIM1
IRQ[14]	LCPU_IRQ[14]	IRQ[41]	rsvd	IRQ[68]	rsvd	IRQ[95]	USART3
IRQ[15]	LCPU_IRQ[15]	IRQ[42]	rsvd	IRQ[69]	TRNG	IRQ[96]	AUD_HP
IRQ[16]	LCPU_IRQ[16]	IRQ[43]	rsvd	IRQ[70]	GPTIM1	IRQ[97]	DCMI
IRQ[17]	LCPU_IRQ[17]	IRQ[44]	rsvd	IRQ[71]	GPTIM2	IRQ[98]	SECU1
IRQ[18]	LCPU_IRQ[18]	IRQ[45]	rsvd	IRQ[72]	BTIM1	IRQ[99]	JPEGD
IRQ[19]	LCPU_IRQ[19]	IRQ[46]	LPTIM1	IRQ[73]	BTIM2	IRQ[100]	CAN2
IRQ[20]	LCPU_IRQ[20]	IRQ[47]	LPTIM2	IRQ[74]	USART2	IRQ[101]	ATIM2
IRQ[21]	rsvd	IRQ[48]	PMUC	IRQ[75]	SPI2	IRQ[102]	rsvd
IRQ[22]	rsvd	IRQ[49]	RTC	IRQ[76]	I2C2	IRQ[103]	I2S2
IRQ[23]	rsvd	IRQ[50]	DMAC1_CH1	IRQ[77]	rsvd	IRQ[104]	rsvd
IRQ[24]	rsvd	IRQ[51]	DMAC1_CH2	IRQ[78]	I2C4	IRQ[105]	PWM1
IRQ[25]	rsvd	IRQ[52]	DMAC1_CH3	IRQ[79]	SDMMC1		

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1.4 总线访问权限

表 1-3: 总线访问权限

	AHB 从设备							
AHB 主控	HP_ITCM	HP_RAM0	HP_RAM 1~2	MPI1~2	HP_AHB HP_APB	LP_ITCM	LP_RAM 0~1	LP_AHB LP_APB
HCPU	√	√	√	√(1)	√	√(2)	√	√
ACPU	x	√	√	√	√	√(2)	√	√
DMAC1	√(3)	√	√	√	√	√(2)	√	√
AES	x	√	√	√	x	x	x	x
LCDC1	x	√	√	√	x	x	x	x
EZIP	x	√	√	√	x	x	x	x
EPIC	x	√	√	√	x	x	x	x
JPEGD	x	√	√	√	x	x	x	x
USBC	x	√	√	√	x	x	x	x
PTM1	x	√	√	x	√	√(2)	√	√
LCPU	x	√(4)	√(4)	√	√	√	√(5)	√
DMAC2	x	√(4)	√(4)	√	√	√	√	√
PTC2	x	x	x	x	√	x	x	√

* (1)HCPU 既可以通过 0x10000000 起始地址访问 MPI 内容，也可以通过 0x60000000 起始地址访问 MPI 内容。其他主控只能通过 0x60000000 访问 MPI。

(2)HPSYS 的主控访问 LPSYS 的 ITCM，起始地址是 0x20800000，与 LCPU 访问的地址不同。

(3) 其它主控访问 HCPU 的 ROM，起始地址从 0xa0000000 开始，也就是说增加了 0xa0000000 的偏移。

(4)LPSYS 的主控访问 HPSYS 的 SRAM，起始地址从 0x2a000000 开始，也就是说增加了 0x0a000000 的偏移。

(5)LCPU 访问 LPSYS 的 SRAM，起始地址既可以从 0x00400000 开始，也可以从 0x20400000 开始。

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2 时钟与复位

2.1 简介

时钟与复位模块用于控制芯片时钟与复位，可实现时钟选择，时钟分频，各模块使能，各模块复位等功能。

2.2 复位源

芯片的复位源主要分为板级复位，看门狗复位，软件复位，唤醒复位四类。每一类有若干种复位源，每种复位源的作用域不同。

2.2.1 板级复位

板级复位源主要包括：

上电复位 POR (Power On Reset)。芯片上电时自动产生的复位，能够将芯片整体初始化，所有模块状态都复位成默认值。

欠压复位 BOR (Brown-Out Reset)。芯片 VSYS 电压低于一定阈值时自动产生的复位，能够将芯片整体初始化，所有模块状态都复位成默认值。

电源按键 (PWRKEY) 复位。如果芯片的电源按键 PA34 持续高电平超过 10 秒，会发生 PWRKEY 复位，将除 RTC 与 IWDT 以外的所有模块复位。通过 PMUC 的 WSR_PWRKEY 标志可以查询是否发生过 PWRKEY 复位，通过 PMUC 的 WCR_PWRKEY 可以清除该标志。复位所需持续高电平的时间可通过 PMUC 的 PWRKEY_CNT 寄存器配置，默认约 10 秒。

VBAT 欠压复位。芯片 VBAT 供电电压低于一定阈值时自动产生的复位，能够将除 RTC 与 IWDT 以外的所有模块复位。通过 PMUC 的 WSR_LOWBAT 标志可以查询是否发生过 VBAT 欠压复位，通过 PMUC 的 WCR_LOWBAT 可以清除该标志。

2.2.2 看门狗复位

看门狗复位源主要包括：

全局看门狗 IWDT。IWDT 的超时信息会上报至 HCPU 的 NMI 中断。如果该看门狗连续超时两次，会产生 IWDT 复位，自动将除 RTC 与 IWDT 以外的所有模块复位。通过 PMUC 的 WSR_IWDTRST 标志可以查询是否发生过 IWDT 复位，通过 PMUC 的 WCR_IWDTRST 清除该标志。

看门狗 WDT1 和 WDT2 并不能直接产生复位，而是会将超时信息分别上报至 ACPU 和 LCPU 的 NMI 中断，并会将连续超时两次的信息上报至 HCPU 的中断，由 HCPU 触发软件复位。

2.2.3 软件复位

软件复位源主要包括：

软件重启 Reboot。软件通过将 PMUC 的 CR_REBOOT 写 1，可以触发软件重启。重启后除 PMUC，RTC 与 IWDT

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以外的所有模块复位。软件重启后 PMUC 的 CR_REBOOT 保持为 1，可以作为发生过软件重启的标志。如果需要再次触发软件重启，需要首先将 CR_REBOOT 置 0。

HCPU 系统复位。软件通过配置 HCPU 内部寄存器发送 SYSRESETREQ，能够复位 HPSYS 内部除 HPSYS_AON 和 SECU1 以外的各模块，包括 HCPU、ACPU、EPIC、DMAC1 等。外部调试器连接上 HCPU 后发送的系统复位等同 HCPU 系统复位。

ACPU 系统复位。软件通过配置 ACPU 内部寄存器发送 SYSRESETREQ，能够复位 ACPU 模块。外部调试器连接上 ACPU 后发送的系统复位等同 ACPU 系统复位。

LCPU 系统复位。软件通过配置 LCPU 内部寄存器发送 SYSRESETREQ，能够复位 LPSYS 内部除 LPSYS_AON 和 SECU2 以外的所有模块，包括 LCPU、DMAC2、MAC 等。外部调试器连接上 LCPU 后发送的系统复位等同 LCPU 系统复位。

模块 RCC 复位。可以通过 HPSYS_RCC 或 LPSYS_RCC 内的 $RSTR_x$ 寄存器实现单个模块的复位。

2.2.4 唤醒复位

唤醒复位源主要包括：

Hibernate 唤醒。芯片进入 hibernate 模式，唤醒时会将除 PMUC，RTC 与 IWDT 以外的所有模块复位。

HPSYS standby 唤醒。HPSYS 进入 standby 模式，唤醒时会复位 HPSYS 内部除 HPSYS_AON 以外的各模块，包括 HCPU、EPIC、DMAC1 等。

LPSYS standby 唤醒。LPSYS 进入 standby 模式，唤醒时会复位 LPSYS 内部除 LPSYS_AON 以外的各模块，包括 LCPU、DMAC2、MAC 等。

芯片主要复位源

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表 2-1: 芯片主要复位源

复位作用域		板级复位			看门狗复位
		POR/BOR	PWRKEY	LOWBAT	IWDT
HPSYS	All	√	√	√	√
LPSYS	All	√	√	√	√
AON	PMUC	√	√	√	√
	IWDT	√	√	√	√
	RTC	√	-	-	-

芯片主要复位源-续

表 2-2: 芯片主要复位源-续

复位作用域		软件复位				唤醒复位		
		Reboot	HCPU sysrst	ACPU sysrst	LCPU sysrst	hibernate 唤醒	HPSYS standby 唤醒	LPSYS standby 唤醒
HPSYS	HCPU	√	√	-	-	√	√	-
	ACPU	√	√	√	-	√	√	-
	SRAM ret	√	-	-	-	√	-	-
	SRAM noret	√	-	-	-	√	√	-
	HPSYS 外设	√	√	-	-	√	√	-
	HPAON	√	√	-	-	√	-	-
LPSYS	LCPU	√	√	-	√	√	-	√
	SRAM	√	-	-	-	√	-	-
	LPSYS 外设	√	√	-	-	√	-	√
	LPAON	√	√	-	-	√	-	-
AON	PMUC	-	-	-	-	-	-	-
	IWDT	-	-	-	-	-	-	-
	RTC	-	-	-	-	-	-	-

2.3 时钟源

芯片内部主要时钟源如下表。各功能模块时钟均基于这些时钟源产生。

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表 2-3: 芯片主要时钟源

时钟	频率	依赖关系
clk_lrc10	~10kHz	无
clk_lrc32	~32kHz	无
clk_lxt32	32.768kHz	32k 晶振
clk_hrc48	~48MHz	无
clk_hxt48	48MHz	48M 晶振
clk_dll1	48~384MHz	clk_hxt48
clk_dll2	48~384MHz	clk_hxt48
clk_audpll	49.152MHz	clk_hxt48

clk_lrc10 是芯片内部产生的低功耗 RC 振荡器时钟，频率约为 10kHz，但存在一定偏差。该时钟频率会受外部环境影响，使用时可通过测量流程获取当前频率。芯片启动后该时钟作为低功耗模块 (如 PMUC) 的默认工作时钟自动开启。clk_lrc10 相关配置寄存器是 PMUC 的 LRC10_CR。

clk_lrc32 是芯片内部产生的低功耗 RC 振荡器时钟，频率约为 32kHz，但存在一定偏差。该时钟频率会受外部环境影响，使用时可通过测量流程获取当前实际频率。clk_lrc32 默认开启，相关配置寄存器是 PMUC 的 LRC32_CR。

clk_lxt32 是基于外部 32k 晶振产生的低功耗时钟，频率为 32.768kHz。该时钟为可选时钟，在需要精确计时的场景下推荐使用。clk_lxt32 默认关闭，相关配置寄存器是 PMUC 的 LXT_CR。

clk_hrc48 是芯片内部产生的 RC 振荡器时钟。芯片启动时该时钟作为 HCPU 的默认工作时钟自动开启，但此时频率未经过校准，是小于 48MHz 的未知值。校准前，应先将 HCPU 的工作时钟切换到其它时钟 (如 clk_hxt48) 上，再执行校准流程。校准之后，clk_hrc48 频率是 48MHz。clk_hrc48 配置寄存器是 PMUC 的 HRC_CR，校准相关寄存器是 HPSYS_RCC 中的 HRCCAL1 和 HRCCAL2。当芯片 HPSYS 与 LPSYS 均处于 deepsleep/standby/hibernate 等低功耗模式时，该时钟默认关闭。

clk_hxt48 是基于外部 48M 晶振产生的时钟，频率为 48MHz。芯片启动时该时钟自动开启，是用于产生更高频率时钟的基础时钟，也是蓝牙工作所需的基础时钟。当系统不需要更高频率时钟，且蓝牙处于睡眠状态时，该时钟可以关闭。当芯片 HPSYS 与 LPSYS 均处于 deepsleep/standby/hibernate 等低功耗模式时，该时钟默认关闭。clk_hxt48 相关配置寄存器是 PMUC 的 HXT_CR1/2/3。

clk_dll1/2 是芯片内部的 DLL 模块基于 clk_hxt48 产生的高频率时钟。这些时钟默认关闭，在需要时分别开启，可独立产生不同频率。DLL 模块产生的时钟频率以 24MHz(≤384MHz 时) 或 48MHz(>384MHz 时) 为阶梯可配置，配置寄存器分别为 HPSYS_RCC 中的 DLL1CR 和 DLL2CR。当芯片 HPSYS 处于低功耗模式时，这些时钟默认关闭。

clk_audpll 是芯片内部的 PLL 模块基于 clk_hxt48 产生的时钟，是音频相关模块的工作时钟，频率可调，通常设为 44.1MHz。该时钟默认关闭，配置寄存器位于 AUDCODEC 模块。

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2.4 系统时钟结构

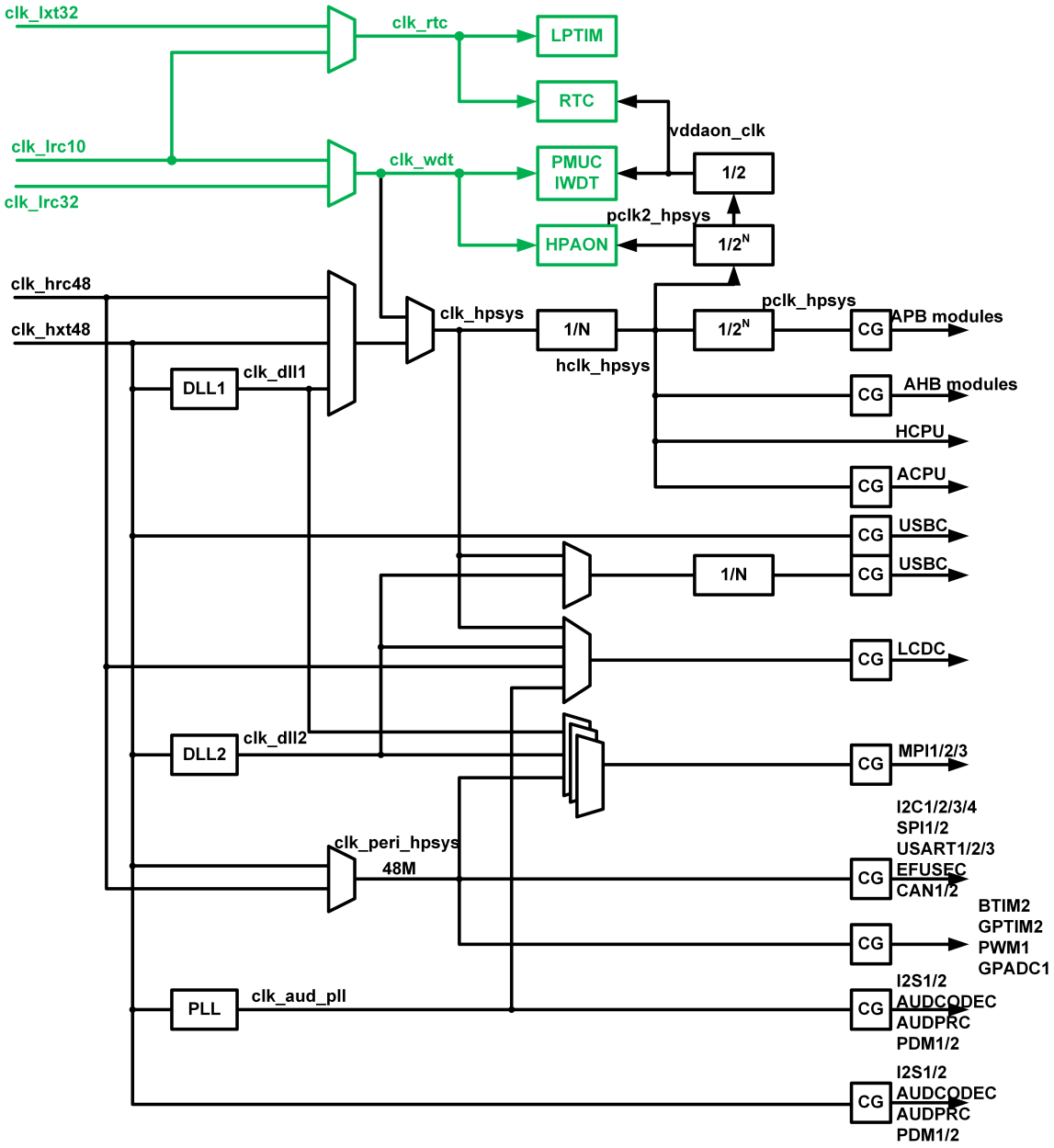


图 2-1: 系统时钟结构

系统时钟 clk_hpsys 可在 clk_hrc48, clk_hxt48 和 clk_dll1 中选择。选择寄存器为 HPSYS_RCC 中的 CSR_SEL_SYS。clk_hpsys 支持的最高频率是 48MHz(基础模式) 或 240MHz(增强模式)。

hclk_hpsys 由 clk_hpsys 1 比 N 分频产生，分频比为 HPSYS_RCC 中的 CFGR_HDIV。hclk_hpsys 支持的最高频率是 48MHz(基础模式) 或 240MHz(增强模式)，是 HCPU、ACPU、EPIC、DMAC1 等 AHB 模块，以及 AHB 总线和 SRAM 的工作时钟。

pclk_hpsys 由 hclk_hpsys 1 比 2N 分频产生，分频比为 2^{CFGR_PDIV1}。pclk_hpsys 支持的最高频率是 48MHz(基础模式) 或 120MHz(增强模式)，是 GPTIM1、BTIM1 等 APB 模块的工作时钟，以及 APB 总线时钟。当 hclk_hpsys 或

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pclk_hpsys 频率发生变化时，GPTIM1、BTIM1 等模块的工作时钟频率随之改变，功能会受到影响。因此在相关模块工作时，应当使得 hclk_hpsys 和 pclk_hpsys 频率保持不变。

pclk2_hpsys 由 hclk_hpsys 1 比 2N 分频产生，分频比为 2^{CFGR_PDIV2} 且不能为 1。pclk2_hpsys 支持的最高频率是 6MHz(基础模式) 或 7.5MHz(增强模式)，是 HPAON 模块的寄存器访问时钟。

MPI1/2/3 的工作时钟可在 clk_dll1，clk_dll2 和 clk_peri_hpsys 中选择。选择寄存器为 HPSYS_RCC 中的 CSR_SEL_MPI1/2/3。MPI1/2/3 的工作时钟彼此异步，并且与其它时钟都为异步关系。

USBC1 的工作时钟可在 clk_hpsys，clk_dll2 和 clk_hxt48 中选择，选择寄存器为 HPSYS_RCC 中的 CSR_SEL_USB，并经 1 比 N 分频产生，分频比为 USBCR_DIV。启动时 USBC1 的默认工作时钟为 clk_hxt48，能够满足下载需求。启动后使用 USBC1 时，工作时钟推荐切换为 DLL1 分频产生的 60MHz。

USART1/2/3、SPI1/2、I2C1/2/3/4、CAN1/2 等外设的工作时钟 clk_peri_hpsys 可在 clk_hrc48 和 clk_hxt48 中选择，频率为 48MHz。选择寄存器为 HPSYS_RCC 中的 CSR_SEL_PERI。clk_peri_hpsys 独立于系统时钟，因此在系统动态调节频率时不受影响。

BTIM2 和 GPTIM2、PWM1 和 GPADC 的工作时钟是 clk_peri_hpsys，独立于系统时钟，在系统动态调节频率时计数不受影响。

音频模块 I2S1、AUDPRC、AUDCODEC、PDM1/2 可在两路工作时钟中选择一路使用，选择寄存器位于这些模块内部。其中一路工作时钟是 clk_hxt48，另一路是 clk_audpll。

PDM1 可在两路工作时钟中选择一路使用，选择寄存器位于 PDM 内部。其中一路工作时钟是 clk_hxt48，另一路由 clk_audpll 16 分频产生。

LCDC 的工作时钟可在 clk_hpsys, clk_dll2, clk_hrc48 和 clk_audpll 中选择。

HPSYS_GPIO 的工作时钟 clk_gpio1 可在 pclk_hpsys 和 clk_wdt 中选择。Active 模式选择 pclk_hpsys，进入 deepsleep 模式自动切换成 clk_wdt，用于 IO 唤醒。

低功耗时钟 clk_rtc 可在 clk_lrc10 和 clk_lxt32 中选择，是 LPTIM1/2、RTC 等低功耗模块的工作时钟，以及蓝牙的睡眠时钟。clk_rtc 选择寄存器为 PMUC 模块的 CR.SEL_RTC。

表 2-4: clk_rtc 相关模块工作时钟

模块	PMUC->CR.SEL_RTC=0	PMUC->CR.SEL_RTC=1
RTC	lrc10	lxt32
LPTIM1	lrc10	lxt32
LPTIM2	lrc10	lxt32
GTIM	lrc10	lxt32
蓝牙睡眠时钟	lrc10	lxt32

低功耗时钟 clk_wdt 可在 clk_lrc10 和 clk_lrc32 中选择，是 HPAON、PMUC、IWDT 等低功耗模块的工作时钟。clk_wdt 选择寄存器为 PMUC 模块的 CR.SEL_WDT。

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表 2-5: clk_wdt 相关模块工作时钟

模块	PMUC->CR.SEL_WDT=0	PMUC->CR.SEL_WDT=1
WDT1	lrc10	lrc32
WDT2	lrc10	lrc32
IWDT	lrc10	lrc32
PMUC	lrc10	lrc32

2.5 模块时钟

本章列举了各模块的工作时钟与总线时钟。

工作时钟是模块内部逻辑单元的运行时钟，时钟频率越快则模块的工作效率越高。对于带有 IO 接口的模块，如 LCDC/I2C 等，接口时钟也往往由工作时钟分频产生。

总线时钟是通过 AHB 或 APB 总线访问模块寄存器的时钟，时钟频率越快则读写模块寄存器的效率越高。

表 2-6: HPSYS 模块时钟

模块	工作时钟	总线时钟
HCPU	hclk_hpsys	hclk_hpsys
ACPU	hclk_hpsys	hclk_hpsys
DMAC1	hclk_hpsys	pclk_hpsys
EPIC	hclk_hpsys	pclk_hpsys
EZIP	hclk_hpsys	pclk_hpsys
LCDC	clk_hpsys 或 clk_dll2 或 clk_hrc48 或 clk_audpll	pclk_hpsys
JPEGD	hclk_hpsys	pclk_hpsys
DCMI	hclk_hpsys	hclk_hpsys
AES	hclk_hpsys	pclk_hpsys
USBC1	clk_hxt48, 或 clk_hpsys/clk_dll2, 并分频	hclk_hpsys
SDMMC1	hclk_hpsys	hclk_hpsys
SDMMC2	hclk_hpsys	hclk_hpsys
MPI1	clk_dll1 或 clk_dll2 或 clk_peri_hpsys	hclk_hpsys
MPI2	clk_dll1 或 clk_dll2 或 clk_peri_hpsys	hclk_hpsys
MPI3	clk_dll1 或 clk_dll2 或 clk_peri_hpsys	hclk_hpsys
CRC1	hclk_hpsys	hclk_hpsys
HPSYS_GPIO	pclk_hpsys 或 clk_wdt	hclk_hpsys
PTM1	hclk_hpsys	hclk_hpsys
SECU1	hclk_hpsys	pclk_hpsys
PINMUX1	/	pclk_hpsys
AUDPRC	clk_hxt48 或 clk_audpll	pclk_hpsys
AUDCODEC	clk_hxt48 或 clk_audpll	pclk_hpsys
I2S1/2	clk_hxt48 或 clk_audpll	pclk_hpsys
PDM1/2	clk_hxt48 或 clk_audpll	pclk_hpsys
I2C1/2/3/4	clk_peri_hpsys	pclk_hpsys
SPI1/2	clk_peri_hpsys	pclk_hpsys
USART1/2/3/4	clk_peri_hpsys	pclk_hpsys
CAN1/2	clk_peri_hpsys	pclk_hpsys
GPADC	clk_peri_hpsys	clk_peri_hpsys

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表 2-6: HPSYS 模块时钟（续）

模块	工作时钟	总线时钟
TSEN	pclk_hpsys	pclk_hpsys
WDT1	clk_wdt	pclk_hpsys
TRNG	pclk_hpsys	pclk_hpsys
EFUSEC	pclk_hpsys	pclk_hpsys
MAILBOX1	pclk_hpsys	pclk_hpsys
ATIM1/2	pclk_hpsys	pclk_hpsys
GPTIM1	pclk_hpsys	pclk_hpsys
GPTIM2	clk_peri_hpsys	clk_peri_hpsys
BTIM1	pclk_hpsys	pclk_hpsys
BTIM2	clk_peri_hpsys	clk_peri_hpsys
PWM1	clk_peri_hpsys	clk_peri_hpsys
RTC	clk_rtc	vddaon_clk
LPTIM1	clk_rtc	pclk2_hpsys
LPTIM2	clk_rtc	pclk2_hpsys
PMUC	clk_wdt	vddaon_clk
IWDT	clk_wdt	vddaon_clk

2.6 模块使能

HPSYS_RCC 中的 ENR1 和 ENR2 寄存器控制各模块使能。模块对应比特为 1 时，该模块寄存器可以访问，模块能够工作。模块对应比特为 0 时，该模块的工作时钟与总线时钟均关闭，模块停止工作，寄存器也无法访问，但寄存器值不会被复位。

HPSYS_RCC 中的 ESR1 和 ESR2 寄存器可用于按位操作打开模块使能。向模块对应比特位写 1，可以打开对应模块使能，其它模块不受影响。

HPSYS_RCC 中的 ECR1 和 ECR2 寄存器可用于按位操作关闭模块使能。向模块对应比特位写 1，可以关闭对应模块使能，其它模块不受影响。

2.7 模块复位

HPSYS_RCC 中的 RSTR1 和 RSTR2 寄存器控制各模块复位。模块对应比特为 1 时，该模块寄存器与内部状态均被复位。模块对应比特为 0 时，模块停止复位。

2.8 时钟的测量与校准

2.8.1 clk_hxt48 的测量与校准

clk_hxt48 是基于外部 48M 晶振产生的时钟，精度主要取决于外部 48M 晶振器件。由于晶振器件的个体差异而产生的频率偏差通常为数十 ppm 量级。

基于 clk_hxt48 产生的高频率时钟包括 clk_dll1, clk_dll2, clk_audpll 以及蓝牙的射频时钟等，其精度与 clk_hxt48 的精度相关。

芯片正常使用时 clk_hxt48 不需要校准。如果产品对频率精度有更高要求，可以选择更高精度的晶振器件，也可

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以在产品的生产环节增加晶振校准流程。

晶振校准流程主要包含以下步骤：

1. 读取 PMUC 的 HXT_CR1.CBANK_SEL 寄存器;
2. 测量 clk_hxt48 的频率;
3. 根据测量的结果增大或减小 CBANK_SEL 寄存器，以降低或提高 clk_hxt48 的频率;
4. 等待 100us，使 clk_hxt48 稳定;
5. 重复步骤 2~4，直到测量结果满足精度要求;
6. 记录此时的 CBANK_SEL 寄存器值，并在后续每次芯片启动后恢复该值。

测量 clk_hxt48 的频率主要有以下几种方法：

- 将 clk_hxt48 通过 PA20 管脚引出直接测量，配置方法为
  - HPSYS_PINMUX->PAD_PA20.FSEL=7;
  - HPSYS_RCC->DBGCLKR=9;

  该测量方法难以达到较高精度。
- 测量蓝牙发射的射频载波信号的频率，计算出 clk_hxt48 的频率。
- 利用时钟源为 clk_hxt48 的 ATIM 或 GPTIM，对外部输入的高精度 PWM 信号进行门控计数，根据计数值计算出 clk_hxt48 的频率。该方法可适用于产品的生产环节。
- 蓝牙接收外部发射的高精度蓝牙信号，计算出 clk_hxt48 的频率。该方法可适用于产品的生产环节。

2.8.2 clk_hrc48 的测量与校准

clk_hrc48 是芯片内部产生的 RC 振荡器时钟，未校准时默认频率低于 48MHz，校准后频率为 48MHz。推荐在芯片每次启动之后进行 clk_hrc48 的校准。

clk_hrc48 校准流程主要包含以下步骤：

1. 系统时钟切换到非 clk_hrc48 的时钟源;
2. 测量 clk_hrc48 的频率;
3. 根据测量的结果增大或减小 PMUC 的 HRC_CR.FREQ_TRIM 寄存器，以提高或降低 clk_hrc48 的频率;
4. 等待 100us，使 clk_hrc48 稳定;
5. 重复步骤 2~4，直到测量结果满足精度要求;
6. 记录此时的 FREQ_TRIM 寄存器值，并在后续每次重启后恢复该值。

测量 clk_hrc48 的频率主要有以下几种方法：

- 将 clk_hrc48 通过 PA20 管脚引出直接测量，配置方法为
  - HPSYS_PINMUX->PAD_PA20.FSEL=7;
  - HPSYS_RCC->DBGCLKR=8;
- 利用 clk_hxt48 测算 clk_hrc48 的频率，配置方法为
  - HPSYS_RCC->HRCCAL1=0x8000; //0x8000 为设置测量的时间长度，以 48MHz 周期计数，可按需修改
  - HPSYS_RCC->HRCCAL1|=HPSYS_RCC_HRCCAL1_CAL_EN; //启动测量
  - 等待直到 HPSYS_RCC->HRCCAL1.CAL_DONE 为 1;
  - 读取 HPSYS_RCC->HRCCAL2.HRC_CNT，得到在配置的时间长度内 clk_hrc48 的周期计数，经过计算可以得到 clk_hrc48 的频率。

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2.8.3 clk_lxt32 的测量

clk_lxt32 是基于外部 32k 晶振产生的低功耗时钟，频率为 32.768kHz，精度主要取决于外部 32k 晶振器件。由于晶振器件的个体差异而产生的频率偏差通常为数十 ppm 量级。

clk_lxt32 的频率无法调节，但可以进行测量以获取更精确的频率值。

测量 clk_lxt32 的频率主要有以下几种方法：

- 将 clk_lxt32 通过 PA24~PA27 管脚引出直接测量，配置方法为 (以 PA24 为例)
  - HPSYS_PINMUX->PAD_PA24=0x4;//功能选择 clk_rtc 输出
  - PMUC->CR |=2；//clk_rtc 选择为 clk_lxt32

  此方法引出的 clk_lxt32 在芯片进入除 hibernate 以外的低功耗模式时也能保持输出，可以用于向外部器件输出 32k 时钟，频率为 32.768kHz。
- 利用 clk_hxt48 测算 clk_lxt32 的频率，必须在 LPSYS 处于 active 模式并且蓝牙没有工作时进行，配置方法为
  - PMUC->CR |=2；//clk_rtc 选择为 clk_lxt32
  - BT_MAC->RCCAL_CTRL=0x8000; //0x8000 为设置测量的时间长度，以 clk_lxt32 的周期计数，可按需修改，最大为 65535
  - BT_MAC->RCCAL_CTRL|=0x20000; //启动测量
  - 等待直到 BT_MAC->RCCAL_RESULT 的比特 31 为 1;
  - 读取 BT_MAC->RCCAL_RESULT，低 30 比特即为在配置的时间长度内 clk_hxt48 的周期计数，经过计算可以得到 clk_lxt32 的频率。
- 利用 clk_hxt48 测算 clk_lrc32 的频率，在 HPSYS 内部完成，不需 LPSYS 处于 active 模式，配置方法为
  - PMUC->CR |=2；//clk_rtc 选择为 clk_lxt32
  - HPSYS_RCC->RC10CAL1=0x8000; //0x8000 为设置测量的时间长度，以 clk_lrc10 的周期计数，可按需修改，最大为 65535
  - HPSYS_RCC->RC10CAL1|=0x20000; //启动测量
  - 等待直到 HPSYS_RCC->RC10CAL2 的比特 31 为 1;
  - 读取 HPSYS_RCC->RC10CAL2，低 30 比特即为在配置的时间长度内 clk_hxt48 的周期计数，经过计算可以得到 clk_lrc10 的频率。

2.8.4 clk_lrc10 的测量

clk_lrc10 是芯片内部产生的低功耗 RC 振荡器时钟，频率约为 10kHz 且无法调节，可以进行测量以获取精确的频率值。

如果 clk_rtc 选择为 clk_lrc10，推荐在芯片工作过程中定期进行 clk_lrc10 的测量。

测量 clk_lrc10 的频率主要有以下几种方法：

- 将 clk_lrc10 通过 PA24~PA27 管脚引出直接测量，配置方法为 (以 PA25 为例)
  - HPSYS_PINMUX->PAD_PA25=0x4; //功能选择 clk_rtc 输出
  - PMUC->CR & =0xfffffffd；//clk_rtc 选择为 clk_lrc10
- 利用 clk_hxt48 测算 clk_lrc10 的频率，必须在 LPSYS 处于 active 模式时进行，配置方法为
  - PMUC->CR &=0xfffffffd；//clk_rtc 选择为 clk_lrc10
  - BT_MAC->RCCAL_CTRL=0x8000; //0x8000 为设置测量的时间长度，以 clk_lrc10 的周期计数，可按需

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修改，最大为 65535

- BT_MAC->RCCAL_CTRL|=0x20000; //启动测量
- 等待直到 BT_MAC->RCCAL_RESULT 的比特 31 为 1;
- 读取 BT_MAC->RCCAL_RESULT，低 30 比特即为在配置的时间长度内 clk_hxt48 的周期计数，经过计算可以得到 clk_lrc10 的频率。

- 利用 clk_hxt48 测算 clk_lrc10 的频率，在 HPSYS 内部完成，不需 LPSYS 处于 active 模式，配置方法为
  - PMUC->CR &=0xfffffffd；//clk_rtc 选择为 clk_lrc10
  - HPSYS_RCC->RC10CAL1=0x8000; //0x8000 为设置测量的时间长度，以 clk_lrc10 的周期计数，可按需修改，最大为 65535
  - HPSYS_RCC->RC10CAL1|=0x20000; //启动测量
  - 等待直到 HPSYS_RCC->RC10CAL2 的比特 31 为 1;
  - 读取 HPSYS_RCC->RC10CAL2，低 30 比特即为在配置的时间长度内 clk_hxt48 的周期计数，经过计算可以得到 clk_lrc10 的频率。

2.9 HPSYS_RCC 寄存器

HPSYS_RCC 的基地址是 0x50000000。

表 2-7: HPSYS_RCC 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**RSTR1**	Reset Register 1
[31]	rw	1'h0	PTM1	0 - no reset; 1 - reset
[30:29]			RSVD	
[28]	rw	1'h0	I2C2	0 - no reset; 1 - reset
[27]	rw	1'h0	I2C1	0 - no reset; 1 - reset
[26]	rw	1'h0	PDM2	0 - no reset; 1 - reset
[25]	rw	1'h0	PDM1	0 - no reset; 1 - reset
[24:22]			RSVD	
[21]	rw	1'h0	SPI2	0 - no reset; 1 - reset
[20]	rw	1'h0	SPI1	0 - no reset; 1 - reset
[19]	rw	1'h0	PWM1	0 - no reset; 1 - reset
[18]	rw	1'h0	BTIM2	0 - no reset; 1 - reset
[17]	rw	1'h0	BTIM1	0 - no reset; 1 - reset
[16]	rw	1'h0	GPTIM2	0 - no reset; 1 - reset
[15]	rw	1'h0	GPTIM1	0 - no reset; 1 - reset
[14]	rw	1'h0	TRNG	0 - no reset; 1 - reset
[13]	rw	1'h0	CRC1	0 - no reset; 1 - reset
[12]	rw	1'h0	AES	0 - no reset; 1 - reset
[11]	rw	1'h0	EFUSEC	0 - no reset; 1 - reset
[10]	rw	1'h0	SYSCFG1	0 - no reset; 1 - reset
[9]	rw	1'h0	I2S2	0 - no reset; 1 - reset
[8]	rw	1'h0	I2S1	0 - no reset; 1 - reset
[7]	rw	1'h0	LCDC1	0 - no reset; 1 - reset
[6]	rw	1'h0	EPIC	0 - no reset; 1 - reset
[5]	rw	1'h0	EZIP1	0 - no reset; 1 - reset
[4]	rw	1'h0	USART2	0 - no reset; 1 - reset

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表 2-7: HPSYS_RCC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[3]	rw	1'h0	USART1	0 - no reset; 1 - reset
[2]	rw	1'h0	PINMUX1	0 - no reset; 1 - reset
[1]	rw	1'h0	MAILBOX1	0 - no reset; 1 - reset
[0]	rw	1'h0	DMAC1	0 - no reset; 1 - reset
0x04			**RSTR2**	Reset Register 2
[31:26]			RSVD	
[25]	rw	1'h0	I2C4	0 - no reset; 1 - reset
[24]	rw	1'h0	JPEGD	0 - no reset; 1 - reset
[23]	rw	1'h0	TSEN	0 - no reset; 1 - reset
[22]	rw	1'h0	GPADC	0 - no reset; 1 - reset
[21]			RSVD	
[20]	rw	1'h0	AUDPRC	0 - no reset; 1 - reset
[19]	rw	1'h0	AUDCODEC	0 - no reset; 1 - reset
[18]	rw	1'h0	CAN2	0 - no reset; 1 - reset
[17]	rw	1'h0	CAN1	0 - no reset; 1 - reset
[16:14]			RSVD	
[13]	rw	1'h0	DCMI	0 - no reset; 1 - reset
[12]	rw	1'h0	USART3	0 - no reset; 1 - reset
[11]			RSVD	
[10]	rw	1'h0	ATIM2	0 - no reset; 1 - reset
[9]	rw	1'h0	ATIM1	0 - no reset; 1 - reset
[8]	rw	1'h0	I2C3	0 - no reset; 1 - reset
[7]			RSVD	
[6]	rw	1'h0	USBC	0 - no reset; 1 - reset
[5]	rw	1'h0	SDMMC2	0 - no reset; 1 - reset
[4]	rw	1'h0	SDMMC1	0 - no reset; 1 - reset
[3]	rw	1'h0	MPI3	0 - no reset; 1 - reset
[2]	rw	1'h0	MPI2	0 - no reset; 1 - reset
[1]	rw	1'h0	MPI1	0 - no reset; 1 - reset
[0]	rw	1'h0	GPIO1	0 - no reset; 1 - reset
0x08			**ENR1**	Enable Register 1
[31]	rw	1'h0	PTM1	write 1 to set module enable, write 0 to disable module
[30:29]			RSVD	
[28]	rw	1'h1	I2C2	write 1 to set module enable, write 0 to disable module
[27]	rw	1'h1	I2C1	write 1 to set module enable, write 0 to disable module
[26]	rw	1'h0	PDM2	write 1 to set module enable, write 0 to disable module
[25]	rw	1'h0	PDM1	write 1 to set module enable, write 0 to disable module
[24]			RSVD	
[23]	rw	1'h1	SECU1	write 1 to set module enable, write 0 to disable module
[22]			RSVD	
[21]	rw	1'h0	SPI2	write 1 to set module enable, write 0 to disable module
[20]	rw	1'h0	SPI1	write 1 to set module enable, write 0 to disable module
[19]	rw	1'h0	PWM1	write 1 to set module enable, write 0 to disable module
[18]	rw	1'h1	BTIM2	write 1 to set module enable, write 0 to disable module
[17]	rw	1'h1	BTIM1	write 1 to set module enable, write 0 to disable module
[16]	rw	1'h1	GPTIM2	write 1 to set module enable, write 0 to disable module
[15]	rw	1'h1	GPTIM1	write 1 to set module enable, write 0 to disable module
[14]	rw	1'h1	TRNG	write 1 to set module enable, write 0 to disable module

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表 2-7: HPSYS_RCC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[13]	rw	1'h1	CRC1	write 1 to set module enable, write 0 to disable module
[12]	rw	1'h1	AES	write 1 to set module enable, write 0 to disable module
[11]	rw	1'h1	EFUSEC	write 1 to set module enable, write 0 to disable module
[10]	rw	1'h1	SYSCFG1	write 1 to set module enable, write 0 to disable module
[9]	rw	1'h0	I2S2	write 1 to set module enable, write 0 to disable module
[8]	rw	1'h0	I2S1	write 1 to set module enable, write 0 to disable module
[7]	rw	1'h0	LCDC1	write 1 to set module enable, write 0 to disable module
[6]	rw	1'h0	EPIC	write 1 to set module enable, write 0 to disable module
[5]	rw	1'h0	EZIP1	write 1 to set module enable, write 0 to disable module
[4]	rw	1'h1	USART2	write 1 to set module enable, write 0 to disable module
[3]			RSVD	
[2]	rw	1'h1	PINMUX1	write 1 to set module enable, write 0 to disable module
[1]	rw	1'h1	MAILBOX1	write 1 to set module enable, write 0 to disable module
[0]	rw	1'h1	DMAC1	write 1 to set module enable, write 0 to disable module
0x0C			**ENR2**	Enable Register 2
[31:26]			RSVD	
[25]	rw	1'h1	I2C4	write 1 to set module enable, write 0 to disable module
[24]	rw	1'h0	JPEGD	write 1 to set module enable, write 0 to disable module
[23]	rw	1'h0	TSEN	write 1 to set module enable, write 0 to disable module
[22]	rw	1'h1	GPADC	write 1 to set module enable, write 0 to disable module
[21]			RSVD	
[20]	rw	1'h0	AUDPRC	write 1 to set module enable, write 0 to disable module
[19]	rw	1'h0	AUDCODEC	write 1 to set module enable, write 0 to disable module
[18]	rw	1'h0	CAN2	write 1 to set module enable, write 0 to disable module
[17]	rw	1'h0	CAN1	write 1 to set module enable, write 0 to disable module
[16:14]			RSVD	
[13]	rw	1'h0	DCMI	write 1 to set module enable, write 0 to disable module
[12]	rw	1'h1	USART3	write 1 to set module enable, write 0 to disable module
[11]			RSVD	
[10]	rw	1'h0	ATIM2	write 1 to set module enable, write 0 to disable module
[9]	rw	1'h0	ATIM1	write 1 to set module enable, write 0 to disable module
[8]	rw	1'h1	I2C3	write 1 to set module enable, write 0 to disable module
[7]			RSVD	
[6]	rw	1'h0	USBC	write 1 to set module enable, write 0 to disable module
[5]	rw	1'h0	SDMMC2	write 1 to set module enable, write 0 to disable module
[4]	rw	1'h0	SDMMC1	write 1 to set module enable, write 0 to disable module
[3]	rw	1'h1	MPI3	write 1 to set module enable, write 0 to disable module
[2]	rw	1'h1	MPI2	write 1 to set module enable, write 0 to disable module
[1]	rw	1'h1	MPI1	write 1 to set module enable, write 0 to disable module
[0]	rw	1'h1	GPIO1	write 1 to set module enable, write 0 to disable module
0x10			**ESR1**	Enable Set Register 1
[31]	w	1'h0	PTM1	write 1 to set module enable, write 0 has no effect
[30:29]			RSVD	
[28]	w	1'h0	I2C2	write 1 to set module enable, write 0 has no effect
[27]	w	1'h0	I2C1	write 1 to set module enable, write 0 has no effect
[26]			RSVD	
[25]	w	1'h0	PDM1	write 1 to set module enable, write 0 has no effect
[24]	w	1'h0	PDM2	write 1 to set module enable, write 0 has no effect

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表 2-7: HPSYS_RCC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[23]	w	1'h0	SECU1	write 1 to set module enable, write 0 has no effect
[22]			RSVD	
[21]	w	1'h0	SPI2	write 1 to set module enable, write 0 has no effect
[20]	w	1'h0	SPI1	write 1 to set module enable, write 0 has no effect
[19]	w	1'h0	PWM1	write 1 to set module enable, write 0 has no effect
[18]	w	1'h0	BTIM2	write 1 to set module enable, write 0 has no effect
[17]	w	1'h0	BTIM1	write 1 to set module enable, write 0 has no effect
[16]	w	1'h0	GPTIM2	write 1 to set module enable, write 0 has no effect
[15]	w	1'h0	GPTIM1	write 1 to set module enable, write 0 has no effect
[14]	w	1'h0	TRNG	write 1 to set module enable, write 0 has no effect
[13]	w	1'h0	CRC1	write 1 to set module enable, write 0 has no effect
[12]	w	1'h0	AES	write 1 to set module enable, write 0 has no effect
[11]	w	1'h0	EFUSEC	write 1 to set module enable, write 0 has no effect
[10]	w	1'h0	SYSCFG1	write 1 to set module enable, write 0 has no effect
[9]	w	1'h0	I2S2	write 1 to set module enable, write 0 has no effect
[8]	w	1'h0	I2S1	write 1 to set module enable, write 0 has no effect
[7]	w	1'h0	LCDC1	write 1 to set module enable, write 0 has no effect
[6]	w	1'h0	EPIC	write 1 to set module enable, write 0 has no effect
[5]	w	1'h0	EZIP1	write 1 to set module enable, write 0 has no effect
[4]	w	1'h0	USART2	write 1 to set module enable, write 0 has no effect
[3]			RSVD	
[2]	w	1'h0	PINMUX1	write 1 to set module enable, write 0 has no effect
[1]	w	1'h0	MAILBOX1	write 1 to set module enable, write 0 has no effect
[0]	w	1'h0	DMAC1	write 1 to set module enable, write 0 has no effect
0x14			**ESR2**	Enable Set Register 2
[31:26]			RSVD	
[25]	w	1'h0	I2C4	write 1 to set module enable, write 0 has no effect
[24]	w	1'h0	JPEGD	write 1 to set module enable, write 0 has no effect
[23]	w	1'h0	TSEN	write 1 to set module enable, write 0 has no effect
[22]	w	1'h0	GPADC	write 1 to set module enable, write 0 has no effect
[21]			RSVD	
[20]	w	1'h0	AUDPRC	write 1 to set module enable, write 0 has no effect
[19]	w	1'h0	AUDCODEC	write 1 to set module enable, write 0 has no effect
[18]	w	1'h0	CAN2	write 1 to set module enable, write 0 has no effect
[17]	w	1'h0	CAN1	write 1 to set module enable, write 0 has no effect
[16:14]			RSVD	
[13]	w	1'h0	DCMI	write 1 to set module enable, write 0 has no effect
[12]	w	1'h0	USART3	write 1 to set module enable, write 0 has no effect
[11]			RSVD	
[10]	w	1'h0	ATIM2	write 1 to set module enable, write 0 has no effect
[9]	w	1'h0	ATIM1	write 1 to set module enable, write 0 has no effect
[8]	w	1'h0	I2C3	write 1 to set module enable, write 0 has no effect
[7]			RSVD	
[6]	w	1'h0	USBC	write 1 to set module enable, write 0 has no effect
[5]	w	1'h0	SDMMC2	write 1 to set module enable, write 0 has no effect
[4]	w	1'h0	SDMMC1	write 1 to set module enable, write 0 has no effect
[3]	w	1'h0	MPI3	write 1 to set module enable, write 0 has no effect
[2]	w	1'h0	MPI2	write 1 to set module enable, write 0 has no effect

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表 2-7: HPSYS_RCC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	w	1'h0	MPI1	write 1 to set module enable, write 0 has no effect
[0]	w	1'h0	GPIO1	write 1 to set module enable, write 0 has no effect
0x18			**ECR1**	Enable Clear Register 1
[31]	w	1'h0	PTM1	write 1 to clear module enable, write 0 has no effect
[30:29]			RSVD	
[28]	w	1'h0	I2C2	write 1 to clear module enable, write 0 has no effect
[27]	w	1'h0	I2C1	write 1 to clear module enable, write 0 has no effect
[26]			RSVD	
[25]	w	1'h0	PDM1	write 1 to clear module enable, write 0 has no effect
[24]	w	1'h0	PDM2	write 1 to clear module enable, write 0 has no effect
[23]	w	1'h0	SECU1	write 1 to clear module enable, write 0 has no effect
[22]			RSVD	
[21]	w	1'h0	SPI2	write 1 to clear module enable, write 0 has no effect
[20]	w	1'h0	SPI1	write 1 to clear module enable, write 0 has no effect
[19]	w	1'h0	PWM1	write 1 to clear module enable, write 0 has no effect
[18]	w	1'h0	BTIM2	write 1 to clear module enable, write 0 has no effect
[17]	w	1'h0	BTIM1	write 1 to clear module enable, write 0 has no effect
[16]	w	1'h0	GPTIM2	write 1 to clear module enable, write 0 has no effect
[15]	w	1'h0	GPTIM1	write 1 to clear module enable, write 0 has no effect
[14]	w	1'h0	TRNG	write 1 to clear module enable, write 0 has no effect
[13]	w	1'h0	CRC1	write 1 to clear module enable, write 0 has no effect
[12]	w	1'h0	AES	write 1 to clear module enable, write 0 has no effect
[11]	w	1'h0	EFUSEC	write 1 to clear module enable, write 0 has no effect
[10]	w	1'h0	SYSCFG1	write 1 to clear module enable, write 0 has no effect
[9]	w	1'h0	I2S2	write 1 to clear module enable, write 0 has no effect
[8]	w	1'h0	I2S1	write 1 to clear module enable, write 0 has no effect
[7]	w	1'h0	LCDC1	write 1 to clear module enable, write 0 has no effect
[6]	w	1'h0	EPIC	write 1 to clear module enable, write 0 has no effect
[5]	w	1'h0	EZIP1	write 1 to clear module enable, write 0 has no effect
[4]	w	1'h0	USART2	write 1 to clear module enable, write 0 has no effect
[3]			RSVD	
[2]	w	1'h0	PINMUX1	write 1 to clear module enable, write 0 has no effect
[1]	w	1'h0	MAILBOX1	write 1 to clear module enable, write 0 has no effect
[0]	w	1'h0	DMAC1	write 1 to clear module enable, write 0 has no effect
0x1C			**ECR2**	Enable Clear Register 2
[31:26]			RSVD	
[25]	w	1'h0	I2C4	write 1 to clear module enable, write 0 has no effect
[24]	w	1'h0	JPEGD	write 1 to clear module enable, write 0 has no effect
[23]	w	1'h0	TSEN	write 1 to clear module enable, write 0 has no effect
[22]	w	1'h0	GPADC	write 1 to clear module enable, write 0 has no effect
[21]			RSVD	
[20]	w	1'h0	AUDPRC	write 1 to clear module enable, write 0 has no effect
[19]	w	1'h0	AUDCODEC	write 1 to clear module enable, write 0 has no effect
[18]	w	1'h0	CAN2	write 1 to clear module enable, write 0 has no effect
[17]	w	1'h0	CAN1	write 1 to clear module enable, write 0 has no effect
[16:14]			RSVD	
[13]	w	1'h0	DCMI	write 1 to clear module enable, write 0 has no effect
[12]	w	1'h0	USART3	write 1 to clear module enable, write 0 has no effect

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表 2-7: HPSYS_RCC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11]			RSVD	
[10]	w	1'h0	ATIM2	write 1 to clear module enable, write 0 has no effect
[9]	w	1'h0	ATIM1	write 1 to clear module enable, write 0 has no effect
[8]	w	1'h0	I2C3	write 1 to clear module enable, write 0 has no effect
[7]			RSVD	
[6]	w	1'h0	USBC	write 1 to clear module enable, write 0 has no effect
[5]	w	1'h0	SDMMC2	write 1 to clear module enable, write 0 has no effect
[4]	w	1'h0	SDMMC1	write 1 to clear module enable, write 0 has no effect
[3]	w	1'h0	MPI3	write 1 to clear module enable, write 0 has no effect
[2]	w	1'h0	MPI2	write 1 to clear module enable, write 0 has no effect
[1]	w	1'h0	MPI1	write 1 to clear module enable, write 0 has no effect
[0]	w	1'h0	GPIO1	write 1 to clear module enable, write 0 has no effect
0x20			**CSR**	Clock Select Register
[31:18]			RSVD	
[17:16]	rw	2'h0	SEL_LCDC	select clock source for systick reference 0 - clk_hpsys; 1 - clk_dll2; 2 - clk_hrc48; 3 - clk_audpll
[15]	rw	1'b0	SEL_USBC	select USB source clock 0 - clk_hpsys; 1 - clk_dll2
[14:13]	rw	2'h0	SEL_TICK	select clock source for systick reference 0 - clk_rtc; 1 - reserved; 2 - clk_hrc48; 3 - clk_hxt48
[12]	rw	1'h1	SEL_PERI	select clk_peri_hpsys source used by US-ART/SPI/I2C/GPTIM2/BTIM2/CAN/GPADC 0 - clk_hrc48; 1 - clk_hxt48
[11:10]			RSVD	
[9:8]	rw	2'h0	SEL_MPI3	selet MPI3 function clock 0 - clk_peri_hpsys; 1 - clk_dll1; 2 - clk_dll2; 3 - reserved
[7:6]	rw	2'h0	SEL_MPI2	selet MPI2 function clock 0 - clk_peri_hpsys; 1 - clk_dll1; 2 - clk_dll2; 3 - reserved
[5:4]	rw	2'h0	SEL_MPI1	selet MPI1 function clock 0 - clk_peri_hpsys; 1 - clk_dll1; 2 - clk_dll2; 3 - reserved
[3:2]			RSVD	
[1:0]	rw	2'h0	SEL_SYS	select clk_hpsys source 0 - clk_hrc48; 1 - clk_hxt48; 2 - reserved; 3 - clk_dll1
0x24			**CFGR**	Clock Configuration Register
[31:22]			RSVD	
[21:16]	rw	6'h2	TICKDIV	systick reference clock is systick reference clock source (selected by SEL_TICK) devided by TICKDIV
[15]			RSVD	
[14:12]	rw	3'b100	PDIV2	pclk2_hpsys = hclk_hpsys / (2^{PDIV2}), by default divided by 16. Valid PDIV2 is 1 to 7. 0 is not allowed.
[11]			RSVD	
[10:8]	rw	3'b001	PDIV1	pclk_hpsys = hclk_hpsys / (2^{PDIV1}), by default divided by 2
[7:0]	rw	8'h1	HDIV	hclk_hpsys = clk_hpsys / HDIV if HDIV=0, hclk_hpsys = clk_hpsys
0x28			**USBCR**	USBC Register
[31:3]			RSVD	

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表 2-7: HPSYS_RCC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[2:0]	rw	3'h4	DIV	USB function clock is USB source clock divided by DIV. After divider, USB function clock must be 60MHz. For example, if USBC clock source is 240MHz clk_dll2, DIV should be 4.
0x2C			**DLL1CR**	DLL1 Control Register
[31]	r	1'b0	READY	0: dll not ready 1: dll ready
[30:27]			RSVD	
[26:25]	rw	2'd1	CG_DLY	0 - 0.5us, 1 - 1us, 2 - 1.5us, 3 - 2us
[24:23]	rw	2'd0	LOCK_DLY	0 - 5us, 1 - 10us, 2 - 15us, 3 - 20us
[22:21]	rw	2'd0	PU_DLY	0 - 5us, 1 - 10us, 2 - 15us, 3 - 20us
[20]	rw	1'b0	BYPASS	
[19]	rw	1'b0	VST_SEL	
[18]	rw	1'b0	PRCHG_EXT	
[17]	rw	1'b1	PRCHG_EN	
[16]	rw	1'b1	MCU_PRCHG	
[15]	rw	1'b1	MCU_PRCHG_EN	
[14]	rw	1'b1	OUT_DIV2_EN	0: dll output not divided 1: dll output divided by 2
[13]	rw	1'b1	IN_DIV2_EN	
[12]	rw	1'b1	LDO_FLT_EN	
[11:8]	rw	4'ha	LDO_VREF	
[7]	rw	1'b0	MODE48M_EN	
[6]	rw	1'b1	XTALIN_EN	
[5:2]	rw	4'h0	STG	DLL lock freqency is decided by STG. DLL output frequency is (STG+1)*24MHz if OUT_DIV2_EN=0 e.g. STG=9,DLL output is 240M
[1]	w1t	1'b0	SW	
[0]	rw	1'b0	EN	0: dll disabled 1: dll enabled
0x30			**DLL2CR**	DLL2 Control Register
[31]	r	1'b0	READY	0: dll not ready 1: dll ready
[30:27]			RSVD	
[26:25]	rw	2'd1	CG_DLY	0 - 0.5us, 1 - 1us, 2 - 1.5us, 3 - 2us
[24:23]	rw	2'd0	LOCK_DLY	0 - 5us, 1 - 10us, 2 - 15us, 3 - 20us
[22:21]	rw	2'd0	PU_DLY	0 - 5us, 1 - 10us, 2 - 15us, 3 - 20us
[20]	rw	1'b0	BYPASS	
[19]	rw	1'b0	VST_SEL	
[18]	rw	1'b0	PRCHG_EXT	
[17]	rw	1'b1	PRCHG_EN	
[16]	rw	1'b1	MCU_PRCHG	
[15]	rw	1'b1	MCU_PRCHG_EN	
[14]	rw	1'b1	OUT_DIV2_EN	0: dll output not divided 1: dll output divided by 2
[13]	rw	1'b1	IN_DIV2_EN	
[12]	rw	1'b1	LDO_FLT_EN	
[11:8]	rw	4'ha	LDO_VREF	
[7]	rw	1'b0	MODE48M_EN	

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表 2-7: HPSYS_RCC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[6]	rw	1'b1	XTALIN_EN	
[5:2]	rw	4'h0	STG	DLL lock freqency is decided by STG. DLL output frequency is (STG+1)*24MHz if OUT_DIV2_EN=0 e.g. STG=9,DLL output is 240M
[1]	w1t	1'b0	SW	
[0]	rw	1'b0	EN	0: dll disabled 1: dll enabled
0x34			**HRCCAL1**	HRC Calibration Register 1
[31]	r	1'b0	CAL_DONE	Calibration done. After a new calibration started, results should be processed only when cal_done asserted.
[30]	rw	1'b0	CAL_EN	Calibration enble. Set to 0 to clear result, then set to 1 to start a new calibration
[29:16]			RSVD	
[15:0]	rw	16'h8000	CAL_LENGTH	Target clk_hxt48 cycles during calibration
0x38			**HRCCAL2**	HRC Calibration Register 2
[31:16]	r	16'h0	HXT_CNT	Total clk_hxt48 cycles during calibration
[15:0]	r	16'h0	HRC_CNT	Total clk_hrc48 cycles during calibration
0x3C			**DBGCLKR**	Debug Clock Register
[31:28]	rw	4'b0	DLL2_DTEST_TR	for debug only
[27]	rw	1'b0	DLL2_DTEST_EN	for debug only
[26:25]	rw	2'h1	DLL2_OUT_STR	for debug only
[24]	rw	1'b0	DLL2_CG_EN	for debug only
[23]	rw	1'b0	DLL2_OUT_EN	for debug only
[22]	rw	1'b0	DLL2_OUT_RSTB	for debug only
[21]	rw	1'b0	DLL2_LOOP_EN	for debug only
[20]	rw	1'b0	DLL2_LDO_FLT_EN	for debug only
[19]	rw	1'b0	DLL2_LDO_EN	for debug only
[18]	rw	1'b0	DLL2_DBG	for debug only
[17:14]	rw	4'b0	DLL1_DTEST_TR	for debug only
[13]	rw	1'b0	DLL1_DTEST_EN	for debug only
[12:11]	rw	2'h1	DLL1_OUT_STR	for debug only
[10]	rw	1'b0	DLL1_CG_EN	for debug only
[9]	rw	1'b0	DLL1_OUT_EN	for debug only
[8]	rw	1'b0	DLL1_OUT_RSTB	for debug only
[7]	rw	1'b0	DLL1_LOOP_EN	for debug only
[6]	rw	1'b0	DLL1_LDO_FLT_EN	for debug only
[5]	rw	1'b0	DLL1_LDO_EN	for debug only
[4]	rw	1'b0	DLL1_DBG	for debug only
[3]	rw	1'b0	DBGCLK_EN	for debug only
[2:0]	rw	3'b0	DBGCLK_SEL	for debug only
0x40			**DBGR**	Debug Register
[31:5]			RSVD	
[4]	rw	1'h0	FORCE_HP	for debug only
[3]	rw	1'h0	FORCE_GPIO	for debug only
[2]	rw	1'h0	FORCE_BUS	for debug only
[1]	rw	1'h0	SYSCLK_SWLP	for debug only
[0]	rw	1'h0	SYSCLK_AON	for debug only

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表 2-7: HPSYS_RCC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x44			**DWCFGR**	Deep WFI mode Clock Configuration Register
[31:28]			RSVD	
[27]	rw	1'b0	DLL2_OUT_RSTB	for debug only
[26]	rw	1'b0	DLL2_OUT_EN	for debug only
[25]	rw	1'b0	DLL1_OUT_RSTB	for debug only
[24]	rw	1'b0	DLL1_OUT_EN	for debug only
[23:18]			RSVD	
[17:16]	rw	2'h0	SEL_SYS	select clk_hpsys source during deep WFI 0 - clk_hrc48; 1 - clk_hxt48; 2 - RSVD; 3 - clk_dll1
[15]	rw	1'h1	DIV_EN	enable PDIV1, PDIV2 and HDIV reconfiguration during deep wfi
[14:12]	rw	3'b000	PDIV2	pclk2_hpsys = hclk_hpsys / (2^{PDIV2}) during deep wfi. Valid PDIV2 is 1 to 7. 0 is not allowed.
[11]			RSVD	
[10:8]	rw	3'b000	PDIV1	pclk_hpsys = hclk_hpsys / (2^{PDIV1}) during deep wfi
[7:0]	rw	8'h30	HDIV	hclk_hpsys = clk_hpsys / HDIV during deep wfi
0x48			**SR1**	Status Register 1
[31]	r	1'h0	PTM1	0: module is idle; 1: module is working
[30]			RSVD	
[29]			RSVD	
[28]	r	1'h0	I2C2	0: module is idle; 1: module is working
[27]	r	1'h0	I2C1	0: module is idle; 1: module is working
[26]	r	1'h0	PDM2	0: module is idle; 1: module is working
[25]	r	1'h0	PDM1	0: module is idle; 1: module is working
[24]			RSVD	
[23]			RSVD	
[22]			RSVD	
[21]	r	1'h0	SPI2	0: module is idle; 1: module is working
[20]	r	1'h0	SPI1	0: module is idle; 1: module is working
[19]	r	1'h0	PWM1	0: module is idle; 1: module is working
[18]	r	1'h0	BTIM2	0: module is idle; 1: module is working
[17]	r	1'h0	BTIM1	0: module is idle; 1: module is working
[16]	r	1'h0	GPTIM2	0: module is idle; 1: module is working
[15]	r	1'h0	GPTIM1	0: module is idle; 1: module is working
[14]			RSVD	
[13]			RSVD	
[12]	r	1'h0	AES	0: module is idle; 1: module is working
[11]			RSVD	
[10]			RSVD	
[9]	r	1'h0	I2S2	0: module is idle; 1: module is working
[8]	r	1'h0	I2S1	0: module is idle; 1: module is working
[7]	r	1'h0	LCDC1	0: module is idle; 1: module is working
[6]	r	1'h0	EPIC	0: module is idle; 1: module is working
[5]	r	1'h0	EZIP1	0: module is idle; 1: module is working
[4]	r	1'h0	USART2	0: module is idle; 1: module is working
[3]	r	1'h0	USART1	0: module is idle; 1: module is working
[2]			RSVD	
[1]			RSVD	
[0]	r	1'h0	DMAC1	0: module is idle; 1: module is working

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表 2-7: HPSYS_RCC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x4C			**SR2**	Status Register 2
[31]	r	1'h0	ACPU	0: module is idle; 1: module is working
[30]	r	1'h0	HCPU	0: module is idle; 1: module is working
[29:26]			RSVD	
[25]	r	1'h0	I2C4	0: module is idle; 1: module is working
[24]	r	1'h0	JPEGD	0: module is idle; 1: module is working
[23]	r	1'h0	TSEN	0: module is idle; 1: module is working
[22]	r	1'h0	GPADC	0: module is idle; 1: module is working
[21]			RSVD	
[20]	r	1'h0	AUDPRC	0: module is idle; 1: module is working
[19]	r	1'h0	AUDCODEC	0: module is idle; 1: module is working
[18]	r	1'h0	CAN2	0: module is idle; 1: module is working
[17]	r	1'h0	CAN1	0: module is idle; 1: module is working
[16]			RSVD	
[15]			RSVD	
[14]			RSVD	
[13]	r	1'h0	DCMI	0: module is idle; 1: module is working
[12]	r	1'h0	USART3	0: module is idle; 1: module is working
[11]			RSVD	
[10]	r	1'h0	ATIM2	0: module is idle; 1: module is working
[9]	r	1'h0	ATIM1	0: module is idle; 1: module is working
[8]	r	1'h0	I2C3	0: module is idle; 1: module is working
[7]			RSVD	
[6]	r	1'h0	USBC	0: module is idle; 1: module is working
[5]	r	1'h0	SDMMC2	0: module is idle; 1: module is working
[4]	r	1'h0	SDMMC1	0: module is idle; 1: module is working
[3]	r	1'h0	MPI3	0: module is idle; 1: module is working
[2]	r	1'h0	MPI2	0: module is idle; 1: module is working
[1]	r	1'h0	MPI1	0: module is idle; 1: module is working
[0]			RSVD	
0x50			**RC10CAL1**	
[31]			RSVD	
[30]	rw	1'b0	CON_MODE	continous mode
[29:20]	rw	10'h0	CON_NUM	sampling times in continous mode
[19]	rw	1'b0	CAL_SEL	0: clk_lp; 1: clk_wdt
[18]	w1c	1'b0	CAL_STOP	Single pulse/Writing a 1 stop rccal module
[17]	w1c	1'b0	CAL_START	Single pulse/Writing a 1 trigger rccal module
[16]	rw	1'b0	CAL_AUTO	If rccal_auto is 1 then when sleep done the rccal module auto work
[15:0]	rw	16'h8	CAL_LENGTH	low power clk cycle count
0x54			**RC10CAL2**	
[31]	r	1'b0	CAL_DONE	When the rccal module is finish, the rccal_done set 1
[30:0]	r	31'h0	CAL_RSLT	When the rccal module is finish, the rccal_result contain ref_clk cycles

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3 电源管理

3.1 SF32LB57x 锂电池供电版本 (573/575/577 等)

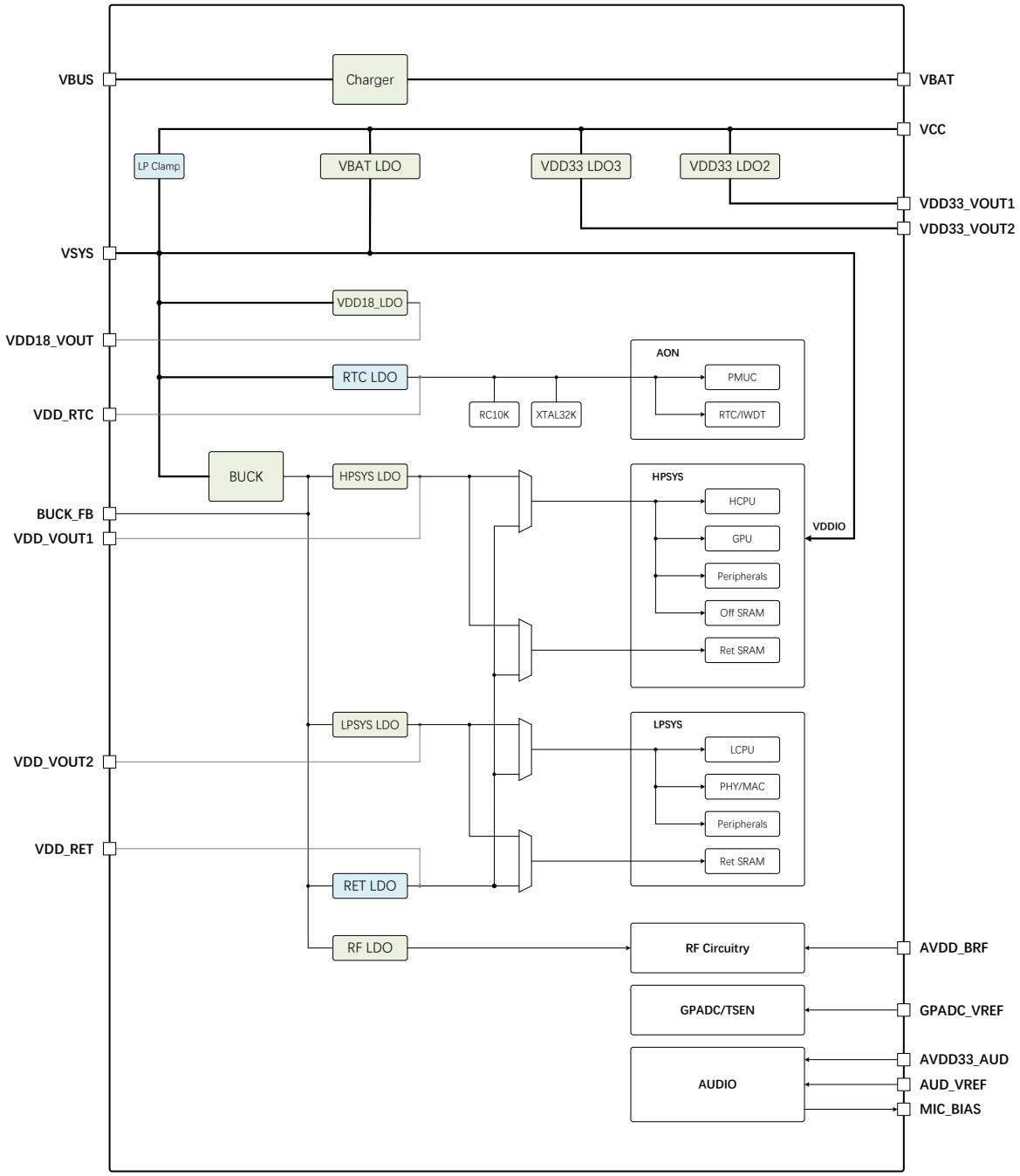


图 3-1: 57x 锂电池供电版本电源管理结构图

VBUS 与 VBAT 是充电相关电源管脚。当使用芯片内部充电方案时，VBUS 是充电输入，VBAT 是充电输出。当使用芯片外部充电方案时，VBAT 仅用于测量电池电压。

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VCC 是芯片的主供电输入，也是除充电管脚外唯一必须由外部电源 (如电池) 供电的管脚。VCC 通过下游的 LDO 产生芯片内部系统的主供电 VSYS，以及主要的输出供电 VDD33_VOUT1 和 VDD33_VOUT2。

除 VCC 外，芯片的其它供电输入包括模拟电路供电，音频电路供电，IO 供电以及合封存储器供电。

模拟电路供电输入 AVDD_BRF 可以连接至 VSYS，由 VSYS 供电。

音频电路供电输入 AVDD33_AUD 可以连接至 VDD33_VOUT1，由 VDD33_VOUT1 供电。

SF32LB57xU 芯片为 QFN68 封装，IO 供电由 VSYS 内部供电，典型电压为 3.3V。合封的 PSRAM 由 VDD18_VOUT 内部供电，合封的 FLASH 由 VDD33_VOUT1 内部供电。

SF32LB57xY 芯片为 QFN80 封装，IO 供电由 VDDIOA 输入管脚提供，典型电压为 1.8V/2.5V/3.3V。合封的 PSRAM 由 VDD18_VOUT 内部供电，合封的 FLASH 由 VDD33_VOUT1 内部供电。

SF32LB57xV 芯片为 BGA112 封装，IO 供电由 VDDIOA 输入管脚提供，典型电压为 1.8V/2.5V/3.3V。合封的 PSRAM 供电由 VDDIOSA 或 VDDIOSB 输入管脚提供，可以连接至 VDD18_VOUT。合封的 FLASH 供电由 VDDIOSB 输入管脚提供，可以连接至 VDD33_VOUT1。

如果合封存储器采用外部电源供电，为保证芯片进入 hibernate 模式时不漏电，该供电应当在芯片外部被 PA21 控制 (例如使用 PA21 作为外部电源开关的使能控制)。当芯片进入 hibernate 模式以后，PA21 表现为高阻，外部下拉电阻使得电源开关关闭；而芯片退出 hibernate 模式以后，PA21 自动输出高电平，开启供电。

VDD18_VOUT 由芯片内部的 VDD18_LDO 产生，可以为合封的 PSRAM 供电。

VDD33_VOUT1 由芯片内部的 VDD33_LDO2 产生，可以为音频供电输入和合封的 Flash 供电，同时能够挂载外部负载 (如外部 Flash，传感器等)。该 LDO 默认关闭，可通过 PMUC 的 PERI_LDO 寄存器开启。芯片启动时 (包括从 hibernate 模式唤醒)BOOTROM 会自动开启该 LDO。

VDD33_VOUT2 由芯片内部的 VDD33_LDO3 产生，可以挂载外部负载 (如马达，传感器等)。该 LDO 默认关闭，可通过 PMUC 的 PERI_LDO 寄存器开启。

VSYS 由芯片内部的 LDO 产生，是芯片内部系统的主供电。VSYS 可直接为 IO 提供供电，同时通过下游的 LDO 产生 VDD18_VOUT 和 VDD_RTC，并通过下游的 BUCK 产生 BUCK_FB。

VDD_RTC 由芯片内部的 LDO 产生，用于给芯片的低功耗模块供电。即使在 hibernate 模式下，该 LDO 也能一直保持工作。

BUCK_FB 由芯片内部的 BUCK 产生，用于给芯片的数字和模拟电路供电。该 BUCK 不能被旁路，也不可被外部 LDO 替代。芯片启动后 (包括从 hibernate 模式唤醒) 自动开启 BUCK，进入 hibernate 模式后自动关闭 BUCK。BUCK 的输出通过下游的 LDO 产生 VDD_VOUT1，VDD_VOUT2，VDD_RET 以及射频电路需要的部分供电。BUCK 的输出电压可根据软件配置，在不同工作场景下自动调节以节约功耗。

VDD_VOUT1 由芯片内部的 LDO 产生，是 HPSYS 的主要供电，输出电压可根据软件配置，在不同工作场景下自动调节以节约功耗。

VDD_VOUT2 由芯片内部的 LDO 产生，是 LPSYS 的主要供电，输出电压可根据软件配置，在不同工作场景下自动调节以节约功耗。

VDD_RET 由芯片内部的 LDO 产生，用于 deepsleep 和 standby 低功耗模式下的供电。

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MIC_BIAS 由芯片内部的 LDO 产生，用于为外部麦克风提供直流偏置电压。该 LDO 默认关闭，可通过 AUDCODEC 的寄存器开启并调节电压。

使用芯片内部充电方案时

表 3-1: 57x 锂电池供电版本电源管脚（内部充电方案）

电源管脚	方向	功能	典型电压 (V)
VBUS	输入	充电输入	5
VBAT	输出	充电输出，给电池充电并提供 VCC 供电	4
VCC	输入	芯片主供电，与电池和 VBAT 连接	4

使用芯片外部充电方案时

表 3-2: 57x 锂电池供电版本电源管脚（外部充电方案）

电源管脚	方向	功能	典型电压 (V)
VBAT (QFN68/BGA112)VBATS (QFN80)	输入	用于测量电池电压	4
VCC	输入	芯片主供电	4

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通用管脚

表 3-3: 57x 锂电池供电版本电源管脚（通用）

电源管脚	方向	功能	典型电压 (V)
AVDD_BRF	输入	模拟电路供电，可由 VSYS 提供	3.3
AVDD33 (QFN80)AVDD33_ANA (BGA112)	输入	模拟电路供电	3.3
AVDD33_AUD	输入	音频电路供电，可由 VDD33_VOUT1 提供	3.3
VDD18_VOUT	输出	给合封的 PSRAM 供电，由内部 VDD18_LDO 输出，默认关闭，需软件开启	1.8
VSYS	输出	芯片内部系统的主供电，同时输出给 AVDD_BRF 供电	3.3
VDD33_VOUT1	输出	VDD33_LDO2 的输出，可用于给合封的 Flash，AVDD33_AUD 以及外部 Flash 等外设供电。芯片启动后，在 BOOT ROM 中自动开启输出	3.3
VDD33_VOUT2	输出	VDD33_LDO3 的输出，可用于给外设供电。默认关闭，需软件开启	3.3
VDD_RTC	内部	内部 RTC_LDO 的输出	1.1
BUCK_FB	内部	内部 BUCK 的输出	1.25
VDD_VOUT1	内部	内部 HPSYS_LDO 的输出	1.1
VDD_VOUT2	内部	内部 LPSYS_LDO 的输出	0.9
VDD_RET	内部	内部 RET_LDO 的输出	0.7
GPADC_VREF	内部	GPADC 参考电压	
AUD_VREF	内部	音频参考电压	
MIC_BIAS	输出	MIC 电源输出。默认关闭，需软件开启	
VDDIOA (QFN80/BGA112)	输入	通用 IO(PA) 电源输入	1.8/2.5/3.3
VDDIOSA (仅 BGA112)	输入	SIP IO(SA) 电源输入，给 SA 合封的 PSRAM 供电，可连接到 VDD18_VOUT	1.8
VDDIOSB (仅 BGA112)	输入	SIP IO(SB) 电源输入，给 SB 合封的 PSRAM 供电，可连接到 VDD18_VOUT，或给 SB 合封的 FLASH 供电，可连接到 VDD33_VOUT1	1.8/3.3

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3.2 SF32LB57X 常规供电版本 (57E/57G/57Z 等)

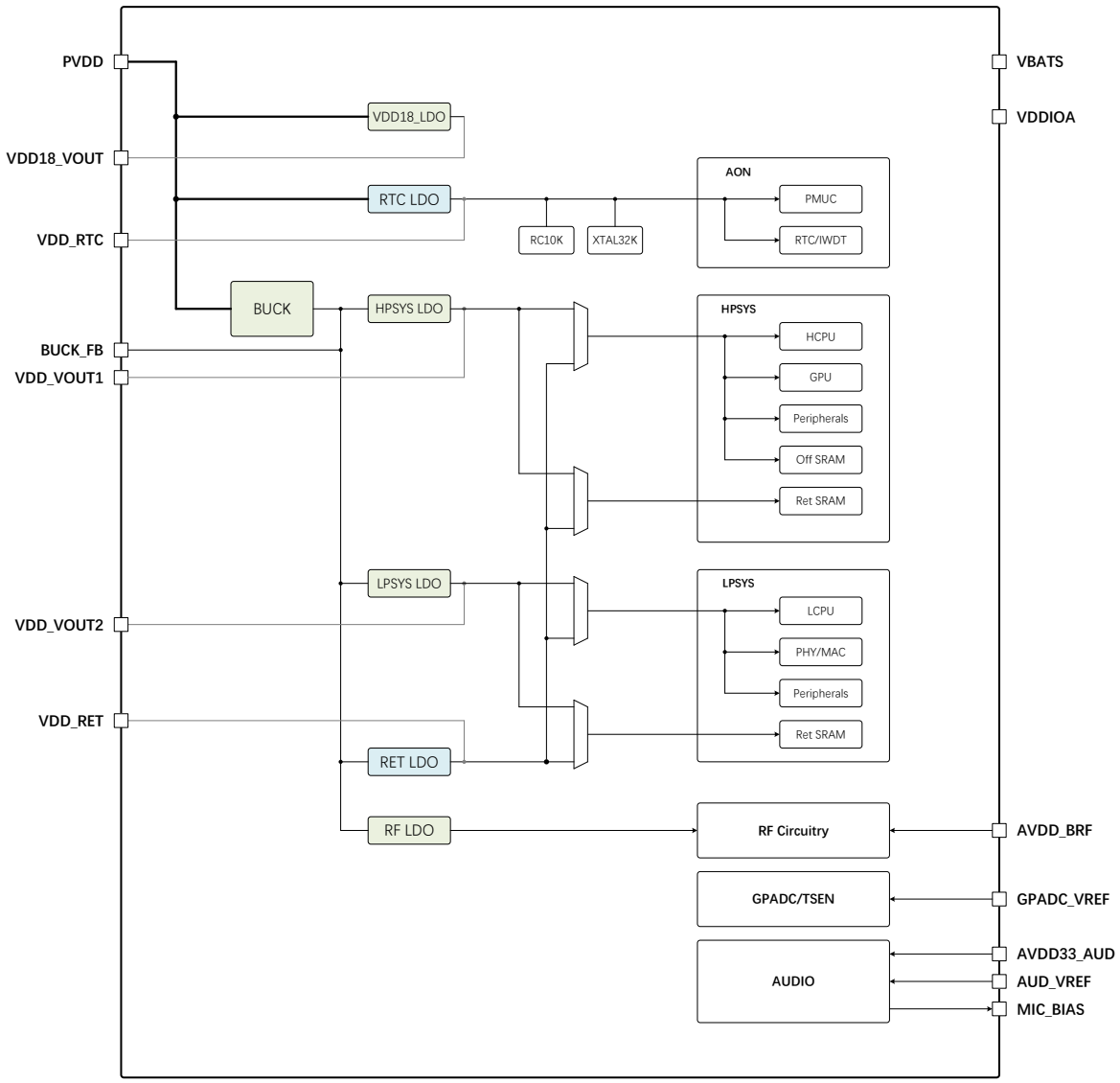


图 3-2: 57X 常规供电版本电源管理结构图

PVDD 是芯片的主供电输入，支持 1.8V 至 3.3V 电源供电。PVDD 通过下游的 LDO 产生 VDD18_VOUT 和 VDD_RTC，并通过下游的 BUCK 产生 BUCK_FB。

除 PVDD 外，芯片的其它供电输入还包括模拟电路供电，音频电路供电，IO 供电以及合封存储器供电。

芯片的模拟电路供电输入包括 AVDD_BRF 和 AVDD33。

芯片的音频电路供电输入是 AVDD33_AUD。

芯片的 IO 供电输入是 VDDIOA，典型电压为 1.8V/2.5V/3.3V。

SF32LB57XU 芯片为 QFN68 封装，合封的 PSRAM 由 VDD18_VOUT 内部供电，合封的 FLASH 由 VDDIOA 供电。

SF32LB57XY 芯片为 QFN80 封装，合封的 PSRAM 由 VDD18_VOUT 内部供电，合封的 FLASH 供电由 VDDIOSB

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输入管脚提供。

SF32LB57XV 芯片为 BGA112 封装，合封的 PSRAM 供电由 VDDIOSA 或 VDDIOSB 输入管脚提供，可以连接至 VDD18_VOUT。合封的 FLASH 供电由 VDDIOSB 输入管脚提供。

如果合封存储器采用外部电源供电，为保证芯片进入 hibernate 模式时不漏电，该供电应当在芯片外部被 PA21 控制 (例如使用 PA21 作为外部电源开关的使能控制)。当芯片进入 hibernate 模式以后，PA21 表现为高阻，外部下拉电阻使得电源开关关闭；而芯片退出 hibernate 模式以后，PA21 自动输出高电平，开启供电。

VDD_RTC 由芯片内部的 LDO 产生，用于给芯片的低功耗模块供电。即使在 hibernate 模式下，该 LDO 也能一直保持工作。

BUCK_FB 由芯片内部的 BUCK 产生，用于给芯片的数字和模拟电路供电。该 BUCK 不能被旁路，也不可被外部 LDO 替代。芯片启动后 (包括从 hibernate 模式唤醒) 自动开启 BUCK，进入 hibernate 模式后自动关闭 BUCK。BUCK 的输出通过下游的 LDO 产生 VDD_VOUT1，VDD_VOUT2，VDD_RET 以及射频电路需要的部分供电。BUCK 的输出电压可根据软件配置，在不同工作场景下自动调节以节约功耗。

VDD_VOUT1 由芯片内部的 LDO 产生，是 HPSYS 的主要供电，输出电压可根据软件配置，在不同工作场景下自动调节以节约功耗。

VDD_VOUT2 由芯片内部的 LDO 产生，是 LPSYS 的主要供电，输出电压可根据软件配置，在不同工作场景下自动调节以节约功耗。

VDD_RET 由芯片内部的 LDO 产生，用于 deepsleep 和 standby 低功耗模式下的供电。

MIC_BIAS 由芯片内部的 LDO 产生，用于为外部麦克风提供直流偏置电压。该 LDO 默认关闭，可通过 AUDCODEC 的寄存器开启并调节电压。

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表 3-4: 57X 常规供电版本电源管脚

电源管脚	方向	功能	典型电压 (V)
PVDD	输入	芯片主供电	3.3
VBATS	输入	用于测量电池电压,如无需求可不接	4
VDDIOA	输入	通用 IO(PA) 电源输入	1.8/3.3
VDDIOSA (仅 BGA112)	输入	SIP IO(SA) 电源输入，给 SA 合封的 PSRAM 供电，可连接到 VDD18_VOUT	1.8
VDDIOSB (QFN80/BGA112)	输入	SIP IO(SB) 电源输入，给 SB 合封的 PSRAM 供电，可连接到 VDD18_VOUT，或给 SB 合封的 FLASH 供电	1.8/3.3
AVDD_BRF	输入	模拟电路供电	3.3
AVDD33 (QFN68/QFN80)AVDD33_ANA (BGA112)	输入	模拟电路供电	3.3
AVDD33_AUD	输入	音频电路供电	3.3
VDD18_VOUT	输出	给合封的 PSRAM 供电，由内部 VDD18_LDO 输出，默认关闭，需软件开启	1.8
VDD_RTC	内部	内部 RTC_LDO 的输出	1.1
BUCK_FB	内部	内部 BUCK 的输出	1.25
VDD_VOUT1	内部	内部 HPSYS_LDO 的输出	1.1
VDD_VOUT2	内部	内部 LPSYS_LDO 的输出	0.9
VDD_RET	内部	内部 RET_LDO 的输出	0.7
GPADC_VREF	内部	GPADC 参考电压	
AUD_VREF	内部	音频参考电压	
MIC_BIAS	输出	MIC 电源输出。默认关闭，需软件开启	

3.3 充电模块

芯片集成了锂电池充电模块。充电电流和满电电压均可调节，充电电流最大支持 400mA。客户可根据电池规格和 VBUS 端线阻的大小，设置相应的参数。

图3-3是电池的充电曲线。当电池电压低于 V_{cc} 时，充电模块处于 Trickle Charge 模式，会以较低的电流 I_{tri} 给电池充电。当电池电压高于 V_{cc} 之后，充电模块处于 Constant Charge 模式，并且以恒流 I_{cc} 充电直到电池电压接近设置的满电电压 V_{cv}。之后，充电模块就进入 Constant Voltage 模式。在这个模式下，充电电流会慢慢下降，直到电流小于截止充电电流 I_{end}，充电环路自动断开，进入 Charger Full 模式。满电之后，如果电源适配器没有断开，那么电池电压经过一段时间消耗降低到 Re-Charge Threshold，会自动开启充电程序直到电池满电。

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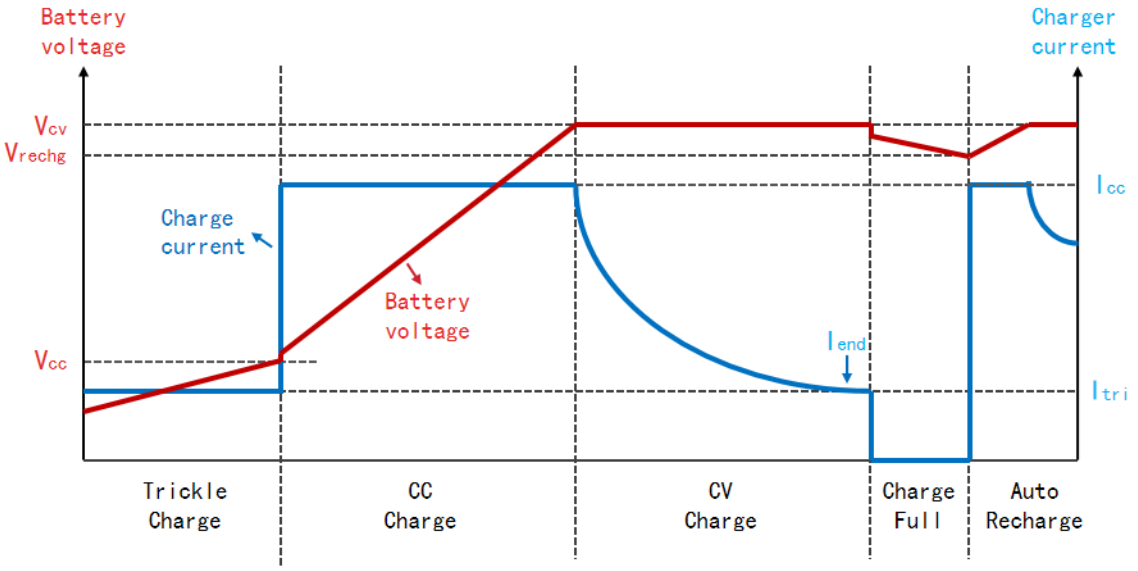


图 3-3: 充电曲线

3.4 PMUC 寄存器

PMUC 的基地址是 0x500CA000。

表 3-5: PMUC 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**CR**	Control Register
[31:12]			RSVD	
[11:8]	rw	4'h7	RST_CNT	Determine the reset pulse width for both LPSYSRST and SYSRSTREQ
[7:5]			RSVD	
[4]	rw	1'h0	LPSYSRST	Write 1 to resetn LPSYS, self-cleared when reset done
[3]	rw	1'h0	REBOOT	Write 1 to reboot; write 0 to clear after boot up
[2]	rw	1'h0	HIBER_EN	Write 1 to enter hibernate mode; write 0 to clear when exit from hibernate
[1]	rw	1'h0	SEL_RTC	Clock select for clk_rtc. 0: clk_lrc10, 1: clk_lxt32
[0]	rw	1'h0	SEL_WDT	Clock select for clk_wdt. 0: clk_lrc10, 1: clk_lxt32
0x04			**WER**	Wakeup Enable register
[31]			RSVD	
[30]	rw	1'b1	PWRKEY	Set 1 to enable PWRKEY to restart the whole chip
[29]	rw	1'b1	LOWBAT	Set 1 to enable LOWBAT to restart the whole chip
[28:26]			RSVD	
[25]	rw	1'b0	CHG	Set 1 to enable Charger event as wakeup source. See charger control register for details.
[24:18]			RSVD	
[17]	rw	1'b0	IWDT	Set 1 to enable IWDT 1st round timeout as wakeup source
[16]	rw	1'b0	RTC	Set 1 to enable RTC as wakeup source
[15:14]			RSVD	
[13]	rw	1'b0	PA27	Set 1 to enable PA27 as wakeup source
[12]	rw	1'b0	PA26	Set 1 to enable PA26 as wakeup source
[11]	rw	1'b0	PA25	Set 1 to enable PA25 as wakeup source
[10]	rw	1'b0	PA24	Set 1 to enable PA24 as wakeup source

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表 3-5: PMUC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[9]	rw	1'b0	PA42	Set 1 to enable PA42 as wakeup source
[8]	rw	1'b0	PA41	Set 1 to enable PA41 as wakeup source
[7]	rw	1'b0	PA40	Set 1 to enable PA40 as wakeup source
[6]	rw	1'b0	PA39	Set 1 to enable PA39 as wakeup source
[5]	rw	1'b0	PA38	Set 1 to enable PA38 as wakeup source
[4]	rw	1'b0	PA37	Set 1 to enable PA37 as wakeup source
[3]	rw	1'b0	PA36	Set 1 to enable PA36 as wakeup source
[2]	rw	1'b0	PA35	Set 1 to enable PA35 as wakeup source
[1]	rw	1'b0	PA34	Set 1 to enable PA34 as wakeup source
[0]	rw	1'b0	PA33	Set 1 to enable PA33 as wakeup source
0x08			**WSR**	Wakeup Status register
[31]			RSVD	
[30]	r	1'b0	PWRKEY	Indicates reset by PWRKEY
[29]	r	1'b0	LOWBAT	Indicates reset by LOWBAT
[28]	r	1'b0	IWDTRST	Indicates reset by IWDT 2nd round timeout
[27]	r	1'b0	SYSRSTREQ	Indicates reset by HCPU sysresetreq
[26]			RSVD	
[25]	r	1'b0	CHG	Indicates wakeup by charger event
[24:18]			RSVD	
[17]	r	1'b0	IWDT	Indicates wakeup by IWDT 1st round timeout
[16]	r	1'b0	RTC	Indicates wakeup by RTC
[15:14]			RSVD	
[13]	r	1'b0	PA27	Indicates wakeup by PA27
[12]	r	1'b0	PA26	Indicates wakeup by PA26
[11]	r	1'b0	PA25	Indicates wakeup by PA25
[10]	r	1'b0	PA24	Indicates wakeup by PA24
[9]	r	1'b0	PA42	Indicates wakeup by PA42
[8]	r	1'b0	PA41	Indicates wakeup by PA41
[7]	r	1'b0	PA40	Indicates wakeup by PA40
[6]	r	1'b0	PA39	Indicates wakeup by PA39
[5]	r	1'b0	PA38	Indicates wakeup by PA38
[4]	r	1'b0	PA37	Indicates wakeup by PA37
[3]	r	1'b0	PA36	Indicates wakeup by PA36
[2]	r	1'b0	PA35	Indicates wakeup by PA35
[1]	r	1'b0	PA34	Indicates wakeup by PA34
[0]	r	1'b0	PA33	Indicates wakeup by PA33
0x0C			**WCR**	Wakeup Clear register
[31]			RSVD	
[30]	w1c	1'b0	PWRKEY	Write 1 to clear PWRKEY reset flag
[29]	w1c	1'b0	LOWBAT	Write 1 to clear LOWBAT flag
[28]	w1c	1'b0	IWDTRST	Write 1 to clear IWDT reset flag
[27]	w1c	1'b0	SYSRSTREQ	Write 1 to clear SYSRSTREQ reset flag
[26:14]			RSVD	
[13]	w1c	1'b0	PA27	Write 1 to clear PA27 wakeup flag. Only valid if PIN wakeup is configured as edge trigger
[12]	w1c	1'b0	PA26	Write 1 to clear PA26 wakeup flag. Only valid if PIN wakeup is configured as edge trigger

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表 3-5: PMUC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11]	w1c	1'b0	PA25	Write 1 to clear PA25 wakeup flag. Only valid if PIN wakeup is configured as edge trigger
[10]	w1c	1'b0	PA24	Write 1 to clear PA24 wakeup flag. Only valid if PIN wakeup is configured as edge trigger
[9]	w1c	1'b0	PA42	Write 1 to clear PA42 wakeup flag. Only valid if PIN wakeup is configured as edge trigger
[8]	w1c	1'b0	PA41	Write 1 to clear PA41 wakeup flag. Only valid if PIN wakeup is configured as edge trigger
[7]	w1c	1'b0	PA40	Write 1 to clear PA40 wakeup flag. Only valid if PIN wakeup is configured as edge trigger
[6]	w1c	1'b0	PA39	Write 1 to clear PA39 wakeup flag. Only valid if PIN wakeup is configured as edge trigger
[5]	w1c	1'b0	PA38	Write 1 to clear PA38 wakeup flag. Only valid if PIN wakeup is configured as edge trigger
[4]	w1c	1'b0	PA37	Write 1 to clear PA37 wakeup flag. Only valid if PIN wakeup is configured as edge trigger
[3]	w1c	1'b0	PA36	Write 1 to clear PA36 wakeup flag. Only valid if PIN wakeup is configured as edge trigger
[2]	w1c	1'b0	PA35	Write 1 to clear PA35 wakeup flag. Only valid if PIN wakeup is configured as edge trigger
[1]	w1c	1'b0	PA34	Write 1 to clear PA34 wakeup flag. Only valid if PIN wakeup is configured as edge trigger
[0]	w1c	1'b0	PA33	Write 1 to clear PA33 wakeup flag. Only valid if PIN wakeup is configured as edge trigger
0x10			**VRTC_CR**	VRTC Control Register
[31:20]			RSVD	
[19:13]	rw	7'h0	RESERVE	for debug only
[12:9]	rw	4'h0	BOR_VT_TRIM	for debug only
[8]	rw	1'h1	BOR_EN	Brownout Reset Enable
[7:4]	rw	4'h7	VRTC_TRIM	for debug only
[3:0]	rw	4'hc	VRTC_VBIT	for debug only
0x14			**VRET_CR**	VRET Control Register
[31:22]			RSVD	
[21:16]	rw	6'h20	DLY	VRET_LDO power up delay in number of CLK_LP cycles
[15:14]			RSVD	
[13:10]	rw	4'h7	TRIM	for debug only
[9:6]			RSVD	
[5:2]	rw	4'h7	VBIT	for debug only
[1]	rw	1'h0	BM	for debug only
[0]	rw	1'h1	EN	for debug only
0x18			**LRC10_CR**	RC10K Control Register
[31]	r	1'b1	RDY	Indicates clk_lrc10 is ready
[30:18]			RSVD	
[17:14]	rw	4'h7	LDO_TRIM	for debug only
[13:10]	rw	4'hc	LDO_VBIT	for debug only
[9]	rw	1'h1	LDO_EN	for debug only
[8]	rw	1'h0	REFRES	for debug only
[7:6]	rw	2'h3	CHGCAP	for debug only

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表 3-5: PMUC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[5:4]	rw	2'h3	CHGCRT	for debug only
[3]	rw	1'h0	CMPBM2	for debug only
[2:1]	rw	2'h0	CMPBM1	for debug only
[0]	rw	1'h1	EN	set 1 to enable clk_lrc10
0x1C			**LRC32_CR**	RC32K Control Register
[31]	r	1'b0	RDY	Indicates clk_lrc32 is ready
[30:10]			RSVD	
[9:6]	rw	4'h6	RSEL	for debug only
[5:4]	rw	2'h0	CHGCRT	for debug only
[3]	rw	1'h0	CMPBM2	for debug only
[2:1]	rw	2'h0	CMPBM1	for debug only
[0]	rw	1'h1	EN	set 1 to enable clk_lrc32
0x20			**LXT_CR**	XTAL32K Control Register
[31]	r	1'h0	RDY	Indicates clk_lxt32 is ready
[30:16]			RSVD	
[15]	rw	1'h0	EXT_EN	use external 32K input from IO
[14]	rw	1'h1	CAP_SEL	for debug only
[13:10]	rw	4'hf	BMSTART	for debug only
[9]	rw	1'h1	BMSEL	for debug only
[8]	rw	1'h0	AMPCTRL_ENB	for debug only
[7:6]	rw	2'h2	AMP_BM	for debug only
[5:2]	rw	4'h2	BM	for debug only
[1]	rw	1'h0	RSN	for debug only
[0]	rw	1'h0	EN	set 1 to enable clk_lxt32
0x24			**AON_BG**	AON Bandgap Register
[31:6]			RSVD	
[5]	rw	1'h0	BUF_VOS_POLAR	for debug only
[4:3]	rw	2'h3	BUF_VOS_STEP	for debug only
[2:0]	rw	3'h0	BUF_VOS_TRIM	for debug only
0x28			**AON_LDO**	AON LDO Register
[31:24]			RSVD	
[23]			RSVD	
[22]	r	1'h0	VBUS_RDY	for debug only
[21:19]	rw	3'h4	VBUS_SET_VTHN	for debug only
[18:16]	rw	3'h6	VBUS_SET_VTHP	for debug only
[15]			RSVD	
[14]	r	1'h1	VBAT_RDY	for debug only
[13:11]	rw	3'h0	VBAT_SET_VTHN	for debug only
[10:8]	rw	3'h3	VBAT_SET_VTHP	for debug only
[7]			RSVD	
[6]	r	1'h0	VBAT_LDO_SWMODE	for debug only
[5]	rw	1'h1	VBAT_LDO_EN_SWMODE	for debug only
[4]	rw	1'h1	VBAT_LDO_EN_SS	for debug only
[3:0]	rw	4'h9	VBAT_LDO_SET_VOUT	for debug only
0x2C			**BUCK_CR1**	BUCK Control Register 1
[31]	r	1'h1	SS_DONE	for debug only
[30]	rw	1'h0	BG_BUF_VOS_POLAR	for debug only
[29:28]	rw	2'h3	BG_BUF_VOS_STEP	for debug only

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表 3-5: PMUC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[27:25]	rw	3'h0	BG_BUF_VOS_TRIM	for debug only
[24]	rw	1'b0	UVLO_X_BIAS	for debug only
[23]	rw	1'b0	ZCD_AON	for debug only
[22]	rw	1'b0	OCP_AON	for debug only
[21]	rw	1'b0	SEL_LX22	for debug only
[20]	rw	1'b0	SEL_IOCP_HI	for debug only
[19:17]	rw	3'h4	IOCP_TUNE	for debug only
[16:15]	rw	2'h1	COMP_IDYN_TUNE	for debug only
[14:13]	rw	2'h1	COMP_IQ_TUNE	for debug only
[12]	rw	1'h0	COMP_BM_AHI	for debug only
[11:9]	rw	3'h4	COT_CTUNE	for debug only
[8:6]	rw	3'h4	MOT_CTUNE	for debug only
[5]			RSVD	
[4]	rw	1'h0	BYPASS_UVLO	for debug only
[3]	rw	1'h0	BYPASS_OCP	for debug only
[2]	rw	1'h0	BYPASS_PG	for debug only
[1]	rw	1'h0	CTRL	for debug only
[0]	rw	1'h1	EN	for debug only
0x30			**BUCK_CR2**	BUCK Control Register 2
[31:28]	rw	4'h4	TDIS	Discharge for TDIS*4 LP clock cycles during reboot
[27:23]	rw	5'h3	SET_VOUT_L	for debug only
[22:18]	rw	5'ha	SET_VOUT_M	for debug only
[17]	rw	1'h0	FORCE_RDY	for debug only
[16]			RSVD	
[15:12]	rw	4'h0	L2M_CNT	for debug only
[11:8]	rw	4'h0	L2H_CNT	for debug only
[7:4]	rw	4'h0	M2H_CNT	for debug only
[3]	rw	1'h0	L2M_EN	for debug only
[2]	rw	1'h0	M2L_EN	for debug only
[1]	rw	1'h0	H2L_EN	for debug only
[0]	rw	1'h0	H2M_EN	for debug only
0x34			**BUCK_CR3**	BUCK Control Register 3
[31:7]			RSVD	
[6:4]	rw	3'h4	PSWDRV_BM	for debug only
[3:1]	rw	3'h4	OCP_BM	for debug only
[0]	rw	1'h1	EN_REFTRK	for debug only
0x38			**CHG_CR1**	Charger Control Register 1
[31:26]	rw	6'h32	CV_VCTRL	
[25:24]	rw	2'h0	CC_RANGE	
[23:19]	rw	5'hf	CC_MN	
[18:14]	rw	5'h10	CC_MP	
[13:8]	rw	6'h6	CC_VCTRL	
[7:2]	rw	6'hc	CC_ICTRL	
[1]	rw	1'b0	LOOP_EN	only available when CR3 FORCE_CTRL bit is set
[0]	rw	1'b0	EN	only available when CR3 FORCE_CTRL bit is set
0x3C			**CHG_CR2**	Charger Control Register 2
[31:28]	rw	4'h8	VBAT_RANGE	
[27]	rw	1'b0	RANGE_EOC	

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表 3-5: PMUC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[26:24]	rw	3'h3	BM_EOC	
[23:18]	rw	6'h3f	HIGH_VCTRL	
[17:12]	rw	6'h2b	REP_VCTRL	
[11:6]	rw	6'h25	PRECC_ICTRL	
[5:4]	rw	2'h2	PRECC_RANGE	
[3:0]	rw	4'h8	BG_PROG_V1P2	
0x40			**CHG_CR3**	Charger Control Register 3
[31]	rw	1'b0	FORCE_CTRL	When charger plugged out, this bit will auto reset
[30]	rw	1'b0	FORCE_RST	When charger plugged out, this bit will auto reset
[29:11]			RSVD	
[10:6]	rw	5'hf	DLY2	
[5:0]	rw	6'h3f	DLY1	
0x44			**CHG_CR4**	Charger Control Register 4
[31:29]	rw	3'h2	IM_EOC_MODE	
[28:26]	rw	3'h2	IM_CV_MODE	
[25:23]	rw	3'h2	IM_CC_MODE	
[22:20]	rw	3'h2	IM_ABOVE_CC	
[19:17]	rw	3'h3	IM_ABOVE_REP	
[16:14]	rw	3'h2	IM_VBAT_HIGH	
[13:11]	rw	3'h2	IM_VBUS_RDY	0: high level, 1: low level, 2: pos edge, 3: neg edge, others: both edge
[10:8]			RSVD	
[7]	rw	1'b0	IE_EOC	
[6]	rw	1'b0	IE_EOC_MODE	
[5]	rw	1'b0	IE_CV_MODE	
[4]	rw	1'b0	IE_CC_MODE	
[3]	rw	1'b0	IE_ABOVE_CC	
[2]	rw	1'b0	IE_ABOVE_REP	
[1]	rw	1'h0	IE_VBAT_HIGH	
[0]	rw	1'h0	IE_VBUS_RDY	
0x48			**CHG_CR5**	Charger Control Register 5
[31:24]			RSVD	
[23]	r	1'b0	IS_EOC	
[22]	r	1'b0	IS_EOC_MODE	
[21]	r	1'b0	IS_CV_MODE	
[20]	r	1'b0	IS_CC_MODE	
[19]	r	1'b0	IS_ABOVE_CC	
[18]	r	1'b0	IS_ABOVE_REP	
[17]	r	1'b0	IS_VBAT_HIGH	
[16]	r	1'b0	IS_VBUS_RDY	
[15:8]			RSVD	
[7]	w1c	1'b0	IC_EOC	
[6]	w1c	1'b0	IC_EOC_MODE	
[5]	w1c	1'b0	IC_CV_MODE	
[4]	w1c	1'b0	IC_CC_MODE	
[3]	w1c	1'b0	IC_ABOVE_CC	
[2]	w1c	1'b0	IC_ABOVE_REP	
[1]	w1c	1'b0	IC_VBAT_HIGH	
[0]	w1c	1'b0	IC_VBUS_RDY	

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表 3-5: PMUC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x4C			**CHG_SR**	Charger Status Register
[31:15]			RSVD	
[14:8]	r	7'h0	CHG_STATE	Charger finite state machine
[7]			RSVD	
[6]	r	1'b0	EOC_MODE	
[5]	r	1'b0	CV_MODE	
[4]	r	1'b0	CC_MODE	
[3]	r	1'b0	VBAT_ABOVE_CC_OUT	
[2]	r	1'b0	VBAT_ABOVE_REP_OUT	
[1]	r	1'b0	VBAT_HIGH_OUT	
[0]	r	1'b0	VBUS_RDY_OUT	
0x50			**HPSYS_LDO**	HPSYS LDO Control Register
[31:16]			RSVD	
[15:10]	rw	6'h8	DLY	HPSYS_LDO power up delay in CLK_LP cycles
[9:6]	rw	4'h0	VREF2	for debug only
[5:2]	rw	4'h5	VREF	for debug only
[1]	rw	1'b0	BP	
[0]	rw	1'b1	EN	
0x54			**LPSYS_LDO**	LPSYS LDO Control Register
[31:16]			RSVD	
[15:10]	rw	6'h8	DLY	LPSYS_LDO power up delay in CLK_LP cycles
[9:6]	rw	4'h0	VREF2	for debug only
[5:2]	rw	4'h7	VREF	for debug only
[1]	rw	1'b0	BP	
[0]	rw	1'b1	EN	
0x58			**HPSYS_SWR**	HPSYS Switch Register
[31:8]			RSVD	
[7]	rw	1'b0	NORET	for debug only
[6:4]	rw	3'h3	DLY	wait for N cycles before asserting RDY
[3:2]	rw	2'b01	PSW_RET	PSW value during DS/SB
[1:0]	rw	2'b10	PSW	for debug only
0x5C			**LPSYS_SWR**	LPSYS Switch Register
[31:8]			RSVD	
[7]	rw	1'b0	NORET	for debug only
[6:4]	rw	3'h3	DLY	wait for N cycles before asserting RDY
[3:2]	rw	2'b01	PSW_RET	PSW value during DS/SB
[1:0]	rw	2'b10	PSW	for debug only
0x60			**PERI_LDO**	Peripherals LDO
[31:23]			RSVD	
[22:19]	rw	4'hd	VDD33_LDO3_SET_VOUT	set VDD33_VOUT2 output voltage
[18]	rw	1'b0	VDD33_LDO3_PD_VOUT	0: diable VDD33_VOUT2 pull down resistor 1: enable VDD33_VOUT2 pull down resistor to speed up voltage drop after output disabled
[17]	rw	1'b1	VDD33_LDO3_EN_SS	
[16]	rw	1'b0	EN_VDD33_LDO3	0: diable VDD33_VOUT2 output 1: enable VDD33_VOUT2 output
[15]			RSVD	

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表 3-5: PMUC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[14:11]	rw	4'hd	VDD33_LDO2_SET_VOUT	set VDD33_VOUT1 output voltage output 3.3V at default value 4'h6
[10]	rw	1'b0	VDD33_LDO2_PD_VOUT	0: diable VDD33_VOUT1 pull down resistor 1: enable VDD33_VOUT1 pull down resistor to speed up voltage drop after output disabled
[9]	rw	1'b1	VDD33_LDO2_EN_SS	
[8]	rw	1'b0	EN_VDD33_LDO2	0: diable VDD33_VOUT1 output 1: enable VDD33_VOUT1 output
[7]	r	1'b0	LDO18_RDY	
[6:3]	rw	4'hd	LDO18_VREF_SEL	set VDD18_VOUT output voltage output 1.8V at default value 4'hc
[2]	rw	1'b0	LDO18_PD_VOUT	0: diable VDD18_VOUT pull down resistor 1: enable VDD18_VOUT pull down resistor to speed up voltage drop after output disabled
[1]	rw	1'b1	LDO18_EN_SS	
[0]	rw	1'b0	EN_LDO18	0: diable VDD18_VOUT output 1: enable VDD18_VOUT output
0x64			**PMU_TR**	PMU Test Register
[31:6]			RSVD	
[5:3]	rw	3'h0	PMU_DC_MR	for debug only
[2:0]	rw	3'h0	PMU_DC_TR	for debug only
0x68			**PMU_RSVD**	PMU Reserved Register
[31:24]	r	8'h0	RESERVE3	for debug only
[23:16]	rw	8'h0	RESERVE2	for debug only
[15:8]	rw	8'h0	RESERVE1	for debug only
[7:0]	rw	8'h0	RESERVE0	for debug only
0x6C			**HXT_CR1**	HXT48 Control Register 1
[31:30]			RSVD	
[29:20]	rw	10'h1ca	CBANK_SEL	for debug only
[19]	rw	1'b1	GM_EN	for debug only
[18:17]	rw	2'h0	LDO_FLT_RSEL	for debug only
[16:13]	rw	4'ha	LDO_VREF	for debug only
[12:11]	rw	2'h1	BUF_RF_STR	for debug only
[10:9]	rw	2'h1	BUF_AUD_STR	for debug only
[8]	rw	1'b0	BUF_AUD_EN	for debug only
[7:6]	rw	2'h1	BUF_DLL_STR	for debug only
[5]	rw	1'b0	BUF_DLL_EN	for debug only
[4:3]	rw	2'h1	BUF_DIG_STR	for debug only
[2]	rw	1'b1	BUF_DIG_EN	for debug only
[1]	rw	1'b1	BUF_EN	for debug only
[0]	rw	1'b1	EN	0: disable clk_hxt48 1: enable clk_hxt48
0x70			**HXT_CR2**	HXT48 Control Register 2
[31]	rw	1'b0	SLEEP_EN	for debug only
[30:29]	rw	2'h2	SDADC_CLKDIV2_SEL	for debug only
[28:27]	rw	2'h2	SDADC_CLKDIV1_SEL	for debug only
[26]	rw	1'b0	SDADC_CLKIN_EN	for debug only
[25:16]	rw	10'h32	IDAC	for debug only

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表 3-5: PMUC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[15]	rw	1'b0	IDAC_EN	for debug only
[14:13]	rw	2'h2	BUF_SEL3	for debug only
[12:11]	rw	2'h2	BUF_SEL2	for debug only
[10]	rw	1'h0	ACBUF_RSEL	for debug only
[9:8]	rw	2'h2	ACBUF_SEL	for debug only
[7:6]	rw	2'h1	AGC_VINDC	for debug only
[5:2]	rw	4'h8	AGC_VTH	for debug only
[1]	rw	1'b0	AGC_ISTART_SEL	for debug only
[0]	rw	1'b1	AGC_EN	for debug only
0x74			**HXT_CR3**	HXT48 Control Register 3
[31:10]			RSVD	
[9:4]	rw	6'd31	DLY	for debug only
[3:2]	rw	2'h1	BUF_OSLO_STR	for debug only
[1:0]	rw	2'h1	BUF_DAC_STR	for debug only
0x78			**HRC_CR1**	HRC48 Control Register 1
[31]	rw	1'b0	DLY	for debug only
[30]			RSVD	
[29:28]	rw	2'h0	CLKLP_STR	for debug only
[27:26]	rw	2'h2	CLKLP_SEL	for debug only
[25]	rw	1'b1	CLKLP_EN	for debug only
[24:23]	rw	2'h0	CLKHP_STR	for debug only
[22:21]	rw	2'h2	CLKHP_SEL	for debug only
[20]	rw	1'b1	CLKHP_EN	for debug only
[19]	rw	1'b0	CLK96M_EN	for debug only
[18:16]	rw	3'h0	TEMP_TRIM	for debug only
[15:5]	rw	11'h200	FREQ_TRIM	for debug only
[4:1]	rw	4'ha	LDO_VREF	for debug only
[0]	rw	1'b1	EN	0: disable clk_hrc48 1: enable clk_hrc48
0x7C			**HRC_CR2**	HRC48 Control Register 2
[31:12]			RSVD	
[11:9]	rw	3'h1	SS_FD_SEL	for debug only
[8]	rw	1'b0	SS_FD_SEL_FRC_EN	for debug only
[7]	rw	1'b1	SS_AVG0_EN	for debug only
[6]	rw	1'b0	SS_NSEL	for debug only
[5:4]	rw	2'h1	SS_CLK_SEL	for debug only
[3]	rw	1'b0	SS_EN	for debug only
[2:1]	rw	2'h0	IDWN_SEL	for debug only
[0]	rw	1'b0	CLKX2_EN	for debug only
0x80			**CAU_BGR**	CAU Bandgap Register
[31:11]			RSVD	
[10:7]	rw	4'ha	LPBG_VREF12	for debug only
[6:3]	rw	4'ha	LPBG_VREF06	for debug only
[2]	rw	1'b0	LPBG_EN	for debug only
[1]	rw	1'b0	HPBG_EN	for debug only
[0]	rw	1'b0	HPBG_VDDPSW_EN	for debug only
0x84			**CAU_TR**	CAU Test Register
[31:9]			RSVD	

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表 3-5: PMUC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[8:6]	rw	3'h0	CAU_DC_MR	for debug only
[5:3]	rw	3'h0	CAU_DC_BR	for debug only
[2:0]	rw	3'h0	CAU_DC_TR	for debug only
0x88			**CAU_RSVD**	CAU Reserved Register
[31:16]			RSVD	
[15:8]	r	8'h0	RESERVE1	for debug only
[7:0]	rw	8'h0	RESERVE0	for debug only
0x8C			**PWRKEY_CNT**	PowerKey Count Register
[31:20]			RSVD	
[19:4]	rw	16'h186a	RST_CNT	press high for RST_CNT*16 clk_wdt cycles to reset the whole chip
[3:0]			RSVD	
0x90			**HPSYS_VOUT**	
[31:4]			RSVD	
[3:0]	rw	4'ha	VOUT	for debug only
0x94			**LPSYS_VOUT**	
[31:4]			RSVD	
[3:0]	rw	4'h5	VOUT	for debug only
0x98			**BUCK_VOUT**	
[31:5]			RSVD	
[4:0]	rw	5'hd	VOUT	for debug only
0x9C			**WKUP_MODE**	Wakeup Mode Register
[31:28]			RSVD	
[27:26]	rw	2'h0	PA27_MODE	mode for wakeup of PA27
[25:24]	rw	2'h0	PA26_MODE	mode for wakeup of PA26
[23:22]	rw	2'h0	PA25_MODE	mode for wakeup of PA25
[21:20]	rw	2'h0	PA24_MODE	mode for wakeup of PA24
[19:18]	rw	2'h0	PA42_MODE	mode for wakeup of PA42
[17:16]	rw	2'h0	PA41_MODE	mode for wakeup of PA41
[15:14]	rw	2'h0	PA40_MODE	mode for wakeup of PA40
[13:12]	rw	2'h0	PA39_MODE	mode for wakeup of PA39
[11:10]	rw	2'h0	PA38_MODE	mode for wakeup of PA38
[9:8]	rw	2'h0	PA37_MODE	mode for wakeup of PA37
[7:6]	rw	2'h0	PA36_MODE	mode for wakeup of PA36
[5:4]	rw	2'h0	PA35_MODE	mode for wakeup of PA35
[3:2]	rw	2'h0	PA34_MODE	mode for wakeup of PA34
[1:0]	rw	2'h0	PA33_MODE	mode for wakeup of PA33 0: high level, 1: low level, 2: pos edge, 3: neg edge
0xA0			**WKUP_CNT**	Wakeup Count Register
[31:16]			RSVD	
[15:0]	rw	16'h3ff	PIN_DLY	PIN wakeup de-glitch for PIN_DLY cycles of clk_wdt
0xA4			**PRSR1**	PAD Retention Set Register 1
[31]	rw1s	1'b0	PA31	Write 1 to set PA31 retention
[30]	rw1s	1'b0	PA30	Write 1 to set PA30 retention
[29]	rw1s	1'b0	PA29	Write 1 to set PA29 retention
[28]	rw1s	1'b0	PA28	Write 1 to set PA28 retention
[27]	rw1s	1'b0	PA27	Write 1 to set PA27 retention
[26]	rw1s	1'b0	PA26	Write 1 to set PA26 retention
[25]	rw1s	1'b0	PA25	Write 1 to set PA25 retention

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表 3-5: PMUC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[24]	rw1s	1'b0	PA24	Write 1 to set PA24 retention
[23]	rw1s	1'b0	PA23	Write 1 to set PA23 retention
[22]	rw1s	1'b0	PA22	Write 1 to set PA22 retention
[21]	rw1s	1'b0	PA21	Write 1 to set PA21 retention
[20]	rw1s	1'b0	PA20	Write 1 to set PA20 retention
[19]	rw1s	1'b0	PA19	Write 1 to set PA19 retention
[18]	rw1s	1'b0	PA18	Write 1 to set PA18 retention
[17]	rw1s	1'b0	PA17	Write 1 to set PA17 retention
[16]	rw1s	1'b0	PA16	Write 1 to set PA16 retention
[15]	rw1s	1'b0	PA15	Write 1 to set PA15 retention
[14]	rw1s	1'b0	PA14	Write 1 to set PA14 retention
[13]	rw1s	1'b0	PA13	Write 1 to set PA13 retention
[12]	rw1s	1'b0	PA12	Write 1 to set PA12 retention
[11]	rw1s	1'b0	PA11	Write 1 to set PA11 retention
[10]	rw1s	1'b0	PA10	Write 1 to set PA10 retention
[9]	rw1s	1'b0	PA9	Write 1 to set PA09 retention
[8]	rw1s	1'b0	PA8	Write 1 to set PA08 retention
[7]	rw1s	1'b0	PA7	Write 1 to set PA07 retention
[6]	rw1s	1'b0	PA6	Write 1 to set PA06 retention
[5]	rw1s	1'b0	PA5	Write 1 to set PA05 retention
[4]	rw1s	1'b0	PA4	Write 1 to set PA04 retention
[3]	rw1s	1'b0	PA3	Write 1 to set PA03 retention
[2]	rw1s	1'b0	PA2	Write 1 to set PA02 retention
[1]	rw1s	1'b0	PA1	Write 1 to set PA01 retention
[0]	rw1s	1'b0	PA0	Write 1 to set PA00 retention
0xA8			**PRSR2**	PAD Retention Set Register 2
[31]	rw1s	1'b0	SA	Write 1 to set all SA retention
[30]	rw1s	1'b0	SB	Write 1 to set all SB retention
[29:26]			RSVD	
[25]	rw1s	1'b0	PA57	Write 1 to set PA57 retention
[24]	rw1s	1'b0	PA56	Write 1 to set PA56 retention
[23]	rw1s	1'b0	PA55	Write 1 to set PA55 retention
[22]	rw1s	1'b0	PA54	Write 1 to set PA54 retention
[21]	rw1s	1'b0	PA53	Write 1 to set PA53 retention
[20]	rw1s	1'b0	PA52	Write 1 to set PA52 retention
[19]	rw1s	1'b0	PA51	Write 1 to set PA51 retention
[18]	rw1s	1'b0	PA50	Write 1 to set PA50 retention
[17]	rw1s	1'b0	PA49	Write 1 to set PA49 retention
[16]	rw1s	1'b0	PA48	Write 1 to set PA48 retention
[15]	rw1s	1'b0	PA47	Write 1 to set PA47 retention
[14]	rw1s	1'b0	PA46	Write 1 to set PA46 retention
[13]	rw1s	1'b0	PA45	Write 1 to set PA45 retention
[12]	rw1s	1'b0	PA44	Write 1 to set PA44 retention
[11]	rw1s	1'b0	PA43	Write 1 to set PA43 retention
[10]	rw1s	1'b0	PA42	Write 1 to set PA42 retention
[9]	rw1s	1'b0	PA41	Write 1 to set PA41 retention
[8]	rw1s	1'b0	PA40	Write 1 to set PA40 retention
[7]	rw1s	1'b0	PA39	Write 1 to set PA39 retention

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表 3-5: PMUC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[6]	rw1s	1'b0	PA38	Write 1 to set PA38 retention
[5]	rw1s	1'b0	PA37	Write 1 to set PA37 retention
[4]	rw1s	1'b0	PA36	Write 1 to set PA36 retention
[3]	rw1s	1'b0	PA35	Write 1 to set PA35 retention
[2]	rw1s	1'b0	PA34	Write 1 to set PA34 retention
[1]	rw1s	1'b0	PA33	Write 1 to set PA33 retention
[0]	rw1s	1'b0	PA32	Write 1 to set PA32 retention
0xAC			**PRCR1**	PAD Retention Clear Register 1
[31]	rw1c	1'b0	PA31	Write 1 to clear PA31 retention
[30]	rw1c	1'b0	PA30	Write 1 to clear PA30 retention
[29]	rw1c	1'b0	PA29	Write 1 to clear PA29 retention
[28]	rw1c	1'b0	PA28	Write 1 to clear PA28 retention
[27]	rw1c	1'b0	PA27	Write 1 to clear PA27 retention
[26]	rw1c	1'b0	PA26	Write 1 to clear PA26 retention
[25]	rw1c	1'b0	PA25	Write 1 to clear PA25 retention
[24]	rw1c	1'b0	PA24	Write 1 to clear PA24 retention
[23]	rw1c	1'b0	PA23	Write 1 to clear PA23 retention
[22]	rw1c	1'b0	PA22	Write 1 to clear PA22 retention
[21]	rw1c	1'b0	PA21	Write 1 to clear PA21 retention
[20]	rw1c	1'b0	PA20	Write 1 to clear PA20 retention
[19]	rw1c	1'b0	PA19	Write 1 to clear PA19 retention
[18]	rw1c	1'b0	PA18	Write 1 to clear PA18 retention
[17]	rw1c	1'b0	PA17	Write 1 to clear PA17 retention
[16]	rw1c	1'b0	PA16	Write 1 to clear PA16 retention
[15]	rw1c	1'b0	PA15	Write 1 to clear PA15 retention
[14]	rw1c	1'b0	PA14	Write 1 to clear PA14 retention
[13]	rw1c	1'b0	PA13	Write 1 to clear PA13 retention
[12]	rw1c	1'b0	PA12	Write 1 to clear PA12 retention
[11]	rw1c	1'b0	PA11	Write 1 to clear PA11 retention
[10]	rw1c	1'b0	PA10	Write 1 to clear PA10 retention
[9]	rw1c	1'b0	PA9	Write 1 to clear PA09 retention
[8]	rw1c	1'b0	PA8	Write 1 to clear PA08 retention
[7]	rw1c	1'b0	PA7	Write 1 to clear PA07 retention
[6]	rw1c	1'b0	PA6	Write 1 to clear PA06 retention
[5]	rw1c	1'b0	PA5	Write 1 to clear PA05 retention
[4]	rw1c	1'b0	PA4	Write 1 to clear PA04 retention
[3]	rw1c	1'b0	PA3	Write 1 to clear PA03 retention
[2]	rw1c	1'b0	PA2	Write 1 to clear PA02 retention
[1]	rw1c	1'b0	PA1	Write 1 to clear PA01 retention
[0]	rw1c	1'b0	PA0	Write 1 to clear PA00 retention
0xB0			**PRCR2**	PAD Retention Clear Register 2
[31]	rw1c	1'b0	SA	Write 1 to clear all SB retention
[30]	rw1c	1'b0	SB	Write 1 to clear all SA retention
[29:26]			RSVD	
[25]	rw1c	1'b0	PA57	Write 1 to clear PA57 retention
[24]	rw1c	1'b0	PA56	Write 1 to clear PA56 retention
[23]	rw1c	1'b0	PA55	Write 1 to clear PA55 retention
[22]	rw1c	1'b0	PA54	Write 1 to clear PA54 retention

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表 3-5: PMUC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[21]	rw1c	1'b0	PA53	Write 1 to clear PA53 retention
[20]	rw1c	1'b0	PA52	Write 1 to clear PA52 retention
[19]	rw1c	1'b0	PA51	Write 1 to clear PA51 retention
[18]	rw1c	1'b0	PA50	Write 1 to clear PA50 retention
[17]	rw1c	1'b0	PA49	Write 1 to clear PA49 retention
[16]	rw1c	1'b0	PA48	Write 1 to clear PA48 retention
[15]	rw1c	1'b0	PA47	Write 1 to clear PA47 retention
[14]	rw1c	1'b0	PA46	Write 1 to clear PA46 retention
[13]	rw1c	1'b0	PA45	Write 1 to clear PA45 retention
[12]	rw1c	1'b0	PA44	Write 1 to clear PA44 retention
[11]	rw1c	1'b0	PA43	Write 1 to clear PA43 retention
[10]	rw1c	1'b0	PA42	Write 1 to clear PA42 retention
[9]	rw1c	1'b0	PA41	Write 1 to clear PA41 retention
[8]	rw1c	1'b0	PA40	Write 1 to clear PA40 retention
[7]	rw1c	1'b0	PA39	Write 1 to clear PA39 retention
[6]	rw1c	1'b0	PA38	Write 1 to clear PA38 retention
[5]	rw1c	1'b0	PA37	Write 1 to clear PA37 retention
[4]	rw1c	1'b0	PA36	Write 1 to clear PA36 retention
[3]	rw1c	1'b0	PA35	Write 1 to clear PA35 retention
[2]	rw1c	1'b0	PA34	Write 1 to clear PA34 retention
[1]	rw1c	1'b0	PA33	Write 1 to clear PA33 retention
[0]	rw1c	1'b0	PA32	Write 1 to clear PA32 retention
0xB4			**PBRCR**	PBR Control Register
[31:8]			RSVD	
[7:4]	rw	4'b0	DBG_SEL	reserved for debug
[3:2]			RSVD	
[1]	rw	1'b1	SNS	reserved for debug
[0]	rw	1'b1	RTO	reserved for debug
0xB8			**PBR0R**	PBR0 Register for PA24
[31:15]			RSVD	
[14:12]	rw	3'h0	SEL	select output value 0: value set by PBR0R_OUT 1: clk_rtc 2: selected by CR1_PINOUT_SEL0 in HPSYS_AON 3: selected by CR1_PINOUT_SEL1 in HPSYS_AON others: reserved
[11:10]			RSVD	
[9]	r	1'b0	IN	Input value
[8]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[7]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[6]	rw	1'b0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[5]	rw	1'b1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[4]	rw	1'b0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[3]	rw	1'b0	PE	Pull Enable. Logic HIGH enables week pull device
[2]	rw	1'b0	IE	Input Enable. Logic HIGH enables the input buffer
[1]	rw	1'b0	OE	Output enable. Active high
[0]	rw	1'h0	OUT	Output value if PBR0R_SEL is 0
0xBC			**PBR1R**	PBR1 Register for PA25

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表 3-5: PMUC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:15]			RSVD	
[14:12]	rw	3'h0	SEL	select output value 0: value set by PBR1R_OUT 1: clk_rtc 2: selected by CR1_PINOUT_SEL0 in HPSYS_AON 3: selected by CR1_PINOUT_SEL1 in HPSYS_AON others: reserved
[11:10]			RSVD	
[9]	r	1'b0	IN	Input value
[8]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[7]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[6]	rw	1'b0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[5]	rw	1'b1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[4]	rw	1'b0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[3]	rw	1'b0	PE	Pull Enable. Logic HIGH enables week pull device
[2]	rw	1'b0	IE	Input Enable. Logic HIGH enables the input buffer
[1]	rw	1'b0	OE	Output enable. Active high
[0]	rw	1'h0	OUT	Output value if PBR1R_SEL is 0
0xC0			**PBR2R**	PBR2 Register for PA26
[31:15]			RSVD	
[14:12]	rw	3'h0	SEL	select output value 0: value set by PBR2R_OUT 1: clk_rtc 2: selected by CR1_PINOUT_SEL0 in HPSYS_AON 3: selected by CR1_PINOUT_SEL1 in HPSYS_AON others: reserved
[11:10]			RSVD	
[9]	r	1'b0	IN	Input value
[8]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength
[7]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[6]	rw	1'b0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[5]	rw	1'b1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[4]	rw	1'b0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[3]	rw	1'b0	PE	Pull Enable. Logic HIGH enables week pull device
[2]	rw	1'b0	IE	Input Enable. Logic HIGH enables the input buffer
[1]	rw	1'b0	OE	Output enable. Active high
[0]	rw	1'h0	OUT	Output value if PBR2R_SEL is 0
0xC4			**PBR3R**	PBR3 Register
[31:15]			RSVD	
[14:12]	rw	3'h0	SEL	select output value 0: value set by PBR3R_OUT 1: clk_rtc 2: selected by CR1_PINOUT_SEL0 in HPSYS_AON 3: selected by CR1_PINOUT_SEL1 in HPSYS_AON others: reserved
[11:10]			RSVD	
[9]	r	1'b0	IN	Input value
[8]	rw	1'b0	DS1	Drive Select 1. Used to select output drive strength

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表 3-5: PMUC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7]	rw	1'b1	DS0	Drive Select 0. Used to select output drive strength
[6]	rw	1'b0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[5]	rw	1'b1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[4]	rw	1'b0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[3]	rw	1'b0	PE	Pull Enable. Logic HIGH enables week pull device
[2]	rw	1'b0	IE	Input Enable. Logic HIGH enables the input buffer
[1]	rw	1'b0	OE	Output enable. Active high
[0]	rw	1'h0	OUT	Output value if PBR3R_SEL is 0
0xC8			**PAWK1R**	PA Wakeup Register 1
[31:10]			RSVD	
[9:0]	rw	10'h0	PE	Pull enable of wakeup pin, active high. Keep effective during hibernate mode. Caution: Pull-functions of all pins can be configured in HPSYS_PINMUX registers, but in hibernate mode, such information will be lost, which may lead to wakup pin leakage. Pull-functions set here will keep active in hibernate mode for wakeup pins to avoid leakage. bit 0: pull enable of PA33 bit 1: pull enable of PA34 ..... bit 9: pull enable of PA42
0xCC			**PAWK2R**	PA Wakeup Register 2
[31:10]			RSVD	
[9:0]	rw	10'h0	PS	Pull select of wakeup pin. Logic HIGH selects pull-up, logic LOW select pull-down. Keep effective during hibernate mode. bit 0: pull select of PA33 bit 1: pull select of PA34 ..... bit 9: pull select of PA42
0xD0			**PAWK3R**	PA Wakeup Register 3
[31:10]			RSVD	
[9:0]	rw	10'h3ff	IS	Input Select of wakeup pin. Logic LOW selects CMOS input, logic HIGH selects Schmitt input. Keep effective during hibernate mode. bit 0: input select of PA33 bit 1: input select of PA34 ..... bit 9: input select of PA42

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4 低功耗模式

4.1 简介

芯片支持多种低功耗模式，可满足不同场景下的低功耗需求。

4.2 主要工作模式汇总

芯片 HPSYS 子系统的主要工作模式见下表。除 active 模式外，其它模式均为低功耗模式。

表 4-1: 芯片工作模式

模式	CPU	外设	SRAM	IO	LPTIM	唤醒源	唤醒时间
Active	run	run	可访问	可翻转	run	/	/
Sleep	stop	run	可访问	可翻转	run	任意中断	<1us
Deepsleep	stop	stop	不可访问，全保留	电平保持	run	RTC,IWDT 唤醒 PIN, IO(PA), LPTIM1, 蓝牙	~250us
Standby	reset	reset	不可访问，保留 384KB	电平保持	run	RTC,IWDT 唤醒 PIN,CHG LPTIM1, 蓝牙	~1ms
Hibernate	reset	reset	不可访问，不保留	高阻/上拉/下拉	reset	RTC,IWDT, 唤醒 PIN,CHG	>2ms

LPSYS 子系统专门用于蓝牙通信，会根据蓝牙行为自动进出低功耗模式，并会在需要时自动唤醒 HPSYS。

4.2.1 Active 模式

处于 Active 模式 CPU 与外设正常运行，SRAM 可访问，IO 可正常翻转。为降低运行时的功耗，可以为 CPU 与外设选择合适的时钟源与时钟频率，并仅在外设工作时打开外设的模块使能。Active 模式下，HPSYS 可以工作在基础模式或增强模式，以满足低功耗或高性能运行等场景的需求。

在基础工作模式下 HCPU 最高工作频率为 48MHz，MPI 最高工作频率为 48MHz，主要用于传感器收集，简单算法运算等低功耗场景。在增强工作模式下 HCPU 最高工作频率为 240MHz，主要用于图像和音频处理，复杂算法运算等高性能场景。

芯片启动以后，默认处于基础工作模式。HCPU 需首先对各项电源相关配置进行初始化，随后可以在基础模式和增强模式之间切换。HCPU 执行下述操作可以切换到增强工作模式：

1. 将 HPSYS_CFG 的 SYSCR_LDO_VSEL 置 0；
2. 延时 1ms，延时过程中可并行开启 clk_hxt48 和 clk_dll1 等高速时钟；

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3. 将 HPSYS_CFG 的 ULPMCR 寄存器配置为 0x00130213；
4. clk_hpsys 切换到 clk_dll1 上，MPI 工作时钟也可切换到高速时钟上。

HCPU 执行下述操作可以切换到基础工作模式：

1. clk_hpsys 切换到 clk_hrc48 上，MPI 工作时钟切换到 clk_peri_hpsys，关闭高速时钟；
2. 将 HPSYS_CFG 的 ULPMCR 寄存器配置为 0x00120292；
3. 将 HPSYS_CFG 的 SYSCR_LDO_VSEL 置 1；

HCPU 空闲时，可以进入低功耗模式。所有低功耗模式仅能从 active 模式进入，并且退出时统一回到 active 模式。

4.2.2 Sleep 模式

处于 sleep 模式时，CPU 暂停执行指令，外设仍正常运行，SRAM 可访问，IO 可正常翻转。

HPSYS_AON 的 PMR.MODE 寄存器为 0 时，HCPU 执行 WFI 或 WFE 指令可进入 sleep 模式。HCPU 收到任何已使能的中断请求后退出 sleep 模式，从进入 sleep 模式之前的位置继续执行。

4.2.3 Deepsleep 模式

处于 deepsleep 模式时，系统内大部分时钟均被关闭，仅保留低功耗时钟。CPU 与外设均停止运行。SRAM 不可访问，内容均可保留。配置为输出的 IO(除 PA24~PA27 外) 不可翻转，保持进入 deepsleep 模式之前的电平不变。

HPSYS 进入 deepsleep 模式的流程为：

1. 确保 HPSYS 各外设 (除 LPTIM1) 的工作任务已完成；
2. HCPU 处理完毕当前已上报的中断；
3. HCPU 通过 NVIC 寄存器关闭所有中断使能，避免产生 SysTick, SVCall 和 PendSV 等异常，并将 PRIMASK 置 1；
4. 时钟 clk_hpsys 切换到 clk_hrc48，关闭 clk_dll1/2/3 等高速时钟；
5. 在 HPSYS_AON 中设置唤醒源；
6. 将 HPSYS_AON 的 ISSR.HP_ACTIVE 置 0；
7. 将 HPSYS_AON 的 ANACR.VHP_ISO 置 1；
8. 将 HPSYS_AON 的 PMR.MODE 寄存器配置为 2；
9. HCPU 执行 WFI 指令。

上述流程执行之后，如果仍有中断未关闭而产生了中断或异常请求，本次进入 deepsleep 模式失败，CPU 会保留在 active 模式继续运行。如果发生这种情况，可以在处理完当前中断后重新尝试进入 deepsleep 模式。

为方便调试，在上述第 7 步向 PMR.MODE 寄存器写入 0x80000002，即可无视当前中断状态，强制进入 deepsleep 模式。

deepsleep 模式主要的唤醒源包括 RTC，IWDT, CHG(充电插入), 唤醒 PIN，IO(PA)，LPTIM1，以及来自 LPSYS 的唤醒请求和 MAILBOX2。除唤醒 PIN 外的唤醒源通过 HPSYS_AON 的 WER 寄存器配置。唤醒 PIN 通过 PMUC 的 WER 寄存器配置。

唤醒源生效时，子系统经过一段初始化时间 (约 250us) 后退出 deepsleep 模式，回到 active 模式。CPU，外设以及内存的状态均未丢失，CPU 可从进入 deepsleep 时的位置 (WFI 指令之后) 继续运行。

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退出 deepsleep 模式时，子系统会产生 AON 中断。CPU 应首先运行相应恢复流程。

HPSYS 从 deepsleep 模式退出后，HCPU 的建议恢复流程为：

1. 将 HPSYS_AON 的 PMR.MODE 寄存器配置为 0；
2. 将 HPSYS_AON 的 ANACR.VHP_ISO 置 0；
3. 通过 NVIC 寄存器使能 AON 中断，并将 PRIMASK 置 0；
4. 在 AON 中断中，通过 HPSYS_AON 和 PMUC 的 WSR 寄存器查询唤醒源并进行相应处理，并通过 HPSYS_AON 和 PMUC 的 WCR 寄存器清除 AON 中断标志位；
5. 将 HPSYS_AON 的 ISSR.HP_ACTIVE 置 1；
6. 通过 NVIC 寄存器使能 HCPU 其它中断；
7. 如有需要，重新开启高速时钟。

HCPU 清除唤醒源标志时应当注意，只有 PIN 唤醒的标志是通过 PMUC 的 WCR 寄存器清除，而其它唤醒源标志则需要配置产生唤醒源的对应模块来清除。

从 deepsleep 模式退出后，子系统时钟来自于 clk_hrc48，如果需要切换到其它时钟上，应当重新打开所需的时钟源。

从 deepsleep 模式退出后，子系统内各外设的寄存器内容不会被复位，各外设也保持进入 deepsleep 模式之前的状态

4.2.4 Standby 模式

处于 standby 模式时，系统内大部分时钟与供电均被关闭，仅保留低功耗模块的时钟与供电。CPU 与外设均被复位。SRAM 不可访问，可保留 384KB(0x20020000~0x2007ffff)。配置为输出的 IO(除 PA24~PA27 外) 不可翻转，保持进入 standby 模式之前的电平不变。

HPSYS 进入 standby 模式的流程为：

1. 确保 HPSYS 各外设 (除 LPTIM1) 的工作任务已完成；
2. 在 HPSYS 的保留 SRAM 中备份 SRAM 内容和外设状态；
3. HCPU 处理完毕当前已上报的中断；
4. HCPU 通过 NVIC 寄存器关闭所有中断使能，避免产生 SysTick,SVCall 和 PendSV 等异常，并将 PRIMASK 置 1；
5. 时钟 clk_hpsys 切换到 clk_hrc48；
6. 在 HPSYS_AON 中设置唤醒源；
7. 将 HPSYS_AON 的 ISSR.HP_ACTIVE 置 0；
8. 将 HPSYS_AON 的 ANACR.VHP_ISO 置 1；
9. 在 PMUC 的 PRSR1 和 PRSR2 中将需要 retention 的 IO 对应寄存器置 1；
10. 将 HPSYS_AON 的 PMR.MODE 寄存器配置为 3；
11. HCPU 执行 WFI 指令。

上述流程执行之后，如果仍有中断未关闭而产生了中断或异常请求，本次进入 standby 模式失败，CPU 会保留在 active 模式继续运行。如果发生这种情况，可以在处理完当前中断后重新尝试进入 standby 模式。

为方便调试，在上述第 9 步向 PMR.MODE 寄存器写入 0x80000003，即可无视当前中断状态，强制进入 standby

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模式。

HPSYS 处于 standby 模式时，主要的唤醒源包括 RTC，IWDT, CHG(充电插入), 唤醒 PIN，LPTIM1，以及来自 LPSYS 的唤醒请求和 MAILBOX2。除唤醒 PIN 外的唤醒源通过 HPSYS_AON 的 WER 寄存器配置。唤醒 PIN 通过 PMUC 的 WER 寄存器配置。

唤醒源生效时，系统经过一段初始化时间 (约 1ms) 后退出 standby 模式，回到 active 模式。CPU 和外设的状态均被复位，SRAM 保留 384KB，CPU 从 ROM 中的 0 地址开始运行，并查询 HPSYS_AON 或 LPSYS_AON 的 PMR.MODE 寄存器，选择不同的运行分支。

退出 standby 模式时，子系统会产生 AON 中断。CPU 从 ROM 程序中跳出后，应首先运行相应恢复流程。

HPSYS 从 standby 模式退出后，HCPU 的建议恢复流程为：

1. 将 HPSYS_AON 的 PMR.MODE 与 ANACR 寄存器配置为 0；
2. 通过 NVIC 寄存器使能 AON 中断；
3. 在 AON 中断中，通过 HPSYS_AON 和 PMUC 的 WSR 寄存器查询唤醒源并进行相应处理，并通过 HPSYS_AON 的 WCR 寄存器清除 AON 中断标志位；
4. 重新配置 IO 功能；
5. 将 PMUC 的 PRSR1 和 PRSR2 清 0 以撤销 IO 的 retention 状态；
6. 将 HPSYS_AON 的 ISSR.HP_ACTIVE 置 1；
7. 重新开启高速时钟；
8. 从 HPSYS 的保留 SRAM 中恢复外设配置和 SRAM 内容；
9. 通过 NVIC 寄存器使能 HCPU 其它中断。

HCPU 清除唤醒源标志时应当注意，只有 PIN 唤醒的标志是通过 PMUC 的 WCR 寄存器清除，而其它唤醒源标志则需要配置产生唤醒源的对应模块来清除。

从 standby 模式退出后，子系统的系统时钟来自于 clk_hrc48，如果需要切换到其它时钟上，应当重新打开所需的时钟源。

从 standby 模式退出后，除低功耗外设 (如 LPTIM) 外，子系统内各外设均被复位，使用前应当恢复配置或重新初始化。外设状态可以在进入 standby 模式之前备份在具有 retention 功能的 SRAM 或 PSRAM 中，备份的内容在进出 standby 模式后不会被清除。

4.2.5 Hibernate 模式

Hibernate 模式是芯片的最低功耗模式。该模式下芯片大部分时钟与供电均被关闭，仅保留部分低功耗模块的时钟与供电。CPU，外设，HPSYS(包括 HPSYS_AON)，LPSYS(包括 LPSYS_AON) 所有寄存器均被复位。所有 SRAM 内容均不保留。唤醒 PIN 可配置为高阻，上拉或下拉，其它 IO 进入高阻状态。

Hibernate 模式适用于关机或货架/船运模式。

进入 hibernate 模式的流程为：

1. 在 PMUC 的 WER 寄存器中设置唤醒源；
2. 将 PMUC 的 CR_HIBER_EN 置 1。

Hibernate 模式的唤醒源包括 RTC, IWDT, CHG(充电插入) 和唤醒 PIN。支持唤醒 PIN 功能的 IO 仍可保持上下拉

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电阻生效 (配置位于 PMUC 寄存器，因此不会丢失)。

Hibernate 模式的唤醒源包括 RTC 和唤醒 PIN。支持唤醒 PIN 功能的 IO 仍可保持上下拉电阻生效 (配置位于 RTC 寄存器，因此不会丢失)。

唤醒源生效时，芯片经过一段初始化时间 (>2ms) 后退出 hibernate 模式，回到 active 模式。HCPU 从 ROM 中的 0 地址开始运行。此时 PMUC 的 CR_HIBER_EN 寄存器仍然为 1，CPU 可据此获知此次启动是从 hibernate 模式退出，可进行相应处理并将 CR_HIBER_EN 清 0。

从 hibernate 模式退出后，子系统的系统时钟来自于 clk_hrc48，如果需要切换到其它时钟上，应当重新打开所需的时钟源。

从 hibernate 模式退出后，除 PMUC，RTC 和 IWDT 外，其它模块均被复位，使用前应当重新初始化。

4.2.6 低功耗模式下的调试器行为

芯片进入低功耗模式以后，调试难度增加，最主要的表现是调试器断开或无法连接。UART 调试器默认通过 PA18 和 PA19 两个 IO 连接。SWD 调试器默认通过 PA43 和 PA44 两个 IO 连接。

调试器连接 HCPU 时，出现如下情况会断开且无法重新连接：

1. 调试器的 IO 功能被更改；
2. 使用 UART 调试器时，USART1 或 DMAC1 模块被复位，或时钟被关闭；
3. HPSYS 处于 deepsleep 或 standby 模式；
4. 芯片处于 hibernate 模式。

HPSYS 从 deepsleep 或 standby 模式唤醒，并且 HPSYS_AON 的 ISSR.HP_ACTIVE 置 1 以后，调试器可以重新连接 HCPU 并访问 HPSYS 地址空间。

4.2.7 判断当前低功耗模式

通过测量芯片的电源管脚电压，可以判断当前处于何种低功耗模式。当 HPSYS 处于 active 或 sleep 模式时，LDO1_VOUT 电压保持 1.0V(基础模式) 或 1.2V(增强模式)。当 HPSYS 处于 deepsleep 模式时，LDO1_VOUT 电压保持 0.7V。当 HPSYS 处于 standby 模式时，LDO1_VOUT 电压无法保持，会逐渐下降到 0V。当芯片进入 hibernate 模式时，LDO1_VOUT 和 VDD_RET 都下降到 0V。

表 4-2: 低功耗模式下的电源管脚电压

HPSYS	VDD_VOUT1	VDD_RET	VDD_RTC
active/ sleep/	1.0V/1.2V	0.7V	1.1V
deepsleep	0.7V	0.7V	1.1V
standby	0V	0.7V	1.1V
hibernate	0V	0V	1.1V
power off	0V	0V	0V

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4.3 HPSYS_AON 寄存器

HPSYS_AON 的基地址是 0x500C0000。

表 4-3: HPSYS_AON 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**PMR**	Power Mode Register
[31]	w1s	1'b0	FORCE_SLEEP	Set 1 to force enter low power mode. Will be cleared automatically
[30:2]			RSVD	
[1:0]	rw	2'h0	MODE	Power Mode: 2'h0 - active/idle; 2'h1 - light sleep; 2'h2 - deep sleep; 2'h3 - standby
0x04			**CR**	Control Register
[31]	rw	1'h0	GTIM_EN	Enable global timer
[30:8]			RSVD	
[7:4]	rw	4'h0	PINOUT_SEL1	select output to PBR 2: inverted LPTIM1 PWM output 3: inverted LPTIM2 PWM output others: reserved
[3:0]	rw	4'h0	PINOUT_SEL0	select output to PBR 2: LPTIM1 PWM output 3: LPTIM2 PWM output others: reserved
0x08			**ACR**	Active Mode Control register
[31]	r	1'b0	HXT48_RDY	Indicate hxt48 is ready
[30]	r	1'b0	HRC48_RDY	Indicate hrc48 is ready
[29:4]			RSVD	
[3]	rw	1'b0	EXTPWR_REQ	for debug only
[2]	rw	1'b1	PWR_REQ	Request power during Active mode
[1]	rw	1'b1	HXT48_REQ	Request hxt48 in active mode
[0]	rw	1'b1	HRC48_REQ	Request hrc48 in active mode
0x0C			**LSCR**	Light Sleep Ctrl Register
[31:4]			RSVD	
[3]	rw	1'b0	EXTPWR_REQ	for debug only
[2]	rw	1'b1	PWR_REQ	Request power during Light Sleep mode
[1]	rw	1'b1	HXT48_REQ	Request hxt48 in Light Sleep mode
[0]	rw	1'b1	HRC48_REQ	Request hrc48 in Light Sleep mode
0x10			**DSCR**	Deep Sleep Ctrl Register
[31:4]			RSVD	
[3]	rw	1'b0	EXTPWR_REQ	for debug only
[2]	rw	1'b0	PWR_REQ	Request power during Deep Sleep mode
[1]	rw	1'b0	HXT48_REQ	Request hxt48 in Deep Sleep mode
[0]	rw	1'b0	HRC48_REQ	Request hrc48 in Deep Sleep mode
0x14			**SBCR**	Standby Mode Ctrl Register
[31:9]			RSVD	
[8]	rw	1'h0	PD_RAM2	for debug only
[7]	rw	1'h0	PD_RAM1	for debug only
[6]	rw	1'h0	PD_RAM0	for debug only
[5:4]			RSVD	
[3]	rw	1'b0	EXTPWR_REQ	for debug only
[2]	rw	1'b0	PWR_REQ	Request power during Standby mode

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表 4-3: HPSYS_AON 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	rw	1'b0	HXT48_REQ	Request hxt48 in Standby mode
[0]	rw	1'b0	HRC48_REQ	Request hrc48 in Standby mode
0x18			**WER**	Wakeup Enable register
[31:26]			RSVD	
[25]	rw	1'b0	CHG	Set 1 to enable Charger event as wakeup source
[24]			RSVD	
[23]	rw	1'b0	LP2HP_IRQ	Set 1 to enable MAILBOX2 as wakeup source
[22]	rw	1'b0	LP2HP_REQ	Set 1 to enable LPSYS request as wakeup source
[21]	rw	1'b0	LP2HP_WDT	Set 1 to enable WDT2 2nd timeout as wakeup source
[20]	rw	1'b0	LPTIM1OUT	Set 1 to enable LPTIM1OUT as periodic wakeup source
[19]	rw	1'b0	LPTIM1	Set 1 to enable LPTIM1 as wakeup source
[18]	rw	1'b0	GPIO1	Set 1 to enable IO(PA) as wakeup source
[17]	rw	1'b0	IWDT	Set 1 to enable IWDT as wakeup source
[16]	rw	1'b0	RTC	Set 1 to enable RTC as wakeup source
[15:0]			RSVD	
0x1C			**WSR**	Wakeup Status register
[31:26]			RSVD	
[25]	r	1'b0	CHG	Indicates the wakeup status from Charger event. Note: the status is masked by WER
[24]			RSVD	
[23]	r	1'b0	LP2HP_IRQ	Indicates the wakeup status from MAILBOX2. Note: the status is masked by WER
[22]	r	1'b0	LP2HP_REQ	Indicates the wakeup status from LPSYS request. Note: the status is masked by WER
[21]	r	1'b0	LP2HP_WDT	Indicates the wakeup status from WDT2 2nd timeout request. Note: the status is masked by WER
[20]			RSVD	
[19]	r	1'b0	LPTIM1	Indicates the wakeup status from LPTIM1. Note: the status is masked by WER
[18]	r	1'b0	GPIO1	Indicates the wakeup status from IO(PA). Note: the status is masked by WER
[17]	r	1'b0	IWDT	Indicates the wakeup status from IWDT. Note: the status is masked by WER
[16]	r	1'b0	RTC	Indicates the wakeup status from RTC. Note: the status is masked by WER
[15:0]			RSVD	
0x20			**WCR**	Wakeup Clear register
[31]	w1c	1'b0	AON	Write 1 to clear the AON wakeup IRQ status
[30:0]			RSVD	
0x24			**ISSR**	Inter System Wakeup Register
[31:6]			RSVD	
[5]	r	1'h1	LP_ACTIVE	Read 1 indicates LPSYS is active
[4]	rw	1'h1	HP_ACTIVE	Write 1 to indicates HPSYS is active
[3:2]			RSVD	
[1]	r	1'b0	LP2HP_REQ	Indicate LPSYS request exists
[0]	rw	1'b0	HP2LP_REQ	Write 1 to request LPSYS to stay in active mode
0x28			**ANACR**	Analog Control Register
[31:2]			RSVD	
[1]	rw	1'b0	AUTO_ISO	for debug only
[0]	rw	1'b0	VHP_ISO	Set 1 to force off all HPSYS related analog modules
0x2C			**GTIMR**	Global Timer Register
[31:0]	r	32'h0	CNT	Global timer value. Write to restart from 0 and sync both HP and LP sides

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表 4-3: HPSYS_AON 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x30			**RESERVE0**	Reserve Register 0
[31:0]	rw	32'b0	DATA	Once bit 31 is set to 1, RESERVE0 is locked and read only (for security boot from standby mode).
0x34			**RESERVE1**	Reserve Register 1
[31:0]	rw	32'b0	DATA	for debug only

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5 输入输出

5.1 简介

SF32LB57x 芯片最多支持 58 个可配置的通用 IO 管脚 PA00~PA57，另有 13 个专用于 MPI1 合封 PSRAM 的 IO(SA00~SA12)，以及 13 个专用于 MPI2 合封 PSRAM 或 NOR Flash 的 IO(SB00~SB12)。每个通用 IO 可独立选择输入输出功能，并独立配置驱动强度和上下拉电阻。当配置为 GPIO 功能时，每个通用 IO 均可根据电平的高低或翻转触发中断，并可将系统从某些低功耗模式中唤醒。其中 PA24~PA27 还支持配置为低功耗 IO，用于在低功耗模式下进行输出。

5.2 IO 结构

单个通用 IO 的结构如下图。

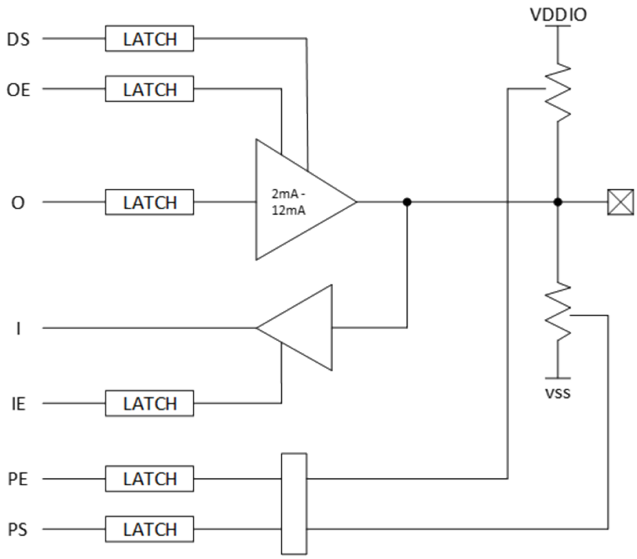


图 5-1: IO 结构

DS 用于配置驱动强度，由 PINMUX 对应 IO 的 DS0 和 DS1 寄存器指定。{DS1,DS0} 的值由 0 到 3，驱动强度逐渐增大。

IO 输出由 O 和 OE 确定，根据 PINMUX 对应 IO 的 FSEL 寄存器选择不同功能，自动映射到相应功能的输出。

IO 输入使能由 PINMUX 对应 IO 的 IE 寄存器控制。当 IE 为高时，输入电平 I 根据 PINMUX 对应 IO 的 FSEL 寄存器自动映射到相应功能的输入；当 IE 为低时，相应功能无法获取到 IO 的输入电平。

PE 和 PS 用于控制 IO 的上下拉电阻，由 PINMUX 对应 IO 的 PE 和 PS 寄存器指定。PE 为 0 时上下拉电阻均不生效。PE 为 1，PS 为 0 时，下拉电阻有效。PE 为 1，PS 为 1 时，上拉电阻有效。上下拉电阻的阻值约为 10k~40k 欧姆，与 IO 外部电路以及接口电平相关。

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5.3 输入输出功能选择

通过配置 PINMUX 对应 IO 的 FSEL 寄存器，可以将 IO 的输入输出映射为若干功能中的一种。PA00~PA57 等通用 IO 的功能既可映射为专用功能 (FSEL 为 0~15)，也可映射为通用矩阵功能 (FSEL>15)。

FSEL 为 0~15 时，IO 信号不经过 IO 矩阵，选择为专用功能，目的是保证延时要求较高信号的时序，并保持与 SF32LB52x 系列芯片的引脚兼容。专用功能主要包括 MPI, LCDC, USB, SDMMC, SPI 等模块的输入输出信号。除 PA43 和 PA44 默认映射为 SWD 功能 (FSEL=1) 外，其它通用 IO 默认都映射为 GPIO 功能 (FSEL=0)。需注意的是，PA18 与 PA19 会在 BOOTMODE1 模式启动时被 BOOTROM 程序分别配置为 USART1_RXD 和 USART1_TXD 功能。

表 5-1: 大核域 GPIO（PA）管脚列表

Pin Number			Pin Name	Type	Sel #	Function
57xUxxx6 (QFN68)	57xYxxx6 (QFN80)	57xVxxx6 (BGA112)				
51	36	C12	PA00	I/O	0	GPIO_A0
					1	LCDC1_SPI_RSTB
					3	SD2_DIO2
					16~255	See Matrix index Table
					Others	Reserved
50	35	C10	PA01	I/O	0	GPIO_A1
					3	SD2_DIO3
					16~255	See Matrix index Table
					Others	Reserved
49	34	D12	PA02	I/O	0	GPIO_A2
					1	LCDC1_SPI_TE
					3	SD2_CLK
					16~255	See Matrix index Table
					Others	Reserved
48	33	D13	PA03	I/O	0	GPIO_A3
					1	LCDC1_SPI_CS
					3	SD2_CMD
					16~255	See Matrix index Table
					Others	Reserved
47	32	D10	PA04	I/O	0	GPIO_A4
					1	LCDC1_SPI_CLK
					3	SD2_DIO0
					16~255	See Matrix index Table
					Others	Reserved
46	31	E12	PA05	I/O	0	GPIO_A5
					1	LCDC1_SPI_DIO0
					3	SD2_DIO1
					16~255	See Matrix index Table
					Others	Reserved
45	30	E13	PA06	I/O	0	GPIO_A6
					1	LCDC1_SPI_DIO1
					2	SD1_DIO2
					16~255	See Matrix index Table
					Others	Reserved
44	29	E11	PA07	I/O	0	GPIO_A7

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表 5-1: 大核域 GPIO（PA）管脚列表（续）

Pin Number			Pin Name	Type	Sel #	Function
57xUxxx6 (QFN68)	57xYxxx6 (QFN80)	57xVxxx6 (BGA112)				
					1	LCDC1_SPI_DIO2
					2	SD1_DIO3
					16~255	See Matrix index Table
					Others	Reserved
43	28	E10	PA08	I/O	0	GPIO_A8
					1	LCDC1_SPI_DIO3
					2	SD1_CLK
					16~255	See Matrix index Table
					Others	Reserved

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表 5-1: 大核域 GPIO（PA）管脚列表（续）

Pin Number			Pin Name	Type	Sel #	Function
57xUxxx6 (QFN68)	57xYxxx6 (QFN80)	57xVxxx6 (BGA112)				
42	26	F12	PA09	I/O	0	GPIO_A9
					2	SD1_CMD
					15	#ADC1N
					16~255	See Matrix index Table
					Others	Reserved
35	19	J12	PA10	I/O	0	GPIO_A10
					2	SD1_DIO0
					15	#ADC2P
					16~255	See Matrix index Table
					Others	Reserved
34	18	H12	PA11	I/O	0	GPIO_A11
					2	SD1_DIO1
					15	#ADC2N
					16~255	See Matrix index Table
					Others	Reserved
33	17	K12	PA12	I/O	0	GPIO_A12
					1	MPI3_CS
					2	SD1_DIO2
					16~255	See Matrix index Table
					Others	Reserved
32	16	H11	PA13	I/O	0	GPIO_A13
					1	MPI3_DIO1
					2	SD1_DIO3
					16~255	See Matrix index Table
					Others	Reserved
31	15	G9	PA14	I/O	0	GPIO_A14
					1	MPI3_DIO2
					2	SD1_CLK
					16~255	See Matrix index Table
					Others	Reserved
30	14	G8	PA15	I/O	0	GPIO_A15
					1	MPI3_DIO0
					2	SD1_CMD
					16~255	See Matrix index Table
					Others	Reserved
29	13	K8	PA16	I/O	0	GPIO_A16
					1	MPI3_CLK
					2	SD1_DIO0
					16~255	See Matrix index Table
					Others	Reserved
28	12	J8	PA17	I/O	0	GPIO_A17
					1	MPI3_DIO3
					2	SD1_DIO1
					16~255	See Matrix index Table
					Others	Reserved

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表 5-1: 大核域 GPIO（PA）管脚列表（续）

Pin Number			Pin Name	Type	Sel #	Function
57xUxxx6 (QFN68)	57xYxxx6 (QFN80)	57xVxxx6 (BGA112)				
27	11	H8	PA18	I/O	0	GPIO_A18
					1	SWDIO
					16~255	See Matrix index Table
					Others	Reserved
26	10	H7	PA19	I/O	0	GPIO_A19
					1	SWCLK
					16~255	See Matrix index Table
					Others	Reserved
25	9	J7	PA20	I/O	0	GPIO_A20
					1	SWO
					16~255	See Matrix index Table
					Others	Reserved
-	8	G7	PA21	I/O	0	GPIO_A21
					16~255	See Matrix index Table
					Others	Reserved
11	74	D1	PA22	I/O	0	GPIO_A22
					2	SD1_DIO2
					3	SD2_DIO2
					15	#XTAL32K_XI
					16~255	See Matrix index Table
					Others	Reserved
10	73	D2	PA23	I/O	0	GPIO_A23
					2	SD1_DIO3
					3	SD2_DIO3
					15	#XTAL32K_XO
					16~255	See Matrix index Table
					Others	Reserved
9	72	G5	PA24	I/O	0	GPIO_A24
					1	SPI1_DIO
					2	SD1_CLK
					3	SD2_CLK
					4	RTC_CLK
					5	LPTIM2_OUT
					6	LPTIM2_OUTB
					16~255	See Matrix index Table
					Others	Reserved
8	71	G4	PA25	I/O	0	GPIO_A25
					1	SPI1_DI
					2	SD1_CMD
					3	SD2_CMD
					4	RTC_CLK
					5	LPTIM2_OUT
					6	LPTIM2_OUTB
					15	#XTAL32K_EXT
					16~255	See Matrix index Table
					Others	Reserved

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表 5-1: 大核域 GPIO（PA）管脚列表（续）

Pin Number			Pin Name	Type	Sel #	Function
57xUxxx6 (QFN68)	57xYxxx6 (QFN80)	57xVxxx6 (BGA112)				
7	70	F4	PA26	I/O	0	GPIO_A26
					2	SD1_DIO0
					3	SD2_DIO0
					4	RTC_CLK
					5	LPTIM2_OUT
					6	LPTIM2_OUTB
					16~255	See Matrix index Table
					Others	Reserved
6	69	E3	PA27	I/O	0	GPIO_A27
					2	SD1_DIO1
					3	SD2_DIO1
					4	RTC_CLK
					5	LPTIM2_OUT
					6	LPTIM2_OUTB
					16~255	See Matrix index Table
					Others	Reserved
5	68	C2	PA28	I/O	0	GPIO_A28
					1	SPI1_CLK
					3	SD2_DIO2
					15	#GPADC_CH0
					16~255	See Matrix index Table
					Others	Reserved
4	67	D3	PA29	I/O	0	GPIO_A29
					1	SPI1_CS
					3	SD2_DIO3
					15	#GPADC_CH1
					16~255	See Matrix index Table
					Others	Reserved
3	66	B2	PA30	I/O	0	GPIO_A30
					3	SD2_CLK
					4	#EFUSE_PWR
					15	#GPADC_CH2
					16~255	See Matrix index Table
					Others	Reserved
2	65	B1	PA31	I/O	0	GPIO_A31
					3	SD2_CMD
					15	#GPADC_CH3
					16~255	See Matrix index Table
					Others	Reserved
1	64	A1	PA32	I/O	0	GPIO_A32
					3	SD2_DIO0
					15	#GPADC_CH4
					16~255	See Matrix index Table
					Others	Reserved

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表 5-1: 大核域 GPIO（PA）管脚列表（续）

Pin Number			Pin Name	Type	Sel #	Function
57xUxxx6 (QFN68)	57xYxxx6 (QFN80)	57xVxxx6 (BGA112)				
67	62	D4	PA33	I/O	0	GPIO_A33
					3	SD2_DIO1
					5	#WKUP_PIN
					15	#GPADC_CH5
					16~255	See Matrix index Table
					Others	Reserved
66	61	A3	PA34	I/O	0	GPIO_A34
					5	#WKUP_PIN
					15	#GPADC_CH6
					16~255	See Matrix index Table
					Others	Reserved
65	60	B3	PA35	I/O	0	GPIO_A35
					4	#USB_DP
					5	#WKUP_PIN
					15	#GPADC_CH7
					16~255	See Matrix index Table
					Others	Reserved
64	59	B4	PA36	I/O	0	GPIO_A36
					4	#USB_DM
					5	#WKUP_PIN
					15	#GPADC_CH8
					16~255	See Matrix index Table
					Others	Reserved
63	58	C4	PA37	I/O	0	GPIO_A37
					1	SPI2_DIO
					2	SD1_DIO2
					5	#WKUP_PIN
					15	#GPADC_CH9
					16~255	See Matrix index Table
					Others	Reserved
62	57	C5	PA38	I/O	0	GPIO_A38
					1	SPI2_DI
					2	SD1_DIO3
					5	#WKUP_PIN
					15	#GPADC_CH10
					16~255	See Matrix index Table
					Others	Reserved
61	56	B5	PA39	I/O	0	GPIO_A39
					1	SPI2_CLK
					2	SD1_CLK
					5	#WKUP_PIN
					16~255	See Matrix index Table
					Others	Reserved

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表 5-1: 大核域 GPIO（PA）管脚列表（续）

Pin Number			Pin Name	Type	Sel #	Function
57xUxxx6 (QFN68)	57xYxxx6 (QFN80)	57xVxxx6 (BGA112)				
60	55	A5	PA40	I/O	0	GPIO_A40
					1	SPI2_CS
					2	SD1_CMD
					5	#WKUP_PIN
					16~255	See Matrix index Table
					Others	Reserved
59	54	D5	PA41	I/O	0	GPIO_A41
					2	SD1_DIO0
					5	#WKUP_PIN
					16~255	See Matrix index Table
					Others	Reserved
58	53	D6	PA42	I/O	0	GPIO_A42
					2	SD1_DIO1
					5	#WKUP_PIN
					16~255	See Matrix index Table
					Others	Reserved
57	52	B6	PA43	I/O	0	GPIO_A43
					1	SWDIO
					16~255	See Matrix index Table
					Others	Reserved
56	51	A6	PA44	I/O	0	GPIO_A44
					1	SWCLK
					16~255	See Matrix index Table
					Others	Reserved
-	50	D7	PA45	I/O	0	GPIO_A45
					3	SD2_DIO2
					16~255	See Matrix index Table
					Others	Reserved
-	49	C7	PA46	I/O	0	GPIO_A46
					3	SD2_DIO3
					16~255	See Matrix index Table
					Others	Reserved
-	48	B7	PA47	I/O	0	GPIO_A47
					3	SD2_CLK
					16~255	See Matrix index Table
					Others	Reserved
-	47	D8	PA48	I/O	0	GPIO_A48
					3	SD2_CMD
					16~255	See Matrix index Table
					Others	Reserved
-	46	C8	PA49	I/O	0	GPIO_A49
					3	SD2_DIO0
					16~255	See Matrix index Table
					Others	Reserved

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表 5-1: 大核域 GPIO（PA）管脚列表（续）

Pin Number			Pin Name	Type	Sel #	Function
57xUxxx6 (QFN68)	57xYxxx6 (QFN80)	57xVxxx6 (BGA112)				
-	45	B8	PA50	I/O	0	GPIO_A50
					3	SD2_DIO1
					16~255	See Matrix index Table
					Others	Reserved
-	40	B13	PA51	I/O	0	GPIO_A51
					16~255	See Matrix index Table
					Others	Reserved
-	39	C11	PA52	I/O	0	GPIO_A52
					16~255	See Matrix index Table
					Others	Reserved
-	38	D9	PA53	I/O	0	GPIO_A53
					16~255	See Matrix index Table
					Others	Reserved
-	37	E9	PA54	I/O	0	GPIO_A54
					16~255	See Matrix index Table
					Others	Reserved
41	25	G12	PA55	I/O	0	GPIO_A55
					15	#ADC1P
					16~255	See Matrix index Table
					Others	Reserved
40	24	F11	PA56	I/O	0	GPIO_A56
					15	#MICBIAS
					16~255	See Matrix index Table
					Others	Reserved
-	27	F10	PA57	I/O	0	GPIO_A57
					16~255	See Matrix index Table
					Others	Reserved
-	-	J9	SB01	I/O	4	MPI3_DIO2
					Others	Reserved
-	-	K9	SB02	I/O	4	MPI3_DIO1
					Others	Reserved
-	-	H10	SB03	I/O	4	MPI3_CS
					Others	Reserved
-	-	J10	SB07	I/O	4	MPI3_DIO0
					Others	Reserved
-	-	J11	SB08	I/O	4	MPI3_DIO3
					Others	Reserved
-	-	K11	SB09	I/O	4	MPI3_CLK
					Others	Reserved

FSEL>15 时，IO 信号会经过 IO 矩阵，延时相对较大，适合频率较低或延时要求不严格的应用。通用矩阵功能包括 I2C, SPI, USART, CAN, PDM, I2S, ATIM, GPTIM, LPTIM, PWM, PTM, PTA 等模块的输入输出信号，其中每个信号都可以映射到任意一个通用 IO 上。用户在使用这些接口信号时可以非常方便灵活的选择 IO。同一个接口输出信号可以映射到多个 IO 同时输出，例如 GPTIM1_CH1 产生的 PWM 输出可以同时映射到 PA05 和 PA07 输出，但若将同一个接口输入信号映射到多个 IO 上则可能引起功能错误。

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表 5-2: Matrix Index Table

func_sel	func	func_sel	func	func_sel	func	func_sel	func
16	I2C1_SCL	56	GPTIM1_CH3	96	I2S1_SDO	136	LCDC_IF15
17	I2C1_SDA	57	GPTIM1_CH4	97	I2S1_SDI	137	LCDC_IF16
18	I2C2_SCL	58	GPTIM1_ETR	98	I2S1_BCK	138	LCDC_IF17
19	I2C2_SDA	59	GPTIM2_CH1	99	I2S1_LRCK	139	LCDC_IF18
20	I2C3_SCL	60	GPTIM2_CH2	100	I2S2_MCLK	140	LCDC_IF19
21	I2C3_SDA	61	GPTIM2_CH3	101	I2S2_SDO	141	LCDC_IF20
22	I2C4_SCL	62	GPTIM2_CH4	102	I2S2_SDI	142	LCDC_IF21
23	I2C4_SDA	63	GPTIM2_ETR	103	I2S2_BCK	143	LCDC_IF22
24	SPI1_CLK	64	LPTIM1_IN	104	I2S2_LRCK	144	LCDC_IF23
25	SPI1_CS	65	LPTIM1_OUT	105	PTM1_CH0	145	LCDC_IF24
26	SPI1_DI	66	LPTIM1_ETR	106	PTM1_CH1	146	LCDC_IF25
27	SPI1_DIO	67	LPTIM2_IN	107	PTM1_CH2	147	LCDC_IF26
28	SPI2_CLK	68	LPTIM2_OUT	108	PTM1_CH3	148	LCDC_IF27
29	SPI2_CS	69	LPTIM2_ETR	109	PTM1_CH4	149	LCDC_IF28
30	SPI2_DI	70	ATIM1_CH1	110	PTM1_CH5	150	LCDC_IF29
31	SPI2_DIO	71	ATIM1_CH2	111	PTM1_CH6	151	PDM1_CLK
32	UART1_TXD	72	ATIM1_CH3	112	PTM1_CH7	152	PDM2_CLK
33	UART1_RXD	73	ATIM1_CH4	113	PTM1_CH8	153	PDM1_DATA
34	UART1_RTS	74	ATIM1_ETR	114	PTM1_CH9	154	PDM1_DATA2
35	UART1_CTS	75	ATIM1_CH1N	115	PTM1_CH10	155	PDM2_DATA
36	UART2_TXD	76	ATIM1_CH2N	116	PTM1_CH11	156	PDM2_DATA2
37	UART2_RXD	77	ATIM1_CH3N	117	PTM1_CH12	157	DCMI_CLK
38	UART2_RTS	78	ATIM1_BK	118	PTM1_CH13	158	DCMI_HSYNC
39	UART2_CTS	79	ATIM1_BK2	119	PTM1_CH14	159	DCMI_VSYNC
40	UART3_TXD	80	ATIM2_CH1	120	PTM1_CH15	160	DCMI_DI0
41	UART3_RXD	81	ATIM2_CH2	121	LCDC_IF0	161	DCMI_DI1
42	UART3_RTS	82	ATIM2_CH3	122	LCDC_IF1	162	DCMI_DI2
43	UART3_CTS	83	ATIM2_CH4	123	LCDC_IF2	163	DCMI_DI3
44	CAN1_TXD	84	ATIM2_ETR	124	LCDC_IF3	164	DCMI_DI4
45	CAN1_RXD	85	ATIM2_CH1N	125	LCDC_IF4	165	DCMI_DI5
46	CAN2_TXD	86	ATIM2_CH2N	126	LCDC_IF5	166	DCMI_DI6
47	CAN2_RXD	87	ATIM2_CH3N	127	LCDC_IF6	167	DCMI_DI7
48	BT_ACTIVE	88	ATIM2_BK	128	LCDC_IF7	168	DCMI_DI8
49	BT_PRIORITY	89	ATIM2_BK2	129	LCDC_IF8	169	DCMI_DI9
50	BT_COLLISION	90	PWM1_CH1	130	LCDC_IF9	170	DCMI_DI10
51	WLAN_ACTIVE	91	PWM1_CH2	131	LCDC_IF10	171	DCMI_DI11
52	BT_TX	92	PWM1_CH3	132	LCDC_IF11	172	DCMI_DI12
53	BT_RX	93	PWM1_CH4	133	LCDC_IF12	173	DCMI_DI13
54	GPTIM1_CH1	94	PWM1_CH5	134	LCDC_IF13	174	DCMI_DI14
55	GPTIM1_CH2	95	I2S1_MCLK	135	LCDC_IF14	175	DCMI_DI15

当 IO 映射为 LCDC 模块的信号 LCDC_IF0~LCDCIF29 时，其具体对应信号取决于当前 LCDC 配置的接口模式。例如，如果 LCDC 配置为 DBI 模式，任意一个通用 IO 映射为 LCDC_IF2 时 (FSEL=123)，即可作为 LCDC_8080_CS 功能使用。

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表 5-3: LCDC mapping table

	SPI	JDI	EPD	DBI	DPI
LCDC_IF0	LCDC_SPI_TE		LCDC_TCON_GDSP	LCDC_8080_TE	LCDC_DPI_CLK
LCDC_IF1	LCDC_SPI_RSTB		LCDC_TCON_GDCLK	LCDC_8080_RSTB	LCDC_DPI_HSYNC
LCDC_IF2	LCDC_SPI_CS		LCDC_TCON_SDCLK	LCDC_8080_CS	LCDC_DPI_VSYNC
LCDC_IF3	LCDC_SPI_CLK		LCDC_TCON_SDSTL	LCDC_8080_WR	LCDC_DPI_DE
LCDC_IF4			LCDC_TCON_SDLE	LCDC_8080_RD	LCDC_DPI_SD
LCDC_IF5			LCDC_TCON_SDOE	LCDC_8080_DC	LCDC_DPI_CM
LCDC_IF6	LCDC_SPI_DIO0		LCDC_TCON_SDAT0	LCDC_8080_DIO0	LCDC_DPI_R0
LCDC_IF7	LCDC_SPI_DIO1		LCDC_TCON_SDAT1	LCDC_8080_DIO1	LCDC_DPI_R1
LCDC_IF8	LCDC_SPI_DIO2		LCDC_TCON_SDAT2	LCDC_8080_DIO2	LCDC_DPI_R2
LCDC_IF9	LCDC_SPI_DIO3		LCDC_TCON_SDAT3	LCDC_8080_DIO3	LCDC_DPI_R3
LCDC_IF10		LCDC_JDI_SCS	LCDC_TCON_SDAT4	LCDC_8080_DIO4	LCDC_DPI_R4
LCDC_IF11		LCDC_JDI_SCLK	LCDC_TCON_SDAT5	LCDC_8080_DIO5	LCDC_DPI_R5
LCDC_IF12		LCDC_JDI_SO	LCDC_TCON_SDAT6	LCDC_8080_DIO6	LCDC_DPI_R6
LCDC_IF13		LCDC_JDI_DISP	LCDC_TCON_SDAT7	LCDC_8080_DIO7	LCDC_DPI_R7
LCDC_IF14		LCDC_JDI_EXTCOMIN	LCDC_TCON_SDAT8	LCDC_8080_DIO8	LCDC_DPI_G0
LCDC_IF15			LCDC_TCON_SDAT9	LCDC_8080_DIO9	LCDC_DPI_G1
LCDC_IF16			LCDC_TCON_SDAT10	LCDC_8080_DIO10	LCDC_DPI_G2
LCDC_IF17			LCDC_TCON_SDAT11	LCDC_8080_DIO11	LCDC_DPI_G3
LCDC_IF18		LCDC_JDI_VCK	LCDC_TCON_SDAT12	LCDC_8080_DIO12	LCDC_DPI_G4
LCDC_IF19		LCDC_JDI_XRST	LCDC_TCON_SDAT13	LCDC_8080_DIO13	LCDC_DPI_G5
LCDC_IF20		LCDC_JDI_HCK	LCDC_TCON_SDAT14	LCDC_8080_DIO14	LCDC_DPI_G6
LCDC_IF21		LCDC_JDI_HST	LCDC_TCON_SDAT15	LCDC_8080_DIO15	LCDC_DPI_G7
LCDC_IF22		LCDC_JDI_ENB		LCDC_8080_RWN	LCDC_DPI_B0
LCDC_IF23		LCDC_JDI_VST		LCDC_8080_CS2	LCDC_DPI_B1
LCDC_IF24		LCDC_JDI_R1			LCDC_DPI_B2
LCDC_IF25		LCDC_JDI_G1			LCDC_DPI_B3
LCDC_IF26		LCDC_JDI_B1			LCDC_DPI_B4
LCDC_IF27		LCDC_JDI_R2			LCDC_DPI_B5
LCDC_IF28		LCDC_JDI_G2			LCDC_DPI_B6
LCDC_IF29		LCDC_JDI_B2			LCDC_DPI_B7

IO 映射为 GPIO 时 (FSEL=0)，IO 的输出值与输出使能可通过 HPSYS_GPIO 模块的寄存器配置。

IO 映射为其它功能时，IO 的输出值与输出使能由对应的功能模块控制。

IO 映射为 GPADC 或 XTAL 等模拟功能，或未定义的功能时，IO 的输出使能关闭。

不论 IO 映射为哪种功能，当需要获取 IO 输入时，都必须将对应 IO 的 IE 寄存器置 1。

不论 IO 映射为哪种功能，IO 的输入值都能够从 HPSYS_GPIO 模块中读取，并可用于产生 GPIO 输入中断。

5.4 IO 上拉与下拉电阻

PE 和 PS 用于控制 IO 的上下拉电阻，由 HPSYS_PINMUX 对应 IO 的 PE 和 PS 寄存器指定。PE 为 0 时上下拉电阻均不生效。PE 为 1，PS 为 0 时，下拉电阻有效。PE 为 1，PS 为 1 时，上拉电阻有效。上下拉电阻的阻值约为 10k~40k 欧姆，与 IO 外部电路以及接口电平相关。

除 PA19, PA22 和 PA23 外，其它通用 IO 都默认存在上拉或下拉电阻。IO 默认的上拉或下拉电阻在芯片上电过

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程中即会生效，因此应格外注意外部电路的默认电平匹配，避免出现上电瞬间的异常行为。

默认存在上拉电阻的通用 IO 如下，这些 IO 应避免连接至 LED 或马达控制等默认需求低电平的设备。

PA03 PA11 PA12 PA18 PA26 PA27 PA39 PA40 PA41 PA42

如果要让 IO 配置为高阻，需将 PE 设置为 0，IO 设置为 GPIO 功能，并且 GPIO 输出使能关闭。

5.5 GPIO 输出

当 IO 配置为 GPIO 功能时，IO 的 O 和 OE 控制信号由 GPIO 寄存器控制，从而产生 IO 的输出。通用 IO(PA00~PA57)由 HPSYS_GPIO 控制。GPIO 寄存器的每个比特对应一个通用 IO，例如 HPSYS_GPIO 中 DOER0 的比特 0 对应 PA00，比特 31 对应 PA31；DOER1 的比特 0 对应 PA32，比特 12 对应 PA44。

DOERx 寄存器直接控制 IO 的 OE 信号，为 1 时 IO 的输出导通，为 0 时 IO 的输出关断。软件可以直接配置 DOERx 寄存器，也可以配置 DOESRx 或 DOECRx 进行位操作以免影响其它 IO。

DORx 寄存器直接控制 IO 的 O 信号，为 1 时 IO 的输出为高电平，为 0 时 IO 的输出为低电平。软件可以直接配置 DORx 寄存器，也可以配置 DOSRx 或 DOCRx 进行位操作以免影响其它 IO。

GPIO 推挽输出的配置方法为：

推挽输出 0，需使 IO 的 OE 为 1 ，O 为 0，即 DOERx 对应比特配置为 1，DORx 对应比特配置为 0。

推挽输出 1，需使 IO 的 OE 为 1 ，O 为 1，即 DOERx 对应比特配置为 1，DORx 对应比特配置为 1。

当需要产生开漏输出时，应当首先根据翻转速率需求，使能 IO 内部上拉电阻 (PE=1,PS=1)，或在芯片外部连接上拉电阻。

GPIO 开漏输出的配置方法为：

开漏输出 0，需使 IO 的 OE 为 1 ，O 为 0，即 DOERx 对应比特配置为 1，DORx 对应比特配置为 0。

开漏输出 1，需使 IO 的 OE 为 0，即 DOERx 的对应比特配置为 0。

5.6 GPIO 输入

无论 IO 映射为哪种功能，IO 输入均能够从 GPIO 寄存器 DIRx 中读取，并可根据配置产生 GPIO 中断。

IO 中断使能应仅在需要时打开。软件可以直接配置 IERx 寄存器，也可以配置 IESRx 或 IECRx 进行位操作以免影响其它 IO。

即使 IO 未配置为 GPIO 功能，IO 中断仍可产生，因此当不需要 IO 产生中断时，应当确保其中断使能关闭。

GPIO 中断产生的条件包括 IO 输入信号为高电平/低电平/上升沿/下降沿/双边沿等，如下表所示。

IPH	IPL	ITR=0	ITR=1
0	0	不触发	不触发
0	1	低电平	下降沿
1	0	高电平	上升沿
1	1	无效配置	双边沿

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ITR 用于选择中断条件类型。软件可以直接配置 ITRx 寄存器，也可以配置 ITSRx 或 ITCRx 进行位操作以免影响其它 IO。

IPH 用于使能高电平或上升沿中断条件。软件可以直接配置 IPHRx 寄存器，也可以配置 IPHSRx 或 IPHCRx 进行位操作以免影响其它 IO。

IPL 用于使能低电平或下降沿中断条件。软件可以直接配置 IPLRx 寄存器，也可以配置 IPLSRx 或 IPLCRx 进行位操作以免影响其它 IO。

产生中断的 IO 可通过 ISRx 查询。向 ISRx 的相应比特写 1 可以清除中断状态。

GPIO 中断可将系统从某些低功耗模式中唤醒。唤醒后，软件应查询 ISRx 判断唤醒源，并清除相关标志。

5.7 合封 IO

合封 IO 专用于 MPI 访问合封 (SiP) 的 NOR Flash 或 pSRAM，包括 13 个专用于 MPI1 合封 PSRAM 的 IO(SA00~SA12) 和 13 个专用于 MPI2 合封 PSRAM 或 NOR Flash 的 IO(SB00~SB12)。合封 IO 与通用 IO 的结构相同，可以在 HPSYS_PINMUX 中单独配置每个 IO 的功能以及上下拉电阻。

合封 NOR Flash 的 IO 由 BOOTROM 程序在启动时配置。

合封 PSRAM 的 IO 由二级 Bootloader 程序配置。

5.8 低功耗 IO

PA24~PA27 除原有的通用 IO 输入输出通路以外，另有一组低功耗 IO 输入输出通路，能够在芯片处于低功耗模式下保持输入与输出能力。低功耗 IO 的输入使能、输出使能、上下拉电阻等功能由硬件自动管理，不需要额外配置 (调试时可以通过 PMUC 的 PBRxR 寄存器配置)。

低功耗 IO 能够持续输出低功耗时钟 clk_rtc 或 LPTIM2 产生的低功耗 PWM，不受系统进出 deepsleep 或 standby 模式的影响 (hibernate 模式下 LPTIM 停止工作，因此无法输出 PWM，但仍可输出 clk_rtc)。使用时只需将对应通用 IO 的 FSEL 配置为 RTC_CLK(FSEL=4), LPTIM2_OUT(FSEL=5) 或 LPTIM2_OUTB(FSEL=6) 即可。应注意从 standby 或 hibernate 模式唤醒以后需要重新配置 FSEL。

5.9 IO 供电

IO 的电平标准取决于其供电电压。

合封 IO 的供电电源同时也是对应合封存储器的供电电源。

不同型号的芯片 IO 供电方式不同。

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表 5-4: 不同型号的芯片 IO 供电方式

芯片型号	封装	IO(PA) 供电	IO(SA) 供电	IO(SB) 供电
SF32LB573/5/7(锂电池供电)	QFN68	内部供电 3.3V	内部供电 VDD18_VOUT 1.8V	内部供电 VDD33_VOUT1 3.3V
SF32LB57E/G/Z(3.3V 供电)	QFN68	外供 VDDIOA	内部供电 VDD18_VOUT 1.8V	外供 VDDIOA
	QFN80	外供 VDDIOA	内部供电 VDD18_VOUT 1.8V	外供 VDDIOSB
	BGA	外供 VDDIOA	外供 VDDIOSA （可接 VDD18_VOUT）	外供 VDDIOSB

5.10 唤醒 PIN

芯片支持最多 14 个唤醒 PIN，包括 PA24~PA27 和 PA33~PA42。唤醒 PIN 能够将芯片从 hibernate 模式、standby 模式或 deepsleep 模式中唤醒，唤醒触发方式包括高电平唤醒、低电平唤醒、上升沿唤醒、下降沿唤醒以及双边沿唤醒。唤醒 PIN 功能不依赖于 IO 的功能选择，即 FSEL 寄存器不影响唤醒 PIN 功能。

hibernate 模式支持最多 14 个唤醒 PIN 同时作为唤醒源。

standby 模式支持最多 14 个唤醒 PIN 同时作为唤醒源。

deepsleep 模式除支持最多 14 个唤醒 PIN 同时作为唤醒源以外，还支持任意 IO 唤醒。例如，HPSYS 进入 deepsleep 模式以后，不仅能够被 14 个唤醒 PIN 中的任意一个唤醒 (唤醒状态位是 PMUC 的 WSR_PAxx)，也能够被任意 IO 唤醒 (唤醒状态位是 HPSYS_AON 的 WSR_GPIO1，具体唤醒的 IO 需要在 GPIO 寄存器内查询)。

这 14 个唤醒 PIN 除原有的 IO 输入通路以外，另有一路输入通路用于唤醒 PIN 功能，其输入使能随该 IO 的唤醒使能 (PMUC->WER.PAxx) 自动开关。应保证已开启唤醒 PIN 功能的 IO 未处于中间态电平，否则会产生漏电。可以通过设置所需 IO 的上下拉电阻，并在进入 standby/hibernate 模式时使 IO 进入 retention 模式来保证 IO 处于确定电平。

PIN 唤醒默认开启硬件防抖机制，防抖时长可通过 PMUC 的 WKUP_CNT.PIN_DLY 寄存器配置，默认约为 30ms。如果需要更快的响应速度，应当减小该寄存器的值。

5.11 低功耗模式下的 IO 状态

HPSYS 在 active 模式与 sleep 模式下，IO 正常工作，输出可正常翻转，可产生 IO 中断。

HPSYS 进入 deepsleep 模式以后，所有 IO 进入睡眠模式，输入使能、输出使能、上下拉电阻等配置保持不变，输出保持前值，停止翻转，无法产生 IO 中断，但可产生 IO 唤醒。例外情况是 PA24~PA27 能够进行低功耗输出并可产生 PIN 唤醒；PA33~PA42 能够产生 PIN 唤醒。

HPSYS 进入 standby 模式以后，所有通用 IO 默认关断 (SNS=0)，也可通过配置 PMUC 的 PRSR1 和 PRSR2 寄存器进入 retention 模式。所有合封 IO 进入 retention 模式。关断模式下输入使能与输出使能关闭，上下拉电阻关闭，IO 表现为高阻，无法产生 IO 中断与唤醒。retention 模式下输入使能、输出使能、上下拉电阻等配置保持不变，输出保持前值，停止翻转，无法产生 IO 中断和 IO 唤醒。例外情况是 PA24~PA27 能够进行低功耗输出并可产生 PIN 唤醒；PA33~PA42 能够产生 PIN 唤醒。

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芯片进入 hibernate 模式以后，所有通用 IO 和合封 IO 默认关断 (SNS=0)，也可通过配置 PMUC 的 PRSR1 和 PRSR2 寄存器进入 retention 模式。关断模式下输入使能与输出使能关闭，上下拉电阻关闭，IO 表现为高阻，无法产生 IO 中断与唤醒。retention 模式下输入使能、输出使能、上下拉电阻等配置保持不变，输出保持前值，停止翻转，无法产生 IO 中断和 IO 唤醒。例外情况是 PA24~PA27 能够进行低功耗输出并可产生 PIN 唤醒，PA33~PA42 能够产生 PIN 唤醒。

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表 5-5: IO 工作状态

IO	功能	active	sleep	deepsleep	standby	hibernate
PA00~PA23 PA28~PA32 PA43~PA57	输入使能	工作	工作	保持	无效/保持	无效/保持
	输出使能	工作	工作	保持	无效/保持	无效/保持
	输出电平	可翻转	可翻转	保持	高阻/保持	高阻/保持
	上下拉电阻	有效	有效	保持	无效/保持	无效/保持
	GPIO 中断	有	有	无	无	无
	IO 唤醒	/	/	有	无	无
	PIN 唤醒	/	/	无	无	无
PA33~PA42	输入使能	工作	工作	保持	无效/保持/唤醒	无效/保持/唤醒
	输出使能	工作	工作	保持	无效/保持	无效/保持
	输出电平	可翻转	可翻转	保持	高阻/保持	高阻/保持
	上下拉电阻	有效	有效	保持	无效/保持	无效/保持
	GPIO 中断	有	有	无	无	无
	IO 唤醒	有	有	有	无	无
	PIN 唤醒	有	有	有	有	有
PA24~PA27	输入使能	工作	工作	保持	无效/保持/唤醒	无效/保持/唤醒
	输出使能	工作	工作	工作 (1)	工作 (1)	工作 (1)
	输出电平	可翻转	可翻转	可翻转 (1)	可翻转 (1)	可翻转 (1)
	上下拉电阻	有效	有效	保持	无效/保持	无效/保持
	GPIO 中断	有	有	无	无	无
	IO 唤醒	有	有	有	无	无
	PIN 唤醒	有	有	有	有	有
SA00~SA12 SB00~SB12	输入使能	工作	工作	保持	保持	无效/保持
	输出使能	工作	工作	保持	保持	无效/保持
	输出电平	可翻转	可翻转	保持	保持	高阻/保持
	上下拉电阻	有效	有效	保持	保持	无效/保持
	GPIO 中断	无	无	无	无	无
	IO 唤醒	无	无	无	无	无
	PIN 唤醒	无	无	无	无	无

* (1) 仅限低功耗 IO 输出通路

5.12 避免 IO 漏电

IO 漏电是芯片低功耗调试中经常遇到的问题。常见的 IO 漏电有以下几类：

1. 短路漏电。输出高电平的 IO，与另一个输出低电平的 IO(可能来自其它器件) 通过芯片外部电路短路，会产生较大电流，严重时可造成芯片损坏。
2. 输出导通漏电。IO 输出高电平时，芯片内部或外部存在下拉电阻，产生导通电流。或 IO 输出低电平时，芯片内部或外部存在上拉电阻，产生导通电流。
3. 上下拉电阻导通漏电。某个 IO 在芯片内部或外部同时存在上拉电阻和下拉电阻，产生导通电流。
4. 输入中间态电平漏电。IO 输入通路导通时，输入端处于中间态电平，使得 IO 内部产生导通电流。这种漏电较为隐蔽，且可表现为浮动变化的漏电电流。

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针对第 2 类漏电，对于配置成模块输出或 GPIO 推挽输出的 IO，可关闭上下拉电阻 (PE 设为 0)。

针对第 3 类漏电，应检查芯片外部电路，确保上拉与下拉电阻不存在冲突。对于支持唤醒 PIN 功能的通用 IO，应通过 RTC 中的 PAWK1R 和 PAWK2R 寄存器配置上下拉电阻，关闭 PINMUX 寄存器中的上下拉电阻配置，避免配置冲突。

针对第 4 类漏电，除能明确输入电平是高电平或低电平的 IO 以外，应采用下述配置方法：

- 不需要输入功能的通用 IO，关闭输入使能 (IE 设为 0)。
- 使能唤醒 PIN 功能的 IO，可配置上拉或下拉电阻，并在进入 standby/hibernate 模式时使 IO 进入 retention 模式。

芯片提供的 IO 数目众多，当无法确定哪些 IO 发生漏电时，可以将所有通用 IO (PA00~PA57) 在 PINMUX 中配置成非输入高阻状态 (IE=0,PE=0,OE=0)，并且将 PMUC 的 WER 全部关闭，这种状态下芯片 IO 不会产生漏电。再分批恢复 IO 的配置，找到发生漏电的 IO 并消除漏电因素。

5.13 避免合封 IO 漏电

合封 IO 的供电电源同时也提供给对应的合封存储器，因此合封存储器的漏电也会体现在合封 IO 的电源上。常见的合封 IO 漏电有以下两种：

1. 芯片进入低功耗模式，但合封存储器未进入低功耗状态。合封的 NOR flash 或 pSRAM 在未访问的待机状态下也会消耗电流 (与存储器型号有关，通常约 10~200uA 量级)，这部分漏电在芯片进入低功耗模式后更加凸显，因此推荐芯片在进入 deepsleep 或 standby 模式之前先让合封存储器进入低功耗状态 (漏电约 1~10uA 量级)，芯片醒来以后再让合封存储器退出低功耗状态。合封的 pSRAM 可通过指令进入 half sleep 模式，合封的 NOR flash 可通过指令进入 deep power down 模式，这些模式可以显著降低存储器的漏电。
2. 合封 IO 不可控造成合封存储器漏电。当芯片进入 hibernate 模式，合封 IO 表现为高阻浮动电平。如果此时合封 IO 的电源仍在供电，有可能使得合封存储器进入高漏电状态 (如 CS 管脚为浮动的低电平或中间电平，可能产生上百 uA 到若干 mA 的漏电)。因此在芯片进入 hibernate 模式之前，应关闭合封 IO 的供电电源，避免合封存储器的漏电。如果合封 IO 电源为芯片内部供电，软件可在进出 hibernate 模式时控制内部供电电源的开关，不需外部的电源开关。芯片预留了 PA21 用于控制合封电源，当芯片上电或从 hibernate 唤醒以后 PA21 自动输出高，进入 hibernate 模式以后变为高阻。如果合封 IO 电源为芯片外部供电，可将 PA21 用于使能外部电源开关，从而控制合封电源的开启与关闭，避免漏电。

5.14 HPSYS_PINMUX 寄存器

HPSYS_PINMUX 的基地址是 0x50003000。

表 5-6: HPSYS_PINMUX 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x0			**PAD_SA00**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength

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表 5-6: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x4			**PAD_SA01**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x8			**PAD_SA02**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0xC			**PAD_SA03**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x10			**PAD_SA04**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down

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表 5-6: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x14			**PAD_SA05**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x18			**PAD_SA06**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x1C			**PAD_SA07**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x20			**PAD_SA08**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x24			**PAD_SA09**	
[31:16]			RSVD	

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表 5-6: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x28			**PAD_SA10**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x2C			**PAD_SA11**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x30			**PAD_SA12**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x34			**PAD_SB00**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate

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表 5-6: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x38			**PAD_SB01**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x3C			**PAD_SB02**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x40			**PAD_SB03**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x44			**PAD_SB04**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device

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表 5-6: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7:0]	rw	8'h0	FSEL	Function Select
0x48			**PAD_SB05**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x4C			**PAD_SB06**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x50			**PAD_SB07**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x54			**PAD_SB08**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x58			**PAD_SB09**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW

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表 5-6: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x5C			**PAD_SB10**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x60			**PAD_SB11**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x64			**PAD_SB12**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x68			**PAD_PA00**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input

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表 5-6: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x6C			**PAD_PA01**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x70			**PAD_PA02**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x74			**PAD_PA03**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x78			**PAD_PA04**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select

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表 5-6: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x7C			**PAD_PA05**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x80			**PAD_PA06**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x84			**PAD_PA07**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x88			**PAD_PA08**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x8C			**PAD_PA09**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength

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表 5-6: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x90			**PAD_PA10**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x94			**PAD_PA11**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x98			**PAD_PA12**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x9C			**PAD_PA13**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer

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表 5-6: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0xA0			**PAD_PA14**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0xA4			**PAD_PA15**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0xA8			**PAD_PA16**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0xAC			**PAD_PA17**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0xB0			**PAD_PA18**	

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表 5-6: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0xB4			**PAD_PA19**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h0	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h0	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0xB8			**PAD_PA20**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0xBC			**PAD_PA21**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0xC0			**PAD_PA22**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength

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表 5-6: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h0	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h0	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0xC4			**PAD_PA23**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h0	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h0	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0xC8			**PAD_PA24**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0xCC			**PAD_PA25**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0xD0			**PAD_PA26**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down

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表 5-6: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0xD4			**PAD_PA27**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0xD8			**PAD_PA28**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0xDC			**PAD_PA29**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0xE0			**PAD_PA30**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0xE4			**PAD_PA31**	
[31:16]			RSVD	

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表 5-6: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0xE8			**PAD_PA32**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0xEC			**PAD_PA33**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0xF0			**PAD_PA34**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0xF4			**PAD_PA35**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate

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表 5-6: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0xF8			**PAD_PA36**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0xFC			**PAD_PA37**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x100			**PAD_PA38**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x104			**PAD_PA39**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device

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表 5-6: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7:0]	rw	8'h0	FSEL	Function Select
0x108			**PAD_PA40**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x10C			**PAD_PA41**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x110			**PAD_PA42**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h1	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x114			**PAD_PA43**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x118			**PAD_PA44**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW

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表 5-6: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x11C			**PAD_PA45**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x120			**PAD_PA46**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x124			**PAD_PA47**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x128			**PAD_PA48**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input

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表 5-6: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x12C			**PAD_PA49**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x130			**PAD_PA50**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x134			**PAD_PA51**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x138			**PAD_PA52**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select

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表 5-6: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x13C			**PAD_PA53**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x140			**PAD_PA54**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x144			**PAD_PA55**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x148			**PAD_PA56**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select
0x14C			**PAD_PA57**	
[31:16]			RSVD	
[15]	rw	1'h0	POE	Reserved. Always set to logic LOW
[14]	rw	1'b1	DS1	Drive Select 1. Used to select output drive strength

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表 5-6: HPSYS_PINMUX 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[13]	rw	1'b0	DS0	Drive Select 0. Used to select output drive strength
[12]	rw	1'h0	SR	Slew Rate. Logic HIGH selects slow slew rate, logic LOW selects fast slew rate
[11]	rw	1'h1	IS	Input Select. Logic LOW selects CMOS input, logic HIGH selects Schmitt input
[10]	rw	1'h1	IE	Input Enable. Logic HIGH enables the input buffer
[9]	rw	1'h0	PS	Pull Select. Logic HIGH selects pull-up, logic LOW select pull-down
[8]	rw	1'h1	PE	Pull Enable. Logic HIGH enables week pull device
[7:0]	rw	8'h0	FSEL	Function Select

5.15 HPSYS_CFG 寄存器

HPSYS_CFG 的基地址是 0x5000B000。

表 5-7: HPSYS_CFG 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**BMR**	Boot Mode Register
[31:1]			RSVD	
[0]	rw	1'h0	BOOT_MODE	write 1 to assert boot reg, will enter boot mode after reboot write 0 to deassert boot reg read 1 if boot reg asserted, or PA00 input high, or boot mode enabled by DBGUART read 0 if boot reg deasserted, and PA00 input low, and boot mode cleared by DBGUART
0x04			**IDR**	ID Register
[31:24]	r	8'hC2	SID	Series ID
[23:16]	r	8'h05	CID	Chip ID
[15:8]	r	8'h0	PID	Package ID
[7:0]	r	8'h0	REVID	Revision ID
0x08			**SWCR**	SW Control Register
[31:1]			RSVD	
[0]	rw	1'h0	SWSEL	0 - SW connected to HCPU; 1 - SW connected to LCPU
0x0C			**SCR**	Security Control Register
[31:1]			RSVD	
[0]	rw	1'h1	FKEY_MODE	AES will use dedicated algorithm for root key encryption and will not output to SRAM
0x10			**SYSCR**	System Configure Register
[31:2]			RSVD	
[1]	rw	1'h0	DIS_INV2CLN	Set 1 to disable clean cache when invalidate cache
[0]	rw	1'h0	LDO_VSEL	select work mode 0: enhanced mode 1: base mode
0x14			**RTC_TR**	RTC Time Register
[31]	r	1'h0	PM	AM/PM notation 0: AM 1: PM
[30:29]	r	2'h0	HT	Hour tens in BCD format
[28:25]	r	4'h0	HU	Hour units in BCD format
[24:22]	r	3'h0	MNT	Minute tens in BCD format

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表 5-7: HPSYS_CFG 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[21:18]	r	4'h0	MNU	Minute units in BCD format
[17:15]	r	3'h0	ST	Second tens in BCD format
[14:11]	r	4'h0	SU	Second units in BCD format
[10]			RSVD	
[9:0]	r	10'h0	SS	Sub-second counter
0x18			**RTC_DR**	RTC Date Register
[31]	r	1'h0	ERR	reserved for debug
[30]	rw0c	1'h0	RSF	re-sync flag. Write 0 to clear, write 1 has no effect. Auto-cleared when entering low power mode
[29:25]			RSVD	
[24]	r	1'h0	CB	Century flag
[23:20]	r	4'h0	YT	Year tens in BCD format
[19:16]	r	4'h0	YU	Year units in BCD format
[15:13]	r	3'h1	WD	Week day units 000: forbidden 001: Monday ... 111: Sunday
[12]	r	1'h0	MT	Month tens in BCD format
[11:8]	r	4'h1	MU	Month units in BCD format
[7:6]			RSVD	
[5:4]	r	2'h0	DT	Date tens in BCD format
[3:0]	r	4'h1	DU	Date units in BCD format
0x1C			**ULPMCR**	ULP Memory Control register
[31:21]			RSVD	
[20]	rw	1'b1	ROM_RME	reserved for debug
[19:18]			RSVD	
[17:16]	rw	2'b11	ROM_RM	reserved for debug
[15:13]			RSVD	
[12:10]	rw	3'b000	RAM_WPULSE	reserved for debug
[9:7]	rw	3'b100	RAM_WA	reserved for debug
[6:5]	rw	2'b00	RAM_RA	reserved for debug
[4]	rw	1'b1	RAM_RME	reserved for debug
[3:2]			RSVD	
[1:0]	rw	2'b11	RAM_RM	reserved for debug
0x20			**DBGR**	Debug Select Register
[31]	rw	1'h0	SWAP	Swap upper/lower byte of debug data
[30]	r	1'h0	LP2HP_NMIF	LP2HP NMI interrupt flag
[29]	rw	1'h0	LP2HP_NMIE	LP2HP NMI interrupt enable
[28]	rw	1'h0	HP2LP_NMI	set 1 to send NMI interrupt to LCPU
[27]	rw	1'b0	CLK_EN	reserved for debug
[26:24]	rw	3'b0	CLK_SEL	reserved for debug
[23:16]	rw	8'h0	BITEN_H	bit enable for debug data higher byte, active high
[15:8]	rw	8'h0	BITEN_L	bit enable for debug data lower byte, active high
[7:4]	rw	4'h0	SEL_H	select higher byte of debug data
[3:0]	rw	4'h0	SEL_L	select lower byte of debug data
0x24			**MDBGR**	Memory Debug Register
[31:6]			RSVD	

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表 5-7: HPSYS_CFG 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[5]	rw	1'b0	DIS_ROM	reserved for debug
[4]	rw	1'b0	PD_ROM	reserved for debug
[3]	rw	1'b0	LS_ROM	reserved for debug
[2]	rw	1'b0	LS_RAM2	reserved for debug
[1]	rw	1'b0	LS_RAM1	reserved for debug
[0]	rw	1'b0	LS_RAM0	reserved for debug
0x38			**LPIRQ**	Interrupt Selection for LCPU
[31:16]			RSVD	
[15]	rw1c	1'h0	IF1	hp2lp1 interrupt status. Write 1 to clear.
[14]			RSVD	
[13:8]	rw	6'h0	SEL1	select hp2lp1 interrupt source
[7]	rw1c	1'h0	IF0	hp2lp0 interrupt status. Write 1 to clear.
[6]			RSVD	
[5:0]	rw	6'h0	SEL0	select hp2lp0 interrupt source
0x3C			**USBCR**	USB Control register
[31:24]			RSVD1	
[23:16]			RSVD0	
[15:13]	rw	3'h0	DC_TR	reserved for debug
[12]	rw	1'h0	DC_TE	reserved for debug
[11]			RSVD	
[10:8]	rw	3'h0	TX_RTUNE	TX outp impedance tuning 0 = 50 Ohm, 1 = 46 Ohm, 2 = 43 Ohm, 3 = 40 Ohm, 4 = 37.5 Ohm, 5 = 35 Ohm, 6 = 33 Ohm, 7 = 31.5 Ohm
[7]			RSVD	
[6]	rw	1'h0	DP_EN	0:disable dp pull up or pull down 1:enable dp pull or pull down
[5]	rw	1'h0	DM_PD	enable DM 15k Ohm pull down resistor
[4]	rw	1'h0	LDO_LP_EN	2.5V LDO low power mode enable. 0 = 240 uA, 1 = 50 uA
[3:1]	rw	3'h0	LDO_VSEL	2.5V LDO output voltage setting 0 = 2.40 V, 1 = 2.47 V, 2 = 2.53 V, 3 = 2.60 V, 4 = 2.60 V, 5 = 2.67 V, 6 = 2.73 V, 7 = 2.8 V
[0]	rw	1'h0	USB_EN	USB PHY enable, turn on power swith, power up LDO and bias
0x40			**SYS_RSVD**	HPSYS RSVD Register
[31:24]	r	8'h0	RESERVE3	reserved for debug
[23:16]	rw	8'hff	RESERVE2	reserved for debug
[15:8]	rw	8'h0	RESERVE1	reserved for debug
[7:0]	rw	8'h0	RESERVE0	reserved for debug
0x44			**ANAU_CR**	ANAU Control Register
[31:7]			RSVD	
[6:4]	rw	3'h0	DC_MR	reserved for debug
[3]	rw	1'b1	EFUSE_VDD_PD	reserved for debug
[2]	rw	1'b0	EFUSE_VDD_EN	reserved for debug
[1]	rw	1'b0	EN_VBAT_MON	reserved for debug
[0]	rw	1'b0	EN_BG	reserved for debug
0x48			**ANAU_RSVD**	ANAU Reserve Register
[31:24]	r	8'h0	RESERVE3	reserved for debug
[23:16]	rw	8'h0	RESERVE2	reserved for debug
[15:8]	rw	8'h0	RESERVE1	reserved for debug
[7:0]	rw	8'h0	RESERVE0	reserved for debug

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表 5-7: HPSYS_CFG 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x4C			**ANATR**	Analog Test Register
[31:8]			RSVD	
[7:5]	rw	3'h0	DC_UR_ATEST1	reserved for debug
[4]	rw	1'h0	DC_TE_ATEST1	reserved for debug
[3:1]	rw	3'h0	DC_UR_ATEST0	reserved for debug
[0]	rw	1'h0	DC_TE_ATEST0	reserved for debug
0x50			**CAU2_CR**	CAU2 Control Register
[31:13]			RSVD	
[12:10]	rw	3'h0	DC_MR	reserved for debug
[9:7]	rw	3'h0	DC_BR	reserved for debug
[6:4]	rw	3'h0	DC_TR	reserved for debug
[3:0]			RSVD	
0x54			**CAU2_RSVD**	CAU2 RSVD Register1
[31:24]			RSVD	
[23:16]	rw	8'h0	RESERVE2	reserved for debug
[15:8]	r	8'h0	RESERVE1	reserved for debug
[7:0]	r	8'h0	RESERVE0	reserved for debug

5.16 HPSYS_GPIO 寄存器

HPSYS_GPIO 的基地址是 0x500A0000。

表 5-8: HPSYS_GPIO 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**DIR0**	Data Input Register
[31:0]	r	32'h0	IN	GPIO[31:0] input value
0x04			**DOR0**	Data Output Register
[31:0]	rw	32'h0	OUT	GPIO[31:0] output value if output enabled
0x08			**DOSR0**	Data Output Set Register
[31:0]	w	32'h0	DOS	set 1 to pull up output of corresponding GPIO[31:0]
0x0C			**DOCR0**	Data Output Clear Register
[31:0]	w	32'h0	DOC	set 1 to pull down output of corresponding GPIO[31:0]
0x10			**DOER0**	Data Output Enable Register
[31:0]	rw	32'h0	DOE	GPIO[31:0] output enable
0x14			**DOESR0**	Data Output Enable Set Register
[31:0]	w	32'h0	DOES	set 1 to enable output of corresponding GPIO[31:0]
0x18			**DOECR0**	Data Output Enable Clear Register
[31:0]	w	32'h0	DOEC	set 1 to disable output of corresponding GPIO[31:0]
0x1C			**IER0**	Interrupt Enable Register
[31:0]	rw	32'h0	IER	GPIO[31:0] interrupt enable
0x20			**IESR0**	Interrupt Enable Set Register
[31:0]	w	32'h0	IES	set 1 to enable interrupt of corresponding GPIO[31:0]
0x24			**IECR0**	Interrupt Enable Clear Register
[31:0]	w	32'h0	IEC	set 1 to disable interrupt of corresponding GPIO[31:0]
0x28			**ITR0**	Interrupt Type Register
[31:0]	rw	32'h0	ITR	GPIO[31:0] interrupt type
0x2C			**ITSR0**	Interrupt Type Set Register

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表 5-8: HPSYS_GPIO 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	w	32'h0	ITS	set 1 for edge-sensitive interrupt mode of corresponding GPIO[31:0]
0x30			**ITCR0**	Interrupt Type Clear Register
[31:0]	w	32'h0	ITC	set 1 for level-sensitive interrupt mode of corresponding GPIO[31:0]
0x34			**IPHR0**	Interrupt Polarity High Register
[31:0]	rw	32'h0	IPH	rising edge in edge mode, or high level in level mode of corresponding GPIO[31:0]
0x38			**IPHSR0**	Interrupt Polarity High Set Register
[31:0]	w	32'h0	IPHS	set 1 for rising edge in edge mode, or high level in level mode of corresponding GPIO[31:0]
0x3C			**IPHCR0**	Interrupt Polarity High Clear Register
[31:0]	w	32'h0	IPHC	set 1 for disable rising edge in edge mode, or high level in level mode of corresponding GPIO[31:0]
0x40			**IPLR0**	Interrupt Polarity Low Register
[31:0]	rw	32'h0	IPL	falling edge in edge mode, or low level in level mode of corresponding GPIO[31:0]
0x44			**IPLSR0**	Interrupt Polarity Low Set Register
[31:0]	w	32'h0	IPLS	set 1 for falling edge in edge mode, or low level in level mode of corresponding GPIO[31:0]
0x48			**IPLCR0**	Interrupt Polarity Low Clear Register
[31:0]	w	32'h0	IPLC	set 1 for disable falling edge in edge mode, or low level in level mode of corresponding GPIO[31:0]
0x4C			**ISR0**	Interrupt Status Register
[31:0]	rw	32'h0	IS	Interrupt status. Write 1 will clear interrupt status of corresponding GPIO[31:0]
0x60			**OEMR0**	output mode Register
[31:0]	rw	32'h0	OEM	output mode of corresponding GPIO[31:0]
0x64			**OEMSR0**	output mode Set Register
[31:0]	w	32'h0	OEMS	output mode Set of corresponding GPIO[31:0]
0x68			**OEMCR0**	output mode Clear Register
[31:0]	w	32'h0	OEMC	output mode Clear of corresponding GPIO[31:0]
0x80			**DIR1**	Data Input Register
[31:0]	r	32'h0	IN	GPIO[63:32] input value
0x84			**DOR1**	Data Output Register
[31:0]	rw	32'h0	OUT	GPIO[63:32] output value if output enabled
0x88			**DOSR1**	Data Output Set Register
[31:0]	w	32'h0	DOS	set 1 to pull up output of corresponding GPIO[63:32]
0x8C			**DOCR1**	Data Output Clear Register
[31:0]	w	32'h0	DOC	set 1 to pull down output of corresponding GPIO[63:32]
0x90			**DOER1**	Data Output Enable Register
[31:0]	rw	32'h0	DOE	GPIO[63:32] output enable
0x94			**DOESR1**	Data Output Enable Set Register
[31:0]	w	32'h0	DOES	set 1 to enable output of corresponding GPIO[63:32]
0x98			**DOECR1**	Data Output Enable Clear Register
[31:0]	w	32'h0	DOEC	set 1 to disable output of corresponding GPIO[63:32]
0x9C			**IER1**	Interrupt Enable Register
[31:0]	rw	32'h0	IER	GPIO[63:32] interrupt enable
0xA0			**IESR1**	Interrupt Enable Set Register
[31:0]	w	32'h0	IES	set 1 to enable interrupt of corresponding GPIO[63:32]
0xA4			**IECR1**	Interrupt Enable Clear Register
[31:0]	w	32'h0	IEC	set 1 to disable interrupt of corresponding GPIO[63:32]
0xA8			**ITR1**	Interrupt Type Register

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表 5-8: HPSYS_GPIO 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	ITR	GPIO[63:32] interrupt type
0xAC			**ITSR1**	Interrupt Type Set Register
[31:0]	w	32'h0	ITS	set 1 for edge-sensitive interrupt mode of corresponding GPIO[63:32]
0xB0			**ITCR1**	Interrupt Type Clear Register
[31:0]	w	32'h0	ITC	set 1 for level-sensitive interrupt mode of corresponding GPIO[63:32]
0xB4			**IPHR1**	Interrupt Polarity High Register
[31:0]	rw	32'h0	IPH	rising edge in edge mode, or high level in level mode of corresponding GPIO[63:32]
0xB8			**IPHSR1**	Interrupt Polarity High Set Register
[31:0]	w	32'h0	IPHS	set 1 for rising edge in edge mode, or high level in level mode of corresponding GPIO[63:32]
0xBC			**IPHCR1**	Interrupt Polarity High Clear Register
[31:0]	w	32'h0	IPHC	set 1 for disable rising edge in edge mode, or high level in level mode of corresponding GPIO[63:32]
0xC0			**IPLR1**	Interrupt Polarity Low Register
[31:0]	rw	32'h0	IPL	falling edge in edge mode, or low level in level mode of corresponding GPIO[63:32]
0xC4			**IPLSR1**	Interrupt Polarity Low Set Register
[31:0]	w	32'h0	IPLS	set 1 for falling edge in edge mode, or low level in level mode of corresponding GPIO[63:32]
0xC8			**IPLCR1**	Interrupt Polarity Low Clear Register
[31:0]	w	32'h0	IPLC	set 1 for disable falling edge in edge mode, or low level in level mode of corresponding GPIO[63:32]
0xCC			**ISR1**	Interrupt Status Register
[31:0]	rw	32'h0	IS	Interrupt status. Write 1 will clear interrupt status of corresponding GPIO[63:32]
0xE0			**OEMR1**	output mode Register
[31:0]	rw	32'h0	OEM	output mode of corresponding GPIO[63:32]
0xE4			**OEMSR1**	output mode Set Register
[31:0]	w	32'h0	OEMS	output mode Set of corresponding GPIO[63:32]
0xE8			**OEMCR1**	output mode Clear Register
[31:0]	w	32'h0	OEMC	output mode Clear of corresponding GPIO[63:32]

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6 DMA

6.1 GPDMA(DMAC1)

6.1.1 简介

GPDMA(General Purpose Direct Memory Access Controller) 用于实现总线上两个不同地址区间内数据的搬运工作。GPDMA 共有 8 个独立通道，每个通道可配置源地址区间与目标地址区间，分别映射到各存储器或外设的地址范围内，从而实现存储器-存储器，存储器-外设，外设-存储器，外设-外设之间的高效率传输，有效缓解 CPU 的工作量。GPDMA 的传输支持外设响应模式和存储器搬运模式：在外设响应模式下，GPDMA 基于外设的 DMA 请求进行搬运，从而适配外设的带宽；在存储器搬运模式下，GPDMA 不等待外设的 DMA 请求，尽快完成数据搬运。当多个通道同时使能时，GPDMA 依照优先级由高至低的次序依次搬运；并且在较低优先级的通道搬运过程中，较高优先级的通道能够进行抢占搬运。每个通道传输过半或完成时，能够产生中断或 PTM 触发。每个通道可设置独立触发源，仅当触发条件满足时才启动传输。每个通道内置 FIFO 用于缓存传输数据，支持数据位宽转换与字节交换。

GPDMA 的工作模式支持基础模式，循环模式，重复模式，链表模式。基础模式可完成单次搬运工作。循环模式可无限循环进行搬运。重复模式可进行特定次数的搬运，并支持每次搬运后起始地址自增。链表模式下能够自动执行多个串联任务，其中每个任务能够独立设置地址、模式、数据量、延时、触发条件等参数。

6.1.2 主要特性

- 单 AHB 主控总线，可访问 SRAM，PSRAM，FLASH，AHB 和 APB 外设等，支持 BURST 传输
- 8 个独立的可配置通道
- 支持外设到存储器、存储器到外设、存储器到存储器以及外设到外设的数据传输
- 每个通道的 DMA 请求可在至多 128 个外设 DMA 请求中选择 1 个，或由软件请求
- 每个通道支持 4 档优先级配置，优先级相同时依照通道编号大小判决
- 源地址和目标地址均独立支持单字节、双字节、四字节访问。源和目标的地址必须根据传输数据单元的大小进行对齐，并支持地址自动递增
- 单次传输单元数可配置为 1 到 1048575
- 支持循环缓冲模式，单次传输完成后自动重新启动
- 每个通道支持 4 种事件标志：传输完成、过半传输、传输错误、链表/重复完成，并能独立生成中断请求及 PTM 触发
- 每个通道独立选择触发源，仅当触发事件发生后才启动传输
- 通道 1~2 支持重复模式，可进行特定次数的搬运，并支持每次搬运后起始地址自增
- 所有通道支持链表模式，可自动执行多个串联任务，每个任务独立设置地址、模式、数据量、延时、触发条件
- 通道 1~2 内置 64-byte FIFO，通道 3~8 内置 8-byte FIFO，用于暂存待传输数据
- 支持数据位宽转换，包括截取/补零/符号扩展/打包/拆包等转换方式
- 支持数据字节交换

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6.1.3 外设请求

每个通道通过配置 CSELR1/2_CxS 或 SELRx_CS 可在 128 个外设请求源中选择任意一个作为该通道的绑定请求源，该外设的应答信号也相应绑定到该通道上。SELRx_CS 是 CSELR1/2_CxS 的镜像寄存器，效果等价。GPDMA 的外设请求表如下。

表 6-1: CSELR1/2_CxS 外设请求表

CxS	外设	CxS	外设	CxS	外设	CxS	外设
0	mpi1	1	mpi2	2	mpi3	3	i2c4
4	usart1_tx	5	usart1_rx	6	usart2_tx	7	usart2_rx
8	gptim1_update	9	gptim1_trigger	10	gptim1_cc1	11	gptim1_cc2
12	gptim1_cc3	13	gptim1_cc4	14	btim1	15	btim2
16	atim1_update	17	atim1_trigger	18	atim1_cc1	19	atim1_cc2
20	atim1_cc3	21	atim1_cc4	22	i2c1	23	i2c2
24	i2c3	25	atim1_com	26	usart3_tx	27	usart3_rx
28	spi1_tx	29	spi1_rx	30	spi2_tx	31	spi2_rx
32	i2s1_tx	33	i2s1_rx	34	i2s2_tx	35	i2s2_rx
36	pdm1_l	37	pdm1_r	38	gpadc	39	adc0 (audio)
40	adc1 (audio)	41	dac0 (audio)	42	dac1 (audio)	43	gptim2_update
44	gptim2_trigger	45	gptim2_cc1	46	audprc_tx_out_ch1	47	audprc_tx_out_ch0
48	audprc_tx_ch3	49	audprc_tx_ch2	50	audprc_tx_ch1	51	audprc_tx_ch0
52	audprc_rx_ch1	53	audprc_rx_ch0	54	gptim2_cc2	55	gptim2_cc3
56	gptim2_cc4	57	sdmmc1	58	dcmi	59	sdmmc2
60	pwm1_cc1	61	pwm1_cc2	62	pwm1_cc3	63	pwm1_cc4
64	ptm1_ofifo0	65	ptm1_ofifo1	66	ptm1_ofifo2	67	ptm1_ofifo3
68	/	69	/	70	/	71	/
72	ptm1_ififo0	73	ptm1_ififo1	74	ptm1_ififo2	75	ptm1_ififo3
76	/	77	/	78	/	79	/
80	pdm2_l	81	pdm2_r	82	atim2_update	83	atim2_trigger
84	atim2_cc1	85	atim2_cc2	86	atim2_cc3	87	atim2_cc4
88	atim2_com						

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6.1.4 GPDMA 结构图

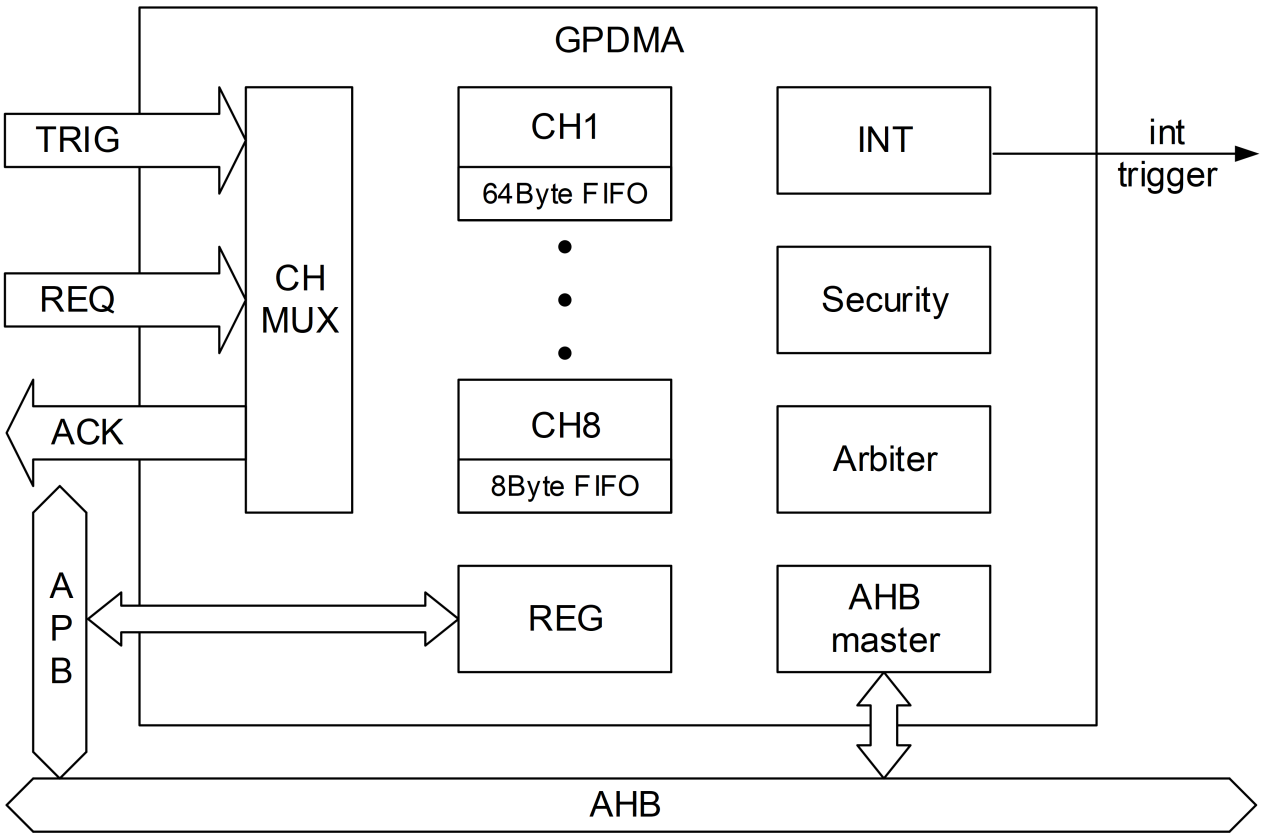


图 6-1: GPDMA 结构图

6.1.5 通道功能

表 6-2: 通道功能

通道编号	重复模式	FIFO 深度	推荐使用方式
1～2	支持	64-byte	存储器间搬运，如 SRAM, PSRAM, FLASH 等
3～8	不支持	8-byte	内存与外设间搬运

所有通道均支持外设到存储器、存储器到外设、存储器到存储器以及外设到外设的数据传输。通道 1～2 在进行存储器搬运时效率会更高，因此当传输涉及到外部存储器 (如 PSRAM 和 FLASH) 时，应当优先选用这些通道。

6.1.6 传输效率

GPDMA 和 CPU 及其它主控设备共享 AHB 总线。当 CPU 和 GPDMA 同时访问相同的目标（存储器或外设）时，GPDMA 请求可能会暂停 CPU 访问系统总线，由总线仲裁器执行循环调度，以保证 CPU 至少可以得到一半的总线带宽。同理，当其它主控设备与 GPDMA 访问相同 AHB 目标时，GPDMA 访问带宽也会下降。

6.1.7 工作模式

每个通道可独立设置为下列工作模式中的一种：基础模式，循环模式，重复模式，链表模式。

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默认的基础模式可完成单次搬运工作，通道从源地址向目标地址搬运一定数量的数据后自动关闭。

CCRx_CIRC 设为 1 可开启循环模式。循环模式是基础模式的自动循环，通道每次搬运完成之后，自动恢复到初始状态重新启动一次搬运。循环模式下，传输不会自动停止，数据传输完成后，CNDTRx 寄存器将自动重新加载初始编程值，内部地址寄存器重新加载 CPARx 和 CM0ARx 寄存器中的基址值。循环模式下通过判断过半传输与传输完成标志，能够实现乒乓缓存的功能。

CREPRx 设为大于 1 的值可开启重复模式，只有通道 1~2 支持。重复模式是基础模式的有限次重复，每次重复时源地址和目的地址可以自动增加，其中 CPARx 增加 CINCRx_PINC，CM0ARx 增加 CINCRx_MINC。通道每次搬运完成之后，重复计数 CREPRx 自动减 1，减到 0 以后通道关闭。

链表模式可将若干任务串联起来自动完成，其中每个任务都相当于基础模式的一次搬运，能够独立设置地址、传输模式、数据量、延时、触发条件等参数。链表模式需要在存储器中预先保存任务链表。链表启动后，通道顺序完成链表中的所有任务，之后自动关闭。链表模式中不支持开启循环及重复。

6.1.8 通道使能

GPDMA 的 8 个通道独立使能。当 CCRx_EN 为 1 且 CNDTRx 不为 0 时，通道传输启动。需要注意当通道使能时，即使上一笔传输已经完成，重新写入非 0 的 CNDTRx 也会立刻启动传输，在此之前应当确保其它参数已经配置完毕，或者在写入 CNDTRx 时保证 CCRx_EN 为 0。

6.1.9 通道触发

通道使能后处于等待状态，仅当触发条件满足时，才启动传输。每个通道可独立选择触发源 (SELRx_TS) 和触发模式 (CCRx_TEDGE 和 CCRx_TPOL)。SELRx_TS 默认为 0，表示无条件触发。除链表模式外，通道仅需单次触发即可完成传输。链表模式下配置的触发条件仅用于触发通道的第一个任务，其后每个任务的触发条件在前一个任务的配置表中设置。

每个通道通过配置 SELRx_TS 可在 128 个触发源中选择任意一个作为该通道的触发信号。

部分触发源需使能 PTM1 的时钟才会生效。

6.1.10 传输模式

每个通道可配置为外设传输模式或存储器传输模式，由 CCRx_MEM2MEM 寄存器控制，主要区别在于是否启用外设请求/应答机制。外设传输模式通过请求/应答机制适配外设的数据带宽，仅在外设准备好了以后才发起传输，通常用于 UART 收发、I2S 音频输入输出、FLASH 烧写等场景。存储器传输模式不需等待请求信号，将以最大可能的数据带宽进行传输，通常用于存储器搬运、CRC 校验等场景。

外设传输模式包括外设读模式 (CCRx_DIR=0) 和外设写模式 (CCRx_DIR=1)。外设读模式下，GPDMA 仅在外设发出请求后才进行数据读取；读出的数据存入 FIFO，积累到一定数量后进行数据写入，写入不依赖于外设请求。外设写模式下，GPDMA 的数据读取不依赖于外设请求，会预先读出数据存入 FIFO，等待外设发出请求后才进行数据写入。

单次外设请求传输的数据量由对应的 CCRx_SBURST 或 CCRx_DBURST 指定。例如当 SPI 需要发送数据，向 GPDMA 发出请求，且 CCRx_DBURST 配置为 2 时，GPDMA 在回复应答之前会连续向 SPI 写入 8 笔数据。

外设传输模式的请求/应答机制流程如下：

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1. 外设在需要传输数据时（如接收缓存满，或发送缓存空），向 GPDMA 相关通道发送请求信号。
2. GPDMA 相关通道启动一次外设传输。
3. 该次外设传输完成后，GPDMA 向外设发送应答信号。
4. 外设获得 GPDMA 的应答信号后，便会释放请求。
5. 检测到外设请求释放后，GPDMA 就会释放应答信号。
6. 外设检测到应答信号释放后，如还有传输需求，可继续发送请求，再次启动 GPDMA 传输。

6.1.11 传输流程

通道触发后，根据需要向 GPDMA 内部的仲裁器发出读请求和写请求。仲裁器基于各通道的优先级，将请求传递至 GPDMA 内部的总线主控，由总线主控读取或写入数据。

满足如下条件时，通道向仲裁器发出读请求：

- 通道 FIFO 剩余空间大于等于本次读取的数据量；
- 通道为外设读模式且收到外设请求，或通道为非外设读模式。

一次读请求读取的数据量是读传输位宽 (由 CCRx_MSIZE 或 CCRx_PSIZE 决定) 与读传输突发长度 (由 CCRx_SBURST 决定) 的乘积，和剩余待读取数据量 (CNDTRx) 之间的较小值。上述乘积不能大于通道 FIFO 最大空间 (通道 1~2 为 64byte，通道 3~8 为 8byte)。

满足如下条件时，通道向仲裁器发出写请求：

- FIFO 有效数据量大于等于本次待写入的数据量；
- 通道为外设写模式且收到外设请求，或通道为非外设写模式。

一次写请求待写入的数据量是写传输位宽 (由 CCRx_PSIZE 或 CCRx_MSIZE 决定) 与写传输突发长度 (由 CCRx_DBURST 决定) 的乘积，和剩余待写入数据量 (CSRx_DSTDNT) 之间的较小值。上述乘积不能大于通道 FIFO 最大空间 (通道 1~2 为 64byte，通道 3~8 为 8byte)。

仲裁器收到各通道的请求后，基于下列原则选择当前胜出的请求，传递至总线主控：

1. 优先级 (CCRx_PL) 最高的通道请求
2. 同等优先级编号最小的通道请求
3. 同一个通道，写请求优先于读请求

总线主控收到仲裁器传来的请求，在 AHB 总线空闲时发出对应的 AHB 读写传输，将读取到的数据存入对应通道的 FIFO，或从对应通道的 FIFO 中取出数据写入。总线主控在完成一笔 AHB 传输前，不会处理新的请求，确保一次请求的数据传输完成后才会有新的请求被处理。

6.1.12 传输方向

GPDMA 的传输方向由 CCRx_DIR 决定。

表 6-3: 传输方向

	源 (读) 起始地址	目标 (写) 起始地址	源 (读) 传输位宽	目标 (写) 传输位宽
DIR=0	CPARx	CM0ARx	CCRx_PSIZE	CCRx_MSIZE
DIR=1	CM0ARx	CPARx	CCRx_MSIZE	CCRx_PSIZE

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6.1.13 传输数量

GPDMA 每个通道传输的数量由 CNDTRx 控制，以读传输位宽计数，支持范围 0～1048575。例如读传输位宽配置为四字节，则通道单次传输最大数据量为 $1048575 \times 4 = 4194300$ 字节。配置 CNDTRx 并启动单元传输 (CCRx_EN=1) 后，每完成一笔总线读取，CNDTRx 寄存器值减 1。

写传输数量由通道根据数据转换方式自动计算得到，传输开始后可从 CSRx_DSTNDT 获取。例如读传输位宽配置为四字节，写传输位宽配置为单字节，数据转换方式为拆包，CNDTRx 为 4194300，则 CSRx_DSTNDT 初始值为 16777200。每完成一笔总线写入，CSRx_DSTNDT 寄存器值减 1。

基础模式下，CNDTRx 和 CSRx_DSTNDT 都减到 0 时传输结束。循环和重复模式下，CNDTRx 和 CSRx_DSTNDT 都减到 0 后会立即重新加载初始值，并继续传输。

打包处理时的传输数量应当保证打包后的数据没有剩余。例如 byte 打包成 word 时，待传输的数据量应当为 4 的整数倍。

剩余的读传输数量可以通过读取 CNDTRx 实时获取。剩余的写传输数量可以通过读取 CSRx_DSTNDT 实时获取。基础模式下传输完成后，CNDTRx 和 CSRx_DSTNDT 的值都应为 0。需要注意 CNDTRx 和 CSRx_DSTNDT 的读取寄存器均为 20bit，无法通过读取 CSRx_DSTNDT 获取超出 20bit 的写传输数量 (此种情况发生在数据转换方式为拆包，且 CNDTRx 配置为较大值时)。

6.1.14 传输地址

传输的起始源地址和目标地址由 CPARx，CM0ARx 以及 CCRx_DIR 决定。如果使能了递增模式（CCRx_MINC 和 CCRx_PINC 独立配置），每完成一笔总线传输，则下次传输的地址是前一次传输的地址加上 1、2 或 4（与传输的位宽一致）。

在传输过程中，这些寄存器将保持初始编程的值。软件无法获得当前正在传输的地址。通常外设 FIFO 的传输地址配置为不递增，而存储器的传输地址配置为递增。

6.1.15 数据处理

GPDMA 传输时，对总线源地址和目标地址的访问可独立通过 CCRx_MSIZE 和 CCRx_PSIZE 配置为单字节/双字节/四字节类型。当源传输位宽和目标传输位宽不一致时，通道提供数据截取/补零/符号扩展/打包/拆包等处理。与此同时，通道还能够对多字节数据进行字节顺序调换。不同配置方式的源数据与目标数据格式如下表。其中表项内数据传输的时间顺序为从下到上，从右至左。

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表 6-4: BYTE 数据处理

SSIZE [1:0]	Source data	Source data stream	SBX	SBS	DSIZE [1:0]	Destination data	PACK	SIGN	DBX	DHX	Destination data stream
00	byte	$B_7,B_6,B_5,B_4,$ B_3,B_2,B_1,B_0	x	x	00	byte	x	x	x	x	$B_7,B_6,B_5,B_4,B_3,B_2,B_1,B_0$
					01	half-word	0	0	0		$0B_7,0B_6,0B_5,0B_4,$ $0B_3,0B_2,0B_1,0B_0$
									1		$B_70,B_60,B_50,B_40,$ B_30,B_20,B_10,B_00
							0	1	0		$SB_7,SB_6,SB_5,SB_4,$ SB_3,SB_2,SB_1,SB_0
									1		$B_7S,B_6S,B_5S,B_4S,$ B_3S,B_2S,B_1S,B_0S
							1	x	0		$B_7B_6,B_5B_4,B_3B_2,B_1B_0$
									1		$B_6B_7,B_4B_5,B_2B_3,B_0B_1$
					10	word	0	0	0	0	$000B_7,000B_6,000B_5,000B_4,$ $000B_3,000B_2,000B_1,000B_0$
									1		$00B_70,00B_60,00B_50,00B_40,$ $00B_30,00B_20,00B_10,00B_00$
									0	1	$0B_700,0B_600,0B_500,0B_400,$ $0B_300,0B_200,0B_100,0B_000$
									1		$B_7000,B_6000,B_5000,B_4000,$ $B_3000,B_2000,B_1000,B_0000$
							0	1	0	0	$SSSB_7,SSSB_6,SSSB_5,SSSB_4,$ $SSSB_3,SSSB_2,SSSB_1,SSSB_0$
									1		$SSB_7S,SSB_6S,SSB_5S,SSB_4S,$ $SSB_3S,SSB_2S,SSB_1S,SSB_0S$
									0	1	$SB_7SS,SB_6SS,SB_5SS,SB_4SS,$ $SB_3SS,SB_2SS,SB_1SS,SB_0SS$
									1		$B_7SSS,B_6SSS,B_5SSS,B_4SSS,$ $B_3SSS,B_2SSS,B_1SSS,B_0SSS$
							1	x	0	0	$B_7B_6B_5B_4,B_3B_2B_1B_0$
									1		$B_6B_7B_4B_5,B_2B_3B_0B_1$
									0	1	$B_5B_4B_7B_6,B_1B_0B_3B_2$
									1		$B_4B_5B_6B_7,B_0B_1B_2B_3$

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表 6-5: Half-word 数据处理

SSIZE [1:0]	Source data	Source data stream	SBX	SBS	DSIZE [1:0]	Destination data	PACK	SIGN	DBX	DHX	Destination data stream
01	half-word	$B_7B_6,B_5B_4,$ B_3B_2,B_1B_0	x	x	00	byte	0	x	0	x	B_6,B_4,B_2,B_0
									1		B_7,B_5,B_3,B_1
							1		0		$B_7,B_6,B_5,B_4,B_3,B_2,B_1,B_0$
					01	half-word	x		0		$B_7B_6,B_5B_4,B_3B_2,B_1B_0$
									1		$B_6B_7,B_4B_5,B_2B_3,B_0B_1$
					10	word	0	0	0	0	$00B_7B_6,00B_5B_4,$ $00B_3B_2,00B_1B_0$
									1		$00B_6B_7,00B_4B_5,$ $00B_2B_3,00B_0B_1$
									0	1	$B_7B_600,B_5B_400,$ B_3B_200,B_1B_000
									1		$B_6B_700,B_4B_500,$ B_2B_300,B_0B_100
							0	1	0	0	$SSB_7B_6,SSB_5B_4,SSB_3B_2,SSB_1B_0$
									1		$SSB_6B_7,SSB_4B_5,SSB_2B_3,SSB_0B_1$
									0	1	$B_7B_6SS,B_5B_4SS,B_3B_2SS,B_1B_0SS$
									1		$B_6B_7SS,B_4B_5SS,B_2B_3SS,B_0B_1SS$
							1	x	0	0	$B_7B_6B_5B_4,B_3B_2B_1B_0$
									1		$B_6B_7B_4B_5,B_2B_3B_0B_1$
									0	1	$B_5B_4B_7B_6,B_1B_0B_3B_2$
									1		$B_4B_5B_6B_7,B_0B_1B_2B_3$

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表 6-6: Word 数据处理

SSIZE [1:0]	Source data	Source data stream	SBX	SBS	DSIZE [1:0]	Destination data	PACK	SIGN	DBX	DHX	Destination data stream
10	word	$B_7B_6B_5B_4$, $B_3B_2B_1B_0$	0	0	00	byte	0	x	0	0	B_4,B_0
									1		B_5,B_1
									0	1	B_6,B_2
									1		B_7,B_3
			0	0			1		0	0	$B_7,B_6,B_5,B_4,B_3,B_2,B_1,B_0$
			0	1							$B_4,B_7,B_6,B_5,B_0,B_3,B_2,B_1$
			1	0							$B_7,B_5,B_6,B_4,B_3,B_1,B_2,B_0$
			1	1							$B_4,B_6,B_7,B_5,B_0,B_2,B_3,B_1$
			0	0	01	half-word	0		0	0	B_5B_4,B_1B_0
									1		B_4B_5,B_0B_1
									0	1	B_7B_6,B_3B_2
									1		B_6B_7,B_2B_3
			0	1			0		0	0	B_6B_5,B_2B_1
									1		B_5B_6,B_1B_2
									0	1	B_4B_7,B_0B_3
									1		B_7B_4,B_3B_0
			1	0			0		0	0	B_6B_4,B_2B_0
									1		B_4B_6,B_0B_2
									0	1	B_7B_5,B_3B_1
									1		B_5B_7,B_1B_3
			0	0			1		0	0	$B_7B_6,B_5B_4,B_3B_2,B_1B_0$
									1		$B_6B_7,B_4B_5,B_2B_3,B_0B_1$
			0	1					0		$B_4B_7,B_6B_5,B_0B_3,B_2B_1$
									1		$B_7B_4,B_5B_6,B_3B_0,B_1B_2$
			1	0					0		$B_7B_5,B_6B_4,B_3B_1,B_2B_0$
									1		$B_5B_7,B_4B_6,B_1B_3,B_0B_2$
			1	1					0		$B_4B_6,B_7B_5,B_0B_2,B_3B_1$
									1		$B_6B_4,B_5B_7,B_2B_0,B_1B_3$
			0	0	10	word	x	x	0	0	$B_7B_6B_5B_4,B_3B_2B_1B_0$
									1		$B_6B_7B_4B_5,B_2B_3B_0B_1$
									0	1	$B_5B_4B_7B_6,B_1B_0B_3B_2$
									1		$B_4B_5B_6B_7,B_0B_1B_2B_3$
			0	1					0	0	$B_4B_7B_6B_5,B_0B_3B_2B_1$
									1		$B_7B_4B_5B_6,B_3B_0B_1B_2$
									0	1	$B_6B_5B_4B_7,B_2B_1B_0B_3$
									1		$B_5B_6B_7B_4,B_1B_2B_3B_0$
			1	0					0	0	$B_7B_5B_6B_4,B_3B_1B_2B_0$
									1		$B_5B_7B_4B_6,B_1B_3B_0B_2$
									0	1	$B_6B_4B_7B_5,B_2B_0B_3B_1$
									1		$B_4B_6B_5B_7,B_0B_2B_1B_3$
			1	1					0	0	$B_4B_6B_7B_5,B_0B_2B_3B_1$
									1		$B_6B_4B_5B_7,B_2B_0B_1B_3$
									0	1	$B_7B_5B_4B_6,B_3B_1B_0B_2$
									1		$B_5B_7B_6B_4,B_1B_3B_2B_0$

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6.1.16 链表模式

所有通道都支持链表模式。启动链表传输之前，首先需要在存储器中准备任务链表。链表存储首地址必须为 4 字节对齐。链表中的每个表项代表一个传输任务，占据 16 个字节的空间，分为传输表项和跳转表项两种类型。

表项存储规则如下：传输表项的下一个表项必须与该传输表项顺序存储，即下一个表项的首地址是该传输表项的首地址加 16 个字节；跳转表项指向的表项可以存储在任何 4 字节对齐的地址，与该跳转表项自身的存储位置无关。

表 6-7: 传输表项 (transfer list) 格式

transfer list	bit field															
baseaddr	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	NEXT	B	SFIX	DFIX	SBURST		DBURST		TEDGE	TPOL	SBX	SBS	DBX	DHX	PACK	SIGN
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RSVD	M2M	PL		SSIZE		DSIZE		SINC	DINC	RSVD	DIR	DELAY			
baseaddr+4	SADDR[31:0]															
baseaddr+8	DADDR[31:0]															
baseaddr+12	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TS								RSVD		CS					
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NDT[15:0]															

表 6-8: 跳转表项 (branch list) 格式

branch list	bit field															
baseaddr	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	NEXT	B	RSVD													
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LCNTCMP										RSVD		DELAY			
baseaddr+4	BLTADDR[31:0]															
baseaddr+8	BEQADDR[31:0]															
baseaddr+12	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TS								RSVD							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RSVD															

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表 6-9: 表项字域含义

字段	含义
NEXT	1: next list exists; 0: current list is the last list
B	1: current list is for branch. Next list is pointed by BLTADDR or BEQADDR. If next list is pointed to 0, linked-list will be finished; 0: current list is for transfer
SFIX	source burst initial address fix mode of current task
DFIX	destination burst initial address fix mode of current task
SBURST	source max burst beats of current task
DBURST	destination max burst beats of current task
TEDGE	trigger mode of NEXT task
TPOL	trigger polarity of NEXT task
SBX	source byte exchange of current task
SBS	source cyclic byte-right-shift of current task
DBX	destination byte exchange of current task
DHX	destination half-word exchange of current task
PACK	pack/unpack mode of current task
SIGN	sign extension mode of current task
M2M	memory-to-memory mode of current task
PL	priority level of current task
SSIZE	source data width of current task
DSIZE	destination data width of current task
SINC	source increment mode of current task
DINC	destination increment mode of current task
DIR	data transfer direction of current task
DELAY	set delay time before NEXT list start, after NEXT list triggered. Delay time is $T_{HCLK} \times 16 \times 2^{DELAY}$
SADDR	source address of current task
DADDR	destination address of current task
TS	trigger selection of NEXT task
CS	channel request selection of current task
NDT	number of data to transfer of current task
LCNTCMP	branch condition. If LCNT<LCNTCMP, then branch to BLTADDR, or else branch to BEQADDR
BLTADDR	Next list is pointed by BLTADDR if LCNT<LCNTCMP
BEQADDR	Next list is pointed by BEQADDR if LCNT≥LCNTCMP. If BEQADDR=0, linked-list will be finished

任务链表准备完成以后，选择触发源 (SELRx_TS) 和触发模式 (CCRx_TEDGE 和 CCRx_TPOL) 作为第一个任务的触发条件，将通道 LCRx_ADDR 指向通道链表存储首地址，并设置 LCRx_START 为 1，即可启动链表传输。

链表传输启动后，通道首先等待触发，当触发条件满足时开始读取第一个表项。传输表项中指定了当前任务的各项参数，通道根据这些参数启动任务的传输。表项中同时配置了下一个任务的触发条件以及启动下一项任务前的等待延时。当前任务传输完成后，通道开始等待下一个任务的触发条件，条件满足后再经过设定的等待延时后，读取下一个任务的表项，之后开始下一个任务的传输。链表的最后一个表项包含链表结束的标志 (NEXT=0)，

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以及链表结束的触发条件，同时配置了最后一个任务的各项参数。当通道完成最后一个任务的传输后，会等待链表结束的触发条件，并在条件满足后结束链表传输，通道关闭。

每个通道都有一个表项计数器，可以从 CSRx_LCNT 读出。链表启动后，计数器清 0。每个表项传输完成后，计数器加 1。

跳转表项会基于该计数值进行条件跳转。如果计数值小于 LCNTCMP，下一个表项地址为 BLTADDR，否则下一个表项地址为 BEQADDR。如果下一个表项地址为 0，则链表传输任务结束。如果将 LCNTCMP 设置为 0，BEQADDR 设置为链表起始地址，可以实现无限循环的链表。

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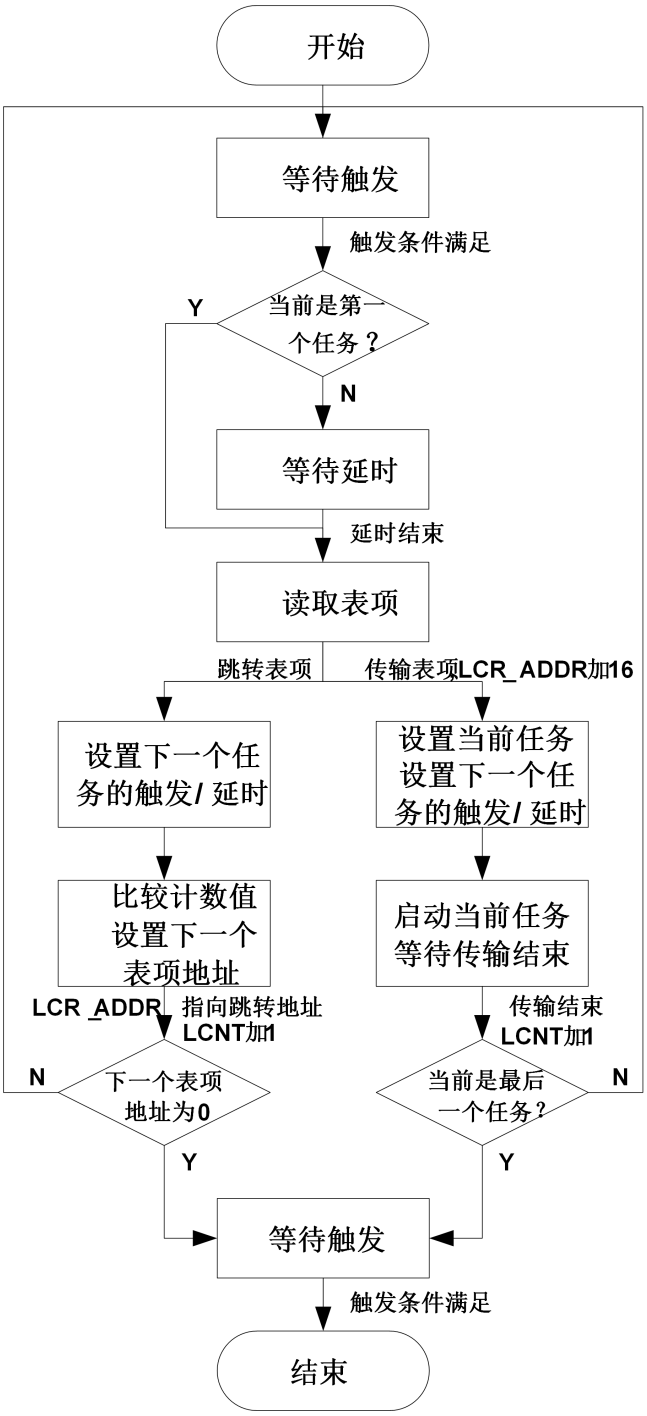
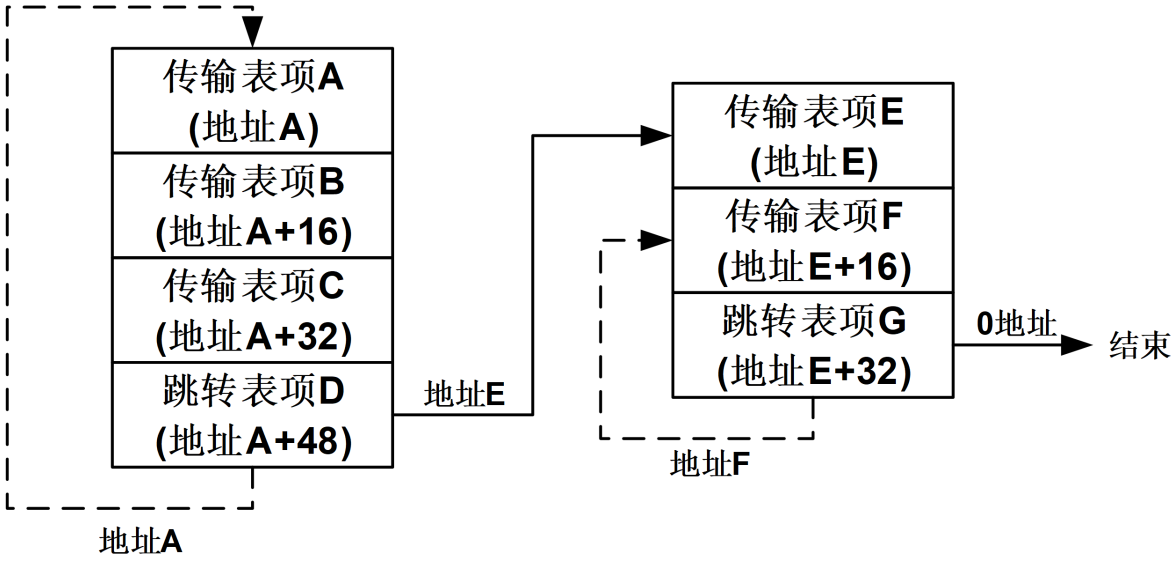


图 6-2: 链表模式执行流程

下图是链表模式下表项存储与执行流程的一个示例。表项 ABCD 顺序存储在地址 A 开始的地址空间，表项 EFG 顺序存储在地址 E 开始的地址空间。表项 ABCD 顺序执行，当执行到表项 D 时，判断计数条件，跳转到表项 A 或表项 E 执行；表项 EFG 顺序执行，当执行到表项 G 时，判断计数条件，跳转到表项 F 或结束链表。

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6.1.17 通知机制

GPDMA 每个通道可独立产生中断和 PTM 触发信号，并可单独配置每种中断的使能。通道传输完成至少一半时，产生 HTIFx 中断和触发。通道单次传输完成后，产生 TCIFx 中断和触发。通道传输全部完成后，产生 LCIFx 中断和触发。通道传输发生总线访问错误时，产生 TEIFx 中断和触发。以上中断任一种发生时，产生 GIFx 中断。通道中断可单独清除，或通过 CGIFx 一并清除。

6.1.18 通道基础模式配置流程

配置 GPDMA 通道基础模式按照以下步骤操作：

1. 在 CPARx 寄存器中设置外设寄存器地址。
   - 在外设请求发生后，或在存储器模式下使能通道后，会将数据从该地址移至存储器或从存储器移至该地址。
2. 设置 CM0ARx 寄存器中的存储器地址。
   - 在外设请求发生后，或在存储器模式下使能通道后，会将数据写入存储器或从存储器读取数据。
3. 确保 CCRx_EN 为 0 时，将待传输的单元数写入 CNDTRx 寄存器。
   - 每次数据传输后，该值都会递减。
4. 在 CCRx 寄存器中配置下列参数：
   - 通道优先级
   - 数据传输方向
   - 循环模式
   - 外设和存储器递增模式
   - 外设和存储器数据大小
   - 传输完成一半和/或全部完成以及/或者出现传输错误时的中断使能
5. 将 CCRx_EN 置 1 以激活通道。
   - 通道在使能后可处理来自此通道所连接外设的请求，或者启动存储器到存储器传输。

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6.1.19 通道链表模式配置流程

配置 GPDMA 通道链表模式按照以下步骤操作：

1. 在存储器中准备任务链表。链表可以位于 SRAM 或 PSRAM，存储首地址必须为 4 字节对齐，每个任务表项 16 个字节。顺序执行的传输表项和跳转表项必须顺序存储，而跳转表项指向的地址可以是任意 4 字节对齐的地址。
2. 在 SELRx_TS，CCRx_TEDGE 和 CCRx_TPOL 中配置第一项任务的触发条件。
3. 设置 CCRx_LCIE 使能通道传输完成中断
4. LCRx_ADDR 指向存储器中任务链表的首地址，并向 LCRx_START 写 1 启动链表任务。链表模式下通道使能会自动激活，因此不需要配置 CCRx_EN。

6.1.20 传输完成处理

基础模式和重复模式下，GPDMA 某通道传输完成后，CNDTRx 自动归零，软件需将该通道的 CCRx_EN 写 0 以避免下次配置时误触发。如果有中断标志出现，软件应当在进行相应处理后清除中断标志。

循环模式下 GPDMA 不会自动停止传输，当软件想要停止传输时，应将该通道的 CCRx_EN 写 0，并清除中断标志。

6.1.21 常见配置错误

- **FIFO 溢出**。读传输位宽 (由 CCRx_MSIZE 或 CCRx_PSIZE 决定) 与读传输突发长度 (由 CCRx_SBURST 决定) 的乘积，以及写传输位宽 (由 CCRx_MSIZE 或 CCRx_PSIZE 决定) 与写传输突发长度 (由 CCRx_DBURST 决定) 的乘积，均不能大于通道 FIFO 最大空间 (通道 1~2 为 64byte，通道 3~8 为 8byte)。
- **传输方向错误**。外设传输模式下，CCRx_DIR 配置应当与通道的外设请求相匹配。
- **打包数据量未对齐**。打包处理时的传输数量应当保证打包后的数据没有剩余。例如 byte 打包成 word 时，待传输的数据量应当为 4 的整数倍。
- **跳转表项条件计算错误**。跳转表项本身执行时也会增加计数值 LCNT。设置 LCNTMAX 时，应当将跳转表项自身，以及循环的次数都计算在内。

6.1.22 链表模式访问外设方法

GPDMA 的链表模式能够将若干次外设任务串联起来自动完成。为达到这个目的，GPDMA 在一次链表传输中既需要配置外设寄存器，又需要配置自身传输模式。推荐采用如下方式构建链表的表项:

任务 1 的外设配置 → 任务 1 的 DMA 配置 → 任务 2 的外设配置 → 任务 2 的 DMA 配置 → ...→ 任务 n 的外设配置 → 任务 n 的 DMA 配置

在任务的外设配置阶段，通道的目标地址指向外设的配置寄存器，从而更新外设的配置并启动外设。外设配置完成后，已经准备好传输，但是 GPDMA 还未给该外设分配可用资源，因此外设并不会启动传输。

在任务的 DMA 配置阶段，当前通道分配给该任务的外设，开启指定数据量的单次 DMA 传输，并在传输完成后跳转到下一个任务。应当注意通道 DMA 搬运完成并不意味着外设工作完成，因此在该阶段往往需要将下一个任务的触发条件 (TS) 配置成当前外设的完成事件，或者等待一段时间 (DELAY)，以防外设工作还未结束时被下一个表项修改配置。

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启动链表之前，所有即将启动的外设应当提前初始化，处于仅需配置少量寄存器即可开启工作的状态，以节约通过 GPDMA 进行配置的数据量。

6.1.23 GPDMA 寄存器

GPDMA 的基地址是 0x50081000。

表 6-10: GPDMA 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**ISR**	
[31]	r	1'h0	TEIF8	channel transfer error flag
[30]	r	1'h0	HTIF8	channel half transfer flag
[29]	r	1'h0	TCIF8	channel transfer complete flag
[28]	r	1'h0	GIF8	channel global interrupt flag
[27]	r	1'h0	TEIF7	channel transfer error flag
[26]	r	1'h0	HTIF7	channel half transfer flag
[25]	r	1'h0	TCIF7	channel transfer complete flag
[24]	r	1'h0	GIF7	channel global interrupt flag
[23]	r	1'h0	TEIF6	channel transfer error flag
[22]	r	1'h0	HTIF6	channel half transfer flag
[21]	r	1'h0	TCIF6	channel transfer complete flag
[20]	r	1'h0	GIF6	channel global interrupt flag
[19]	r	1'h0	TEIF5	channel transfer error flag
[18]	r	1'h0	HTIF5	channel half transfer flag
[17]	r	1'h0	TCIF5	channel transfer complete flag
[16]	r	1'h0	GIF5	channel global interrupt flag
[15]	r	1'h0	TEIF4	channel transfer error flag
[14]	r	1'h0	HTIF4	channel half transfer flag
[13]	r	1'h0	TCIF4	channel transfer complete flag
[12]	r	1'h0	GIF4	channel global interrupt flag
[11]	r	1'h0	TEIF3	channel transfer error flag
[10]	r	1'h0	HTIF3	channel half transfer flag
[9]	r	1'h0	TCIF3	channel transfer complete flag
[8]	r	1'h0	GIF3	channel global interrupt flag
[7]	r	1'h0	TEIF2	channel transfer error flag
[6]	r	1'h0	HTIF2	channel half transfer flag
[5]	r	1'h0	TCIF2	channel transfer complete flag
[4]	r	1'h0	GIF2	channel global interrupt flag
[3]	r	1'h0	TEIF1	channel transfer error flag. Set when bus error detected. Cleared when write 1 to CTEIF or CGIF.
[2]	r	1'h0	HTIF1	channel half transfer flag. Set when half NDT are transferred. Cleared when write 1 to CHTIF or CGIF.
[1]	r	1'h0	TCIF1	channel transfer complete flag. Set when all NDT are transferred. Cleared when write 1 to CTCIF or CGIF.
[0]	r	1'h0	GIF1	channel global interrupt flag. Set when any of TEIF/HTIF/TCIF asserted. Cleared when TEIF/HTIF/TCIF all cleared.
0x04			**IFCR**	
[31]	w	1'h0	CTEIF8	CTEIF, transfer error flag clear
[30]	w	1'h0	CHTIF8	CHTIF, half transfer flag clear
[29]	w	1'h0	CTCIF8	CTCIF, transfer complete flag clear

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[28]	w	1'h0	CGIF8	CGIF, global interrupt flag clear
[27]	w	1'h0	CTEIF7	CTEIF, transfer error flag clear
[26]	w	1'h0	CHTIF7	CHTIF, half transfer flag clear
[25]	w	1'h0	CTCIF7	CTCIF, transfer complete flag clear
[24]	w	1'h0	CGIF7	CGIF, global interrupt flag clear
[23]	w	1'h0	CTEIF6	CTEIF, transfer error flag clear
[22]	w	1'h0	CHTIF6	CHTIF, half transfer flag clear
[21]	w	1'h0	CTCIF6	CTCIF, transfer complete flag clear
[20]	w	1'h0	CGIF6	CGIF, global interrupt flag clear
[19]	w	1'h0	CTEIF5	CTEIF, transfer error flag clear
[18]	w	1'h0	CHTIF5	CHTIF, half transfer flag clear
[17]	w	1'h0	CTCIF5	CTCIF, transfer complete flag clear
[16]	w	1'h0	CGIF5	CGIF, global interrupt flag clear
[15]	w	1'h0	CTEIF4	CTEIF, transfer error flag clear
[14]	w	1'h0	CHTIF4	CHTIF, half transfer flag clear
[13]	w	1'h0	CTCIF4	CTCIF, transfer complete flag clear
[12]	w	1'h0	CGIF4	CGIF, global interrupt flag clear
[11]	w	1'h0	CTEIF3	CTEIF, transfer error flag clear
[10]	w	1'h0	CHTIF3	CHTIF, half transfer flag clear
[9]	w	1'h0	CTCIF3	CTCIF, transfer complete flag clear
[8]	w	1'h0	CGIF3	CGIF, global interrupt flag clear
[7]	w	1'h0	CTEIF2	CTEIF, transfer error flag clear
[6]	w	1'h0	CHTIF2	CHTIF, half transfer flag clear
[5]	w	1'h0	CTCIF2	CTCIF, transfer complete flag clear
[4]	w	1'h0	CGIF2	CGIF, global interrupt flag clear
[3]	w	1'h0	CTEIF1	CTEIF, transfer error flag clear. Write 1 to clear TEIF.
[2]	w	1'h0	CHTIF1	CHTIF, half transfer flag clear. Write 1 to clear HTIF.
[1]	w	1'h0	CTCIF1	CTCIF, transfer complete flag clear. Write 1 to clear TCIF.
[0]	w	1'h0	CGIF1	CGIF, global interrupt flag clear. Write 1 to clear all TEIF/HTIF/TCIF.
0x08			**CCR1**	
[31:30]			RSVD	
[29]	rw	1'h0	SFIX	source burst initial address fix mode 0: burst address will increase normally 1: initial address of each source burst is fixed, but sequential address during source burst will increase normally
[28]	rw	1'h0	DFIX	destination burst start address fix mode 0: burst address will increase normally 1: initial address of each destination burst is fixed, but sequential address during destination burst will increase normally
[27:26]	rw	2'h0	SBURST	source max burst beats if possible. Should set to 0 if source increment mode is 0. 00: SINGLE, single burst. 01: INCR4, 4-beat incrementing burst 10: INCR8, 8-beat incrementing burst 11: INCR16, 16-beat incrementing burst

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[25:24]	rw	2'h0	DBURST	destination max burst beats if possible. Should set to 0 if destination increment mode is 0. 00: SINGLE, single burst. 01: INCR4, 4-beat incrementing burst 10: INCR8, 8-beat incrementing burst 11: INCR16, 16-beat incrementing burst
[23]	rw	1'h0	TEDGE	channel trigger mode 0: level mode 1: edge mode
[22]	rw	1'h0	TPOL	channel trigger polarity 0: high level or positive edge 1: low level or negtive edge
[21]	rw	1'h0	SBX	source byte exchange within the unaligned half-word of each source word 0: no byte-based exchange within the unaligned half-word of each source word 1: the two consecutive bytes within the unaligned half-word of each source word are exchanged.
[20]	rw	1'h0	SBS	source cyclic byte-right-shift within each source word 0: no shift 1: each byte is cyclic right-shifted within each source word, thus the least byte becomes the highest byte.
[19]	rw	1'h0	DBX	destination byte exchange 0: no byte-based exchange within half-word 1: the two consecutive bytes are exchanged in each destination half-word.
[18]	rw	1'h0	DHX	destination half-word exchange 0: no halfword-based exchanged within word 1: the two consecutive half-words are exchanged in each destination word.
[17]	rw	1'h0	PACK	pack/unpack mode when source size and destination size are different 0: no pack/unpack 1: pack/unpack
[16]	rw	1'h0	SIGN	sign extention mode when source size and destination size are different and no pack/unpack 0: zero bit extention 1: sign bit extention
[15]	rw	1'h0	LCIE	list complete interrupt enable 0: disabled 1: enabled
[14]	rw	1'h0	MEM2MEM	memory-to-memory mode 0: disabled 1: enabled
[13:12]	rw	2'h0	PL	priority level 00: low 01: medium 10: high 11: very high

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11:10]	rw	2'h0	MSIZE	memory size Defines the data size of each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: 24 bits
[9:8]	rw	2'h0	PSIZE	peripheral size Defines the data size of each DMA transfer to the identified peripheral. In memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: 24 bits
[7]	rw	1'h0	MINC	memory increment mode Defines the increment mode for each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 0: disabled 1: enabled
[6]	rw	1'h0	PINC	peripheral increment mode Defines the increment mode for each DMA transfer to the identified peripheral. n memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 0: disabled 1: enabled
[5]	rw	1'h0	CIRC	circular mode 0: disabled 1: enabled

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw	1'h0	DIR	data transfer direction This bit must be set only in memory-to-peripheral and peripheral-to-memory modes. 0: read from peripheral – Source attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. – Destination attributes are defined by MSIZE and MINC, plus the CM0/1ARx register. This is still valid in a peripheral-to-peripheral mode. 1: read from memory – Destination attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. – Source attributes are defined by MSIZE and MINC, plus the CM0/1ARx register. This is still valid in a peripheral-to-peripheral mode.
[3]	rw	1'h0	TEIE	transfer error interrupt enable 0: disabled 1: enabled
[2]	rw	1'h0	HTIE	half transfer interrupt enable 0: disabled 1: enabled
[1]	rw	1'h0	TCIE	transfer complete interrupt enable 0: disabled 1: enabled
[0]	rw	1'h0	EN	channel enable When a channel transfer error occurs, this bit is cleared by hardware. It can not be set again by software (channel x re-activated) until the TEIFx bit of the ISR register is cleared (by setting the CTEIFx bit of the IFCR register). 0: disabled 1: enabled
0x0C			**CNDTR1**	
[31:20]			RSVD	
[19:0]	rw	20'h0	NDT	number of data to transfer (0 to 220 - 1) This field is updated by hardware when the channel is enabled: – It is decremented after each single DMA 'read' transfer, indicating the remaining amount of data items to read. – It is kept at zero when the programmed amount of data to transfer is reached, if the channel is not in circular mode (CIRC = 0 in the CCRx register). – It is reloaded automatically by the previously programmed value, when the transfer is complete, if the channel is in circular mode (CIRC = 1). Transfer is completed when both NDT and DSTNDT reach zero. If this field is zero, no transfer can be served whatever the channel status (enabled or not).
0x10			**CPAR1**	

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	PA	peripheral address It contains the base address of the peripheral data register from/to which the data will be read/written. When PSIZE[1:0] = 01 (16 bits), should align to a half-word address. When PSIZE[1] = 1 (32/24 bits), should align to a word address. In memory-to-memory mode, this register identifies the memory destination address if DIR = 1 and the memory source address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral destination address DIR = 1 and the peripheral source address if DIR = 0.
0x14			**CM0AR1**	
[31:0]	rw	32'h0	MA	memory address It contains the base address of the memory from/to which the data will be read/written. When MSIZE[1:0] = 01 (16 bits), should align to a half-word address. When MSIZE[1] = 1 (32/24 bits), should align to a word address. In memory-to-memory mode, this register identifies the memory source address if DIR = 1 and the memory destination address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral source address DIR = 1 and the peripheral destination address if DIR = 0.
0x18			**CSR1**	
[31:22]	r	10'h0	LCNT	counter of completed lists. Cleared when linked-list starts. After each list transfer completes (both NDT and DSTNDT come to 0), LCNT is increased by 1, no matter whether next list have been triggered.
[21]	r	1'h0	CFGERR	indicate configuration error occurs
[20]	r	1'h0	BUSERR	indicate bus error occurs
[19:0]	r	20'h0	DSTNDT	indicate number of destination data to transfer (0 to 220 - 1) This field is updated by hardware when the channel is enabled, and should not be programmed by software – It is decremented after each single DMA 'write' transfer, indicating the remaining amount of data items to transfer. – It is reloaded automatically, when the transfer is complete, if the channel is in circular mode (CIRC = 1).
0x1C			**CCR2**	
[31:30]			RSVD	
[29]	rw	1'h0	SFIX	source burst initial address fix mode 0: burst address will increase normally 1: initial address of each source burst is fixed, but sequential address during source burst will increase normally
[28]	rw	1'h0	DFIX	destination burst start address fix mode 0: burst address will increase normally 1: initial address of each destination burst is fixed, but sequential address during destination burst will increase normally
[27:26]	rw	2'h0	SBURST	source max burst beats if possible. Should set to 0 if source increment mode is 0. 00: SINGLE, single burst. 01: INCR4, 4-beat incrementing burst 10: INCR8, 8-beat incrementing burst 11: INCR16, 16-beat incrementing burst

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[25:24]	rw	2'h0	DBURST	destination max burst beats if possible. Should set to 0 if destination increment mode is 0. 00: SINGLE, single burst. 01: INCR4, 4-beat incrementing burst 10: INCR8, 8-beat incrementing burst 11: INCR16, 16-beat incrementing burst
[23]	rw	1'h0	TEDGE	channel trigger mode 0: level mode 1: edge mode
[22]	rw	1'h0	TPOL	channel trigger polarity 0: high level or positive edge 1: low level or negtive edge
[21]	rw	1'h0	SBX	source byte exchange within the unaligned half-word of each source word 0: no byte-based exchange within the unaligned half-word of each source word 1: the two consecutive bytes within the unaligned half-word of each source word are exchanged.
[20]	rw	1'h0	SBS	source cyclic byte-right-shift within each source word 0: no shift 1: each byte is cyclic right-shifted within each source word, thus the least byte becomes the highest byte.
[19]	rw	1'h0	DBX	destination byte exchange 0: no byte-based exchange within half-word 1: the two consecutive bytes are exchanged in each destination half-word.
[18]	rw	1'h0	DHX	destination half-word exchange 0: no halfword-based exchanged within word 1: the two consecutive half-words are exchanged in each destination word.
[17]	rw	1'h0	PACK	pack/unpack mode when source size and destination size are different 0: no pack/unpack 1: pack/unpack
[16]	rw	1'h0	SIGN	sign extention mode when source size and destination size are different and no pack/unpack 0: zero bit extention 1: sign bit extention
[15]	rw	1'h0	LCIE	list complete interrupt enable 0: disabled 1: enabled
[14]	rw	1'h0	MEM2MEM	memory-to-memory mode 0: disabled 1: enabled
[13:12]	rw	2'h0	PL	priority level 00: low 01: medium 10: high 11: very high

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11:10]	rw	2'h0	MSIZE	memory size Defines the data size of each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: 24 bits
[9:8]	rw	2'h0	PSIZE	peripheral size Defines the data size of each DMA transfer to the identified peripheral. In memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: 24 bits
[7]	rw	1'h0	MINC	memory increment mode Defines the increment mode for each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 0: disabled 1: enabled
[6]	rw	1'h0	PINC	peripheral increment mode Defines the increment mode for each DMA transfer to the identified peripheral. n memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 0: disabled 1: enabled
[5]	rw	1'h0	CIRC	circular mode 0: disabled 1: enabled

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw	1'h0	DIR	data transfer direction This bit must be set only in memory-to-peripheral and peripheral-to-memory modes. 0: read from peripheral – Source attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. – Destination attributes are defined by MSIZE and MINC, plus the CM0/1ARx register. This is still valid in a peripheral-to-peripheral mode. 1: read from memory – Destination attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. – Source attributes are defined by MSIZE and MINC, plus the CM0/1ARx register. This is still valid in a peripheral-to-peripheral mode.
[3]	rw	1'h0	TEIE	transfer error interrupt enable 0: disabled 1: enabled
[2]	rw	1'h0	HTIE	half transfer interrupt enable 0: disabled 1: enabled
[1]	rw	1'h0	TCIE	transfer complete interrupt enable 0: disabled 1: enabled
[0]	rw	1'h0	EN	channel enable When a channel transfer error occurs, this bit is cleared by hardware. It can not be set again by software (channel x re-activated) until the TEIFx bit of the ISR register is cleared (by setting the CTEIFx bit of the IFCR register). 0: disabled 1: enabled
0x20			**CNDTR2**	
[31:20]			RSVD	
[19:0]	rw	20'h0	NDT	number of data to transfer (0 to 220 - 1) This field is updated by hardware when the channel is enabled: – It is decremented after each single DMA 'read' transfer, indicating the remaining amount of data items to read. – It is kept at zero when the programmed amount of data to transfer is reached, if the channel is not in circular mode (CIRC = 0 in the CCRx register). – It is reloaded automatically by the previously programmed value, when the transfer is complete, if the channel is in circular mode (CIRC = 1). Transfer is completed when both NDT and DSTNDT reach zero. If this field is zero, no transfer can be served whatever the channel status (enabled or not).
0x24			**CPAR2**	

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	PA	peripheral address It contains the base address of the peripheral data register from/to which the data will be read/written. When PSIZE[1:0] = 01 (16 bits), should align to a half-word address. When PSIZE[1] = 1 (32/24 bits), should align to a word address. In memory-to-memory mode, this register identifies the memory destination address if DIR = 1 and the memory source address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral destination address DIR = 1 and the peripheral source address if DIR = 0.
0x28			**CM0AR2**	
[31:0]	rw	32'h0	MA	memory address It contains the base address of the memory from/to which the data will be read/written. When MSIZE[1:0] = 01 (16 bits), should align to a half-word address. When MSIZE[1] = 1 (32/24 bits), should align to a word address. In memory-to-memory mode, this register identifies the memory source address if DIR = 1 and the memory destination address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral source address DIR = 1 and the peripheral destination address if DIR = 0.
0x2C			**CSR2**	
[31:22]	r	10'h0	LCNT	counter of completed lists. Cleared when linked-list starts. After each list transfer completes (both NDT and DSTNDT come to 0), LCNT is increased by 1, no matter whether next list have been triggered.
[21]	r	1'h0	CFGERR	indicate configuration error occurs
[20]	r	1'h0	BUSERR	indicate bus error occurs
[19:0]	r	20'h0	DSTNDT	indicate number of destination data to transfer (0 to 220 - 1) This field is updated by hardware when the channel is enabled, and should not be programmed by software – It is decremented after each single DMA 'write' transfer, indicating the remaining amount of data items to transfer. – It is reloaded automatically, when the transfer is complete, if the channel is in circular mode (CIRC = 1).
0x30			**CCR3**	
[31:30]			RSVD	
[29]	rw	1'h0	SFIX	source burst initial address fix mode 0: burst address will increase normally 1: initial address of each source burst is fixed, but sequential address during source burst will increase normally
[28]	rw	1'h0	DFIX	destination burst start address fix mode 0: burst address will increase normally 1: initial address of each destination burst is fixed, but sequential address during destination burst will increase normally
[27:26]	rw	2'h0	SBURST	source max burst beats if possible. Should set to 0 if source increment mode is 0. 00: SINGLE, single burst. 01: INCR4, 4-beat incrementing burst 10: INCR8, 8-beat incrementing burst 11: INCR16, 16-beat incrementing burst

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[25:24]	rw	2'h0	DBURST	destination max burst beats if possible. Should set to 0 if destination increment mode is 0. 00: SINGLE, single burst. 01: INCR4, 4-beat incrementing burst 10: INCR8, 8-beat incrementing burst 11: INCR16, 16-beat incrementing burst
[23]	rw	1'h0	TEDGE	channel trigger mode 0: level mode 1: edge mode
[22]	rw	1'h0	TPOL	channel trigger polarity 0: high level or positive edge 1: low level or negtive edge
[21]	rw	1'h0	SBX	source byte exchange within the unaligned half-word of each source word 0: no byte-based exchange within the unaligned half-word of each source word 1: the two consecutive bytes within the unaligned half-word of each source word are exchanged.
[20]	rw	1'h0	SBS	source cyclic byte-right-shift within each source word 0: no shift 1: each byte is cyclic right-shifted within each source word, thus the least byte becomes the highest byte.
[19]	rw	1'h0	DBX	destination byte exchange 0: no byte-based exchange within half-word 1: the two consecutive bytes are exchanged in each destination half-word.
[18]	rw	1'h0	DHX	destination half-word exchange 0: no halfword-based exchanged within word 1: the two consecutive half-words are exchanged in each destination word.
[17]	rw	1'h0	PACK	pack/unpack mode when source size and destination size are different 0: no pack/unpack 1: pack/unpack
[16]	rw	1'h0	SIGN	sign extention mode when source size and destination size are different and no pack/unpack 0: zero bit extention 1: sign bit extention
[15]	rw	1'h0	LCIE	list complete interrupt enable 0: disabled 1: enabled
[14]	rw	1'h0	MEM2MEM	memory-to-memory mode 0: disabled 1: enabled
[13:12]	rw	2'h0	PL	priority level 00: low 01: medium 10: high 11: very high

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11:10]	rw	2'h0	MSIZE	memory size Defines the data size of each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: 24 bits
[9:8]	rw	2'h0	PSIZE	peripheral size Defines the data size of each DMA transfer to the identified peripheral. In memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: 24 bits
[7]	rw	1'h0	MINC	memory increment mode Defines the increment mode for each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 0: disabled 1: enabled
[6]	rw	1'h0	PINC	peripheral increment mode Defines the increment mode for each DMA transfer to the identified peripheral. n memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 0: disabled 1: enabled
[5]	rw	1'h0	CIRC	circular mode 0: disabled 1: enabled

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw	1'h0	DIR	data transfer direction This bit must be set only in memory-to-peripheral and peripheral-to-memory modes. 0: read from peripheral – Source attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. – Destination attributes are defined by MSIZE and MINC, plus the CM0/1ARx register. This is still valid in a peripheral-to-peripheral mode. 1: read from memory – Destination attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. – Source attributes are defined by MSIZE and MINC, plus the CM0/1ARx register. This is still valid in a peripheral-to-peripheral mode.
[3]	rw	1'h0	TEIE	transfer error interrupt enable 0: disabled 1: enabled
[2]	rw	1'h0	HTIE	half transfer interrupt enable 0: disabled 1: enabled
[1]	rw	1'h0	TCIE	transfer complete interrupt enable 0: disabled 1: enabled
[0]	rw	1'h0	EN	channel enable When a channel transfer error occurs, this bit is cleared by hardware. It can not be set again by software (channel x re-activated) until the TEIFx bit of the ISR register is cleared (by setting the CTEIFx bit of the IFCR register). 0: disabled 1: enabled
0x34			**CNDTR3**	
[31:20]			RSVD	
[19:0]	rw	20'h0	NDT	number of data to transfer (0 to 220 - 1) This field is updated by hardware when the channel is enabled: – It is decremented after each single DMA 'read' transfer, indicating the remaining amount of data items to read. – It is kept at zero when the programmed amount of data to transfer is reached, if the channel is not in circular mode (CIRC = 0 in the CCRx register). – It is reloaded automatically by the previously programmed value, when the transfer is complete, if the channel is in circular mode (CIRC = 1). Transfer is completed when both NDT and DSTNDT reach zero. If this field is zero, no transfer can be served whatever the channel status (enabled or not).
0x38			**CPAR3**	

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	PA	peripheral address It contains the base address of the peripheral data register from/to which the data will be read/written. When PSIZE[1:0] = 01 (16 bits), should align to a half-word address. When PSIZE[1] = 1 (32/24 bits), should align to a word address. In memory-to-memory mode, this register identifies the memory destination address if DIR = 1 and the memory source address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral destination address DIR = 1 and the peripheral source address if DIR = 0.
0x3C			**CM0AR3**	
[31:0]	rw	32'h0	MA	memory address It contains the base address of the memory from/to which the data will be read/written. When MSIZE[1:0] = 01 (16 bits), should align to a half-word address. When MSIZE[1] = 1 (32/24 bits), should align to a word address. In memory-to-memory mode, this register identifies the memory source address if DIR = 1 and the memory destination address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral source address DIR = 1 and the peripheral destination address if DIR = 0.
0x40			**CSR3**	
[31:22]	r	10'h0	LCNT	counter of completed lists. Cleared when linked-list starts. After each list transfer completes (both NDT and DSTNDT come to 0), LCNT is increased by 1, no matter whether next list have been triggered.
[21]	r	1'h0	CFGERR	indicate configuration error occurs
[20]	r	1'h0	BUSERR	indicate bus error occurs
[19:0]	r	20'h0	DSTNDT	indicate number of destination data to transfer (0 to 220 - 1) This field is updated by hardware when the channel is enabled, and should not be programmed by software – It is decremented after each single DMA 'write' transfer, indicating the remaining amount of data items to transfer. – It is reloaded automatically, when the transfer is complete, if the channel is in circular mode (CIRC = 1).
0x44			**CCR4**	
[31:30]			RSVD	
[29]	rw	1'h0	SFIX	source burst initial address fix mode 0: burst address will increase normally 1: initial address of each source burst is fixed, but sequential address during source burst will increase normally
[28]	rw	1'h0	DFIX	destination burst start address fix mode 0: burst address will increase normally 1: initial address of each destination burst is fixed, but sequential address during destination burst will increase normally
[27:26]	rw	2'h0	SBURST	source max burst beats if possible. Should set to 0 if source increment mode is 0. 00: SINGLE, single burst. 01: INCR4, 4-beat incrementing burst 10: INCR8, 8-beat incrementing burst 11: INCR16, 16-beat incrementing burst

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[25:24]	rw	2'h0	DBURST	destination max burst beats if possible. Should set to 0 if destination increment mode is 0. 00: SINGLE, single burst. 01: INCR4, 4-beat incrementing burst 10: INCR8, 8-beat incrementing burst 11: INCR16, 16-beat incrementing burst
[23]	rw	1'h0	TEDGE	channel trigger mode 0: level mode 1: edge mode
[22]	rw	1'h0	TPOL	channel trigger polarity 0: high level or positive edge 1: low level or negtive edge
[21]	rw	1'h0	SBX	source byte exchange within the unaligned half-word of each source word 0: no byte-based exchange within the unaligned half-word of each source word 1: the two consecutive bytes within the unaligned half-word of each source word are exchanged.
[20]	rw	1'h0	SBS	source cyclic byte-right-shift within each source word 0: no shift 1: each byte is cyclic right-shifted within each source word, thus the least byte becomes the highest byte.
[19]	rw	1'h0	DBX	destination byte exchange 0: no byte-based exchange within half-word 1: the two consecutive bytes are exchanged in each destination half-word.
[18]	rw	1'h0	DHX	destination half-word exchange 0: no halfword-based exchanged within word 1: the two consecutive half-words are exchanged in each destination word.
[17]	rw	1'h0	PACK	pack/unpack mode when source size and destination size are different 0: no pack/unpack 1: pack/unpack
[16]	rw	1'h0	SIGN	sign extention mode when source size and destination size are different and no pack/unpack 0: zero bit extention 1: sign bit extention
[15]	rw	1'h0	LCIE	list complete interrupt enable 0: disabled 1: enabled
[14]	rw	1'h0	MEM2MEM	memory-to-memory mode 0: disabled 1: enabled
[13:12]	rw	2'h0	PL	priority level 00: low 01: medium 10: high 11: very high

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11:10]	rw	2'h0	MSIZE	memory size Defines the data size of each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: 24 bits
[9:8]	rw	2'h0	PSIZE	peripheral size Defines the data size of each DMA transfer to the identified peripheral. In memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: 24 bits
[7]	rw	1'h0	MINC	memory increment mode Defines the increment mode for each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 0: disabled 1: enabled
[6]	rw	1'h0	PINC	peripheral increment mode Defines the increment mode for each DMA transfer to the identified peripheral. n memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 0: disabled 1: enabled
[5]	rw	1'h0	CIRC	circular mode 0: disabled 1: enabled

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw	1'h0	DIR	data transfer direction This bit must be set only in memory-to-peripheral and peripheral-to-memory modes. 0: read from peripheral – Source attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. – Destination attributes are defined by MSIZE and MINC, plus the CM0/1ARx register. This is still valid in a peripheral-to-peripheral mode. 1: read from memory – Destination attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. – Source attributes are defined by MSIZE and MINC, plus the CM0/1ARx register. This is still valid in a peripheral-to-peripheral mode.
[3]	rw	1'h0	TEIE	transfer error interrupt enable 0: disabled 1: enabled
[2]	rw	1'h0	HTIE	half transfer interrupt enable 0: disabled 1: enabled
[1]	rw	1'h0	TCIE	transfer complete interrupt enable 0: disabled 1: enabled
[0]	rw	1'h0	EN	channel enable When a channel transfer error occurs, this bit is cleared by hardware. It can not be set again by software (channel x re-activated) until the TEIFx bit of the ISR register is cleared (by setting the CTEIFx bit of the IFCR register). 0: disabled 1: enabled
0x48			**CNDTR4**	
[31:20]			RSVD	
[19:0]	rw	20'h0	NDT	number of data to transfer (0 to 220 - 1) This field is updated by hardware when the channel is enabled: – It is decremented after each single DMA 'read' transfer, indicating the remaining amount of data items to read. – It is kept at zero when the programmed amount of data to transfer is reached, if the channel is not in circular mode (CIRC = 0 in the CCRx register). – It is reloaded automatically by the previously programmed value, when the transfer is complete, if the channel is in circular mode (CIRC = 1). Transfer is completed when both NDT and DSTNDT reach zero. If this field is zero, no transfer can be served whatever the channel status (enabled or not).
0x4C			**CPAR4**	

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	PA	peripheral address It contains the base address of the peripheral data register from/to which the data will be read/written. When PSIZE[1:0] = 01 (16 bits), should align to a half-word address. When PSIZE[1] = 1 (32/24 bits), should align to a word address. In memory-to-memory mode, this register identifies the memory destination address if DIR = 1 and the memory source address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral destination address DIR = 1 and the peripheral source address if DIR = 0.
0x50			**CM0AR4**	
[31:0]	rw	32'h0	MA	memory address It contains the base address of the memory from/to which the data will be read/written. When MSIZE[1:0] = 01 (16 bits), should align to a half-word address. When MSIZE[1] = 1 (32/24 bits), should align to a word address. In memory-to-memory mode, this register identifies the memory source address if DIR = 1 and the memory destination address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral source address DIR = 1 and the peripheral destination address if DIR = 0.
0x54			**CSR4**	
[31:22]	r	10'h0	LCNT	counter of completed lists. Cleared when linked-list starts. After each list transfer completes (both NDT and DSTNDT come to 0), LCNT is increased by 1, no matter whether next list have been triggered.
[21]	r	1'h0	CFGERR	indicate configuration error occurs
[20]	r	1'h0	BUSERR	indicate bus error occurs
[19:0]	r	20'h0	DSTNDT	indicate number of destination data to transfer (0 to 220 - 1) This field is updated by hardware when the channel is enabled, and should not be programmed by software – It is decremented after each single DMA 'write' transfer, indicating the remaining amount of data items to transfer. – It is reloaded automatically, when the transfer is complete, if the channel is in circular mode (CIRC = 1).
0x58			**CCR5**	
[31:30]			RSVD	
[29]	rw	1'h0	SFIX	source burst initial address fix mode 0: burst address will increase normally 1: initial address of each source burst is fixed, but sequential address during source burst will increase normally
[28]	rw	1'h0	DFIX	destination burst start address fix mode 0: burst address will increase normally 1: initial address of each destination burst is fixed, but sequential address during destination burst will increase normally
[27:26]	rw	2'h0	SBURST	source max burst beats if possible. Should set to 0 if source increment mode is 0. 00: SINGLE, single burst. 01: INCR4, 4-beat incrementing burst 10: INCR8, 8-beat incrementing burst 11: INCR16, 16-beat incrementing burst

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[25:24]	rw	2'h0	DBURST	destination max burst beats if possible. Should set to 0 if destination increment mode is 0. 00: SINGLE, single burst. 01: INCR4, 4-beat incrementing burst 10: INCR8, 8-beat incrementing burst 11: INCR16, 16-beat incrementing burst
[23]	rw	1'h0	TEDGE	channel trigger mode 0: level mode 1: edge mode
[22]	rw	1'h0	TPOL	channel trigger polarity 0: high level or positive edge 1: low level or negtive edge
[21]	rw	1'h0	SBX	source byte exchange within the unaligned half-word of each source word 0: no byte-based exchange within the unaligned half-word of each source word 1: the two consecutive bytes within the unaligned half-word of each source word are exchanged.
[20]	rw	1'h0	SBS	source cyclic byte-right-shift within each source word 0: no shift 1: each byte is cyclic right-shifted within each source word, thus the least byte becomes the highest byte.
[19]	rw	1'h0	DBX	destination byte exchange 0: no byte-based exchange within half-word 1: the two consecutive bytes are exchanged in each destination half-word.
[18]	rw	1'h0	DHX	destination half-word exchange 0: no halfword-based exchanged within word 1: the two consecutive half-words are exchanged in each destination word.
[17]	rw	1'h0	PACK	pack/unpack mode when source size and destination size are different 0: no pack/unpack 1: pack/unpack
[16]	rw	1'h0	SIGN	sign extention mode when source size and destination size are different and no pack/unpack 0: zero bit extention 1: sign bit extention
[15]	rw	1'h0	LCIE	list complete interrupt enable 0: disabled 1: enabled
[14]	rw	1'h0	MEM2MEM	memory-to-memory mode 0: disabled 1: enabled
[13:12]	rw	2'h0	PL	priority level 00: low 01: medium 10: high 11: very high

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11:10]	rw	2'h0	MSIZE	memory size Defines the data size of each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: 24 bits
[9:8]	rw	2'h0	PSIZE	peripheral size Defines the data size of each DMA transfer to the identified peripheral. In memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: 24 bits
[7]	rw	1'h0	MINC	memory increment mode Defines the increment mode for each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 0: disabled 1: enabled
[6]	rw	1'h0	PINC	peripheral increment mode Defines the increment mode for each DMA transfer to the identified peripheral. n memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 0: disabled 1: enabled
[5]	rw	1'h0	CIRC	circular mode 0: disabled 1: enabled

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw	1'h0	DIR	data transfer direction This bit must be set only in memory-to-peripheral and peripheral-to-memory modes. 0: read from peripheral – Source attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. – Destination attributes are defined by MSIZE and MINC, plus the CM0/1ARx register. This is still valid in a peripheral-to-peripheral mode. 1: read from memory – Destination attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. – Source attributes are defined by MSIZE and MINC, plus the CM0/1ARx register. This is still valid in a peripheral-to-peripheral mode.
[3]	rw	1'h0	TEIE	transfer error interrupt enable 0: disabled 1: enabled
[2]	rw	1'h0	HTIE	half transfer interrupt enable 0: disabled 1: enabled
[1]	rw	1'h0	TCIE	transfer complete interrupt enable 0: disabled 1: enabled
[0]	rw	1'h0	EN	channel enable When a channel transfer error occurs, this bit is cleared by hardware. It can not be set again by software (channel x re-activated) until the TEIFx bit of the ISR register is cleared (by setting the CTEIFx bit of the IFCR register). 0: disabled 1: enabled
0x5C			**CNDTR5**	
[31:20]			RSVD	
[19:0]	rw	20'h0	NDT	number of data to transfer (0 to 220 - 1) This field is updated by hardware when the channel is enabled: – It is decremented after each single DMA 'read' transfer, indicating the remaining amount of data items to read. – It is kept at zero when the programmed amount of data to transfer is reached, if the channel is not in circular mode (CIRC = 0 in the CCRx register). – It is reloaded automatically by the previously programmed value, when the transfer is complete, if the channel is in circular mode (CIRC = 1). Transfer is completed when both NDT and DSTNDT reach zero. If this field is zero, no transfer can be served whatever the channel status (enabled or not).
0x60			**CPAR5**	

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	PA	peripheral address It contains the base address of the peripheral data register from/to which the data will be read/written. When PSIZE[1:0] = 01 (16 bits), should align to a half-word address. When PSIZE[1] = 1 (32/24 bits), should align to a word address. In memory-to-memory mode, this register identifies the memory destination address if DIR = 1 and the memory source address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral destination address DIR = 1 and the peripheral source address if DIR = 0.
0x64			**CM0AR5**	
[31:0]	rw	32'h0	MA	memory address It contains the base address of the memory from/to which the data will be read/written. When MSIZE[1:0] = 01 (16 bits), should align to a half-word address. When MSIZE[1] = 1 (32/24 bits), should align to a word address. In memory-to-memory mode, this register identifies the memory source address if DIR = 1 and the memory destination address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral source address DIR = 1 and the peripheral destination address if DIR = 0.
0x68			**CSR5**	
[31:22]	r	10'h0	LCNT	counter of completed lists. Cleared when linked-list starts. After each list transfer completes (both NDT and DSTNDT come to 0), LCNT is increased by 1, no matter whether next list have been triggered.
[21]	r	1'h0	CFGERR	indicate configuration error occurs
[20]	r	1'h0	BUSERR	indicate bus error occurs
[19:0]	r	20'h0	DSTNDT	indicate number of destination data to transfer (0 to 220 - 1) This field is updated by hardware when the channel is enabled, and should not be programmed by software – It is decremented after each single DMA 'write' transfer, indicating the remaining amount of data items to transfer. – It is reloaded automatically, when the transfer is complete, if the channel is in circular mode (CIRC = 1).
0x6C			**CCR6**	
[31:30]			RSVD	
[29]	rw	1'h0	SFIX	source burst initial address fix mode 0: burst address will increase normally 1: initial address of each source burst is fixed, but sequential address during source burst will increase normally
[28]	rw	1'h0	DFIX	destination burst start address fix mode 0: burst address will increase normally 1: initial address of each destination burst is fixed, but sequential address during destination burst will increase normally
[27:26]	rw	2'h0	SBURST	source max burst beats if possible. Should set to 0 if source increment mode is 0. 00: SINGLE, single burst. 01: INCR4, 4-beat incrementing burst 10: INCR8, 8-beat incrementing burst 11: INCR16, 16-beat incrementing burst

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[25:24]	rw	2'h0	DBURST	destination max burst beats if possible. Should set to 0 if destination increment mode is 0. 00: SINGLE, single burst. 01: INCR4, 4-beat incrementing burst 10: INCR8, 8-beat incrementing burst 11: INCR16, 16-beat incrementing burst
[23]	rw	1'h0	TEDGE	channel trigger mode 0: level mode 1: edge mode
[22]	rw	1'h0	TPOL	channel trigger polarity 0: high level or positive edge 1: low level or negtive edge
[21]	rw	1'h0	SBX	source byte exchange within the unaligned half-word of each source word 0: no byte-based exchange within the unaligned half-word of each source word 1: the two consecutive bytes within the unaligned half-word of each source word are exchanged.
[20]	rw	1'h0	SBS	source cyclic byte-right-shift within each source word 0: no shift 1: each byte is cyclic right-shifted within each source word, thus the least byte becomes the highest byte.
[19]	rw	1'h0	DBX	destination byte exchange 0: no byte-based exchange within half-word 1: the two consecutive bytes are exchanged in each destination half-word.
[18]	rw	1'h0	DHX	destination half-word exchange 0: no halfword-based exchanged within word 1: the two consecutive half-words are exchanged in each destination word.
[17]	rw	1'h0	PACK	pack/unpack mode when source size and destination size are different 0: no pack/unpack 1: pack/unpack
[16]	rw	1'h0	SIGN	sign extention mode when source size and destination size are different and no pack/unpack 0: zero bit extention 1: sign bit extention
[15]	rw	1'h0	LCIE	list complete interrupt enable 0: disabled 1: enabled
[14]	rw	1'h0	MEM2MEM	memory-to-memory mode 0: disabled 1: enabled
[13:12]	rw	2'h0	PL	priority level 00: low 01: medium 10: high 11: very high

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11:10]	rw	2'h0	MSIZE	memory size Defines the data size of each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: 24 bits
[9:8]	rw	2'h0	PSIZE	peripheral size Defines the data size of each DMA transfer to the identified peripheral. In memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: 24 bits
[7]	rw	1'h0	MINC	memory increment mode Defines the increment mode for each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 0: disabled 1: enabled
[6]	rw	1'h0	PINC	peripheral increment mode Defines the increment mode for each DMA transfer to the identified peripheral. n memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 0: disabled 1: enabled
[5]	rw	1'h0	CIRC	circular mode 0: disabled 1: enabled

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw	1'h0	DIR	data transfer direction This bit must be set only in memory-to-peripheral and peripheral-to-memory modes. 0: read from peripheral – Source attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. – Destination attributes are defined by MSIZE and MINC, plus the CM0/1ARx register. This is still valid in a peripheral-to-peripheral mode. 1: read from memory – Destination attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. – Source attributes are defined by MSIZE and MINC, plus the CM0/1ARx register. This is still valid in a peripheral-to-peripheral mode.
[3]	rw	1'h0	TEIE	transfer error interrupt enable 0: disabled 1: enabled
[2]	rw	1'h0	HTIE	half transfer interrupt enable 0: disabled 1: enabled
[1]	rw	1'h0	TCIE	transfer complete interrupt enable 0: disabled 1: enabled
[0]	rw	1'h0	EN	channel enable When a channel transfer error occurs, this bit is cleared by hardware. It can not be set again by software (channel x re-activated) until the TEIFx bit of the ISR register is cleared (by setting the CTEIFx bit of the IFCR register). 0: disabled 1: enabled
0x70			**CNDTR6**	
[31:20]			RSVD	
[19:0]	rw	20'h0	NDT	number of data to transfer (0 to 220 - 1) This field is updated by hardware when the channel is enabled: – It is decremented after each single DMA 'read' transfer, indicating the remaining amount of data items to read. – It is kept at zero when the programmed amount of data to transfer is reached, if the channel is not in circular mode (CIRC = 0 in the CCRx register). – It is reloaded automatically by the previously programmed value, when the transfer is complete, if the channel is in circular mode (CIRC = 1). Transfer is completed when both NDT and DSTNDT reach zero. If this field is zero, no transfer can be served whatever the channel status (enabled or not).
0x74			**CPAR6**	

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	PA	peripheral address It contains the base address of the peripheral data register from/to which the data will be read/written. When PSIZE[1:0] = 01 (16 bits), should align to a half-word address. When PSIZE[1] = 1 (32/24 bits), should align to a word address. In memory-to-memory mode, this register identifies the memory destination address if DIR = 1 and the memory source address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral destination address DIR = 1 and the peripheral source address if DIR = 0.
0x78			**CM0AR6**	
[31:0]	rw	32'h0	MA	memory address It contains the base address of the memory from/to which the data will be read/written. When MSIZE[1:0] = 01 (16 bits), should align to a half-word address. When MSIZE[1] = 1 (32/24 bits), should align to a word address. In memory-to-memory mode, this register identifies the memory source address if DIR = 1 and the memory destination address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral source address DIR = 1 and the peripheral destination address if DIR = 0.
0x7C			**CSR6**	
[31:22]	r	10'h0	LCNT	counter of completed lists. Cleared when linked-list starts. After each list transfer completes (both NDT and DSTNDT come to 0), LCNT is increased by 1, no matter whether next list have been triggered.
[21]	r	1'h0	CFGERR	indicate configuration error occurs
[20]	r	1'h0	BUSERR	indicate bus error occurs
[19:0]	r	20'h0	DSTNDT	indicate number of destination data to transfer (0 to 220 - 1) This field is updated by hardware when the channel is enabled, and should not be programmed by software – It is decremented after each single DMA 'write' transfer, indicating the remaining amount of data items to transfer. – It is reloaded automatically, when the transfer is complete, if the channel is in circular mode (CIRC = 1).
0x80			**CCR7**	
[31:30]			RSVD	
[29]	rw	1'h0	SFIX	source burst initial address fix mode 0: burst address will increase normally 1: initial address of each source burst is fixed, but sequential address during source burst will increase normally
[28]	rw	1'h0	DFIX	destination burst start address fix mode 0: burst address will increase normally 1: initial address of each destination burst is fixed, but sequential address during destination burst will increase normally
[27:26]	rw	2'h0	SBURST	source max burst beats if possible. Should set to 0 if source increment mode is 0. 00: SINGLE, single burst. 01: INCR4, 4-beat incrementing burst 10: INCR8, 8-beat incrementing burst 11: INCR16, 16-beat incrementing burst

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[25:24]	rw	2'h0	DBURST	destination max burst beats if possible. Should set to 0 if destination increment mode is 0. 00: SINGLE, single burst. 01: INCR4, 4-beat incrementing burst 10: INCR8, 8-beat incrementing burst 11: INCR16, 16-beat incrementing burst
[23]	rw	1'h0	TEDGE	channel trigger mode 0: level mode 1: edge mode
[22]	rw	1'h0	TPOL	channel trigger polarity 0: high level or positive edge 1: low level or negtive edge
[21]	rw	1'h0	SBX	source byte exchange within the unaligned half-word of each source word 0: no byte-based exchange within the unaligned half-word of each source word 1: the two consecutive bytes within the unaligned half-word of each source word are exchanged.
[20]	rw	1'h0	SBS	source cyclic byte-right-shift within each source word 0: no shift 1: each byte is cyclic right-shifted within each source word, thus the least byte becomes the highest byte.
[19]	rw	1'h0	DBX	destination byte exchange 0: no byte-based exchange within half-word 1: the two consecutive bytes are exchanged in each destination half-word.
[18]	rw	1'h0	DHX	destination half-word exchange 0: no halfword-based exchanged within word 1: the two consecutive half-words are exchanged in each destination word.
[17]	rw	1'h0	PACK	pack/unpack mode when source size and destination size are different 0: no pack/unpack 1: pack/unpack
[16]	rw	1'h0	SIGN	sign extention mode when source size and destination size are different and no pack/unpack 0: zero bit extention 1: sign bit extention
[15]	rw	1'h0	LCIE	list complete interrupt enable 0: disabled 1: enabled
[14]	rw	1'h0	MEM2MEM	memory-to-memory mode 0: disabled 1: enabled
[13:12]	rw	2'h0	PL	priority level 00: low 01: medium 10: high 11: very high

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11:10]	rw	2'h0	MSIZE	memory size Defines the data size of each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: 24 bits
[9:8]	rw	2'h0	PSIZE	peripheral size Defines the data size of each DMA transfer to the identified peripheral. In memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: 24 bits
[7]	rw	1'h0	MINC	memory increment mode Defines the increment mode for each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 0: disabled 1: enabled
[6]	rw	1'h0	PINC	peripheral increment mode Defines the increment mode for each DMA transfer to the identified peripheral. n memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 0: disabled 1: enabled
[5]	rw	1'h0	CIRC	circular mode 0: disabled 1: enabled

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw	1'h0	DIR	data transfer direction This bit must be set only in memory-to-peripheral and peripheral-to-memory modes. 0: read from peripheral – Source attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. – Destination attributes are defined by MSIZE and MINC, plus the CM0/1ARx register. This is still valid in a peripheral-to-peripheral mode. 1: read from memory – Destination attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. – Source attributes are defined by MSIZE and MINC, plus the CM0/1ARx register. This is still valid in a peripheral-to-peripheral mode.
[3]	rw	1'h0	TEIE	transfer error interrupt enable 0: disabled 1: enabled
[2]	rw	1'h0	HTIE	half transfer interrupt enable 0: disabled 1: enabled
[1]	rw	1'h0	TCIE	transfer complete interrupt enable 0: disabled 1: enabled
[0]	rw	1'h0	EN	channel enable When a channel transfer error occurs, this bit is cleared by hardware. It can not be set again by software (channel x re-activated) until the TEIFx bit of the ISR register is cleared (by setting the CTEIFx bit of the IFCR register). 0: disabled 1: enabled
0x84			**CNDTR7**	
[31:20]			RSVD	
[19:0]	rw	20'h0	NDT	number of data to transfer (0 to 220 - 1) This field is updated by hardware when the channel is enabled: – It is decremented after each single DMA 'read' transfer, indicating the remaining amount of data items to read. – It is kept at zero when the programmed amount of data to transfer is reached, if the channel is not in circular mode (CIRC = 0 in the CCRx register). – It is reloaded automatically by the previously programmed value, when the transfer is complete, if the channel is in circular mode (CIRC = 1). Transfer is completed when both NDT and DSTNDT reach zero. If this field is zero, no transfer can be served whatever the channel status (enabled or not).
0x88			**CPAR7**	

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	PA	peripheral address It contains the base address of the peripheral data register from/to which the data will be read/written. When PSIZE[1:0] = 01 (16 bits), should align to a half-word address. When PSIZE[1] = 1 (32/24 bits), should align to a word address. In memory-to-memory mode, this register identifies the memory destination address if DIR = 1 and the memory source address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral destination address DIR = 1 and the peripheral source address if DIR = 0.
0x8C			**CM0AR7**	
[31:0]	rw	32'h0	MA	memory address It contains the base address of the memory from/to which the data will be read/written. When MSIZE[1:0] = 01 (16 bits), should align to a half-word address. When MSIZE[1] = 1 (32/24 bits), should align to a word address. In memory-to-memory mode, this register identifies the memory source address if DIR = 1 and the memory destination address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral source address DIR = 1 and the peripheral destination address if DIR = 0.
0x90			**CSR7**	
[31:22]	r	10'h0	LCNT	counter of completed lists. Cleared when linked-list starts. After each list transfer completes (both NDT and DSTNDT come to 0), LCNT is increased by 1, no matter whether next list have been triggered.
[21]	r	1'h0	CFGERR	indicate configuration error occurs
[20]	r	1'h0	BUSERR	indicate bus error occurs
[19:0]	r	20'h0	DSTNDT	indicate number of destination data to transfer (0 to 220 - 1) This field is updated by hardware when the channel is enabled, and should not be programmed by software – It is decremented after each single DMA 'write' transfer, indicating the remaining amount of data items to transfer. – It is reloaded automatically, when the transfer is complete, if the channel is in circular mode (CIRC = 1).
0x94			**CCR8**	
[31:30]			RSVD	
[29]	rw	1'h0	SFIX	source burst initial address fix mode 0: burst address will increase normally 1: initial address of each source burst is fixed, but sequential address during source burst will increase normally
[28]	rw	1'h0	DFIX	destination burst start address fix mode 0: burst address will increase normally 1: initial address of each destination burst is fixed, but sequential address during destination burst will increase normally
[27:26]	rw	2'h0	SBURST	source max burst beats if possible. Should set to 0 if source increment mode is 0. 00: SINGLE, single burst. 01: INCR4, 4-beat incrementing burst 10: INCR8, 8-beat incrementing burst 11: INCR16, 16-beat incrementing burst

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[25:24]	rw	2'h0	DBURST	destination max burst beats if possible. Should set to 0 if destination increment mode is 0. 00: SINGLE, single burst. 01: INCR4, 4-beat incrementing burst 10: INCR8, 8-beat incrementing burst 11: INCR16, 16-beat incrementing burst
[23]	rw	1'h0	TEDGE	channel trigger mode 0: level mode 1: edge mode
[22]	rw	1'h0	TPOL	channel trigger polarity 0: high level or positive edge 1: low level or negtive edge
[21]	rw	1'h0	SBX	source byte exchange within the unaligned half-word of each source word 0: no byte-based exchange within the unaligned half-word of each source word 1: the two consecutive bytes within the unaligned half-word of each source word are exchanged.
[20]	rw	1'h0	SBS	source cyclic byte-right-shift within each source word 0: no shift 1: each byte is cyclic right-shifted within each source word, thus the least byte becomes the highest byte.
[19]	rw	1'h0	DBX	destination byte exchange 0: no byte-based exchange within half-word 1: the two consecutive bytes are exchanged in each destination half-word.
[18]	rw	1'h0	DHX	destination half-word exchange 0: no halfword-based exchanged within word 1: the two consecutive half-words are exchanged in each destination word.
[17]	rw	1'h0	PACK	pack/unpack mode when source size and destination size are different 0: no pack/unpack 1: pack/unpack
[16]	rw	1'h0	SIGN	sign extention mode when source size and destination size are different and no pack/unpack 0: zero bit extention 1: sign bit extention
[15]	rw	1'h0	LCIE	list complete interrupt enable 0: disabled 1: enabled
[14]	rw	1'h0	MEM2MEM	memory-to-memory mode 0: disabled 1: enabled
[13:12]	rw	2'h0	PL	priority level 00: low 01: medium 10: high 11: very high

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11:10]	rw	2'h0	MSIZE	memory size Defines the data size of each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: 24 bits
[9:8]	rw	2'h0	PSIZE	peripheral size Defines the data size of each DMA transfer to the identified peripheral. In memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 00: 8 bits 01: 16 bits 10: 32 bits 11: 24 bits
[7]	rw	1'h0	MINC	memory increment mode Defines the increment mode for each DMA transfer to the identified memory. In memory-to-memory mode, this field identifies the memory source if DIR = 1 and the memory destination if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral source if DIR = 1 and the peripheral destination if DIR = 0. 0: disabled 1: enabled
[6]	rw	1'h0	PINC	peripheral increment mode Defines the increment mode for each DMA transfer to the identified peripheral. n memory-to-memory mode, this field identifies the memory destination if DIR = 1 and the memory source if DIR = 0. In peripheral-to-peripheral mode, this field identifies the peripheral destination if DIR = 1 and the peripheral source if DIR = 0. 0: disabled 1: enabled
[5]	rw	1'h0	CIRC	circular mode 0: disabled 1: enabled

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw	1'h0	DIR	data transfer direction This bit must be set only in memory-to-peripheral and peripheral-to-memory modes. 0: read from peripheral – Source attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. – Destination attributes are defined by MSIZE and MINC, plus the CM0/1ARx register. This is still valid in a peripheral-to-peripheral mode. 1: read from memory – Destination attributes are defined by PSIZE and PINC, plus the CPARx register. This is still valid in a memory-to-memory mode. – Source attributes are defined by MSIZE and MINC, plus the CM0/1ARx register. This is still valid in a peripheral-to-peripheral mode.
[3]	rw	1'h0	TEIE	transfer error interrupt enable 0: disabled 1: enabled
[2]	rw	1'h0	HTIE	half transfer interrupt enable 0: disabled 1: enabled
[1]	rw	1'h0	TCIE	transfer complete interrupt enable 0: disabled 1: enabled
[0]	rw	1'h0	EN	channel enable When a channel transfer error occurs, this bit is cleared by hardware. It can not be set again by software (channel x re-activated) until the TEIFx bit of the ISR register is cleared (by setting the CTEIFx bit of the IFCR register). 0: disabled 1: enabled
0x98			**CNDTR8**	
[31:20]			RSVD	
[19:0]	rw	20'h0	NDT	number of data to transfer (0 to 220 - 1) This field is updated by hardware when the channel is enabled: – It is decremented after each single DMA 'read' transfer, indicating the remaining amount of data items to read. – It is kept at zero when the programmed amount of data to transfer is reached, if the channel is not in circular mode (CIRC = 0 in the CCRx register). – It is reloaded automatically by the previously programmed value, when the transfer is complete, if the channel is in circular mode (CIRC = 1). Transfer is completed when both NDT and DSTNDT reach zero. If this field is zero, no transfer can be served whatever the channel status (enabled or not).
0x9C			**CPAR8**	

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	PA	peripheral address It contains the base address of the peripheral data register from/to which the data will be read/written. When PSIZE[1:0] = 01 (16 bits), should align to a half-word address. When PSIZE[1] = 1 (32/24 bits), should align to a word address. In memory-to-memory mode, this register identifies the memory destination address if DIR = 1 and the memory source address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral destination address DIR = 1 and the peripheral source address if DIR = 0.
0xA0			**CM0AR8**	
[31:0]	rw	32'h0	MA	memory address It contains the base address of the memory from/to which the data will be read/written. When MSIZE[1:0] = 01 (16 bits), should align to a half-word address. When MSIZE[1] = 1 (32/24 bits), should align to a word address. In memory-to-memory mode, this register identifies the memory source address if DIR = 1 and the memory destination address if DIR = 0. In peripheral-to-peripheral mode, this register identifies the peripheral source address DIR = 1 and the peripheral destination address if DIR = 0.
0xA4			**CSR8**	
[31:22]	r	10'h0	LCNT	counter of completed lists. Cleared when linked-list starts. After each list transfer completes (both NDT and DSTNDT come to 0), LCNT is increased by 1, no matter whether next list have been triggered.
[21]	r	1'h0	CFGERR	indicate configuration error occurs
[20]	r	1'h0	BUSERR	indicate bus error occurs
[19:0]	r	20'h0	DSTNDT	indicate number of destination data to transfer (0 to 220 - 1) This field is updated by hardware when the channel is enabled, and should not be programmed by software – It is decremented after each single DMA 'write' transfer, indicating the remaining amount of data items to transfer. – It is reloaded automatically, when the transfer is complete, if the channel is in circular mode (CIRC = 1).
0xA8			**CSELR1**	
[31]			RSVD	
[30:24]	rw	7'h0	C4S	DMA channel 4 request selection
[23]			RSVD	
[22:16]	rw	7'h0	C3S	DMA channel 3 request selection
[15]			RSVD	
[14:8]	rw	7'h0	C2S	DMA channel 2 request selection
[7]			RSVD	
[6:0]	rw	7'h0	C1S	DMA channel 1 request selection
0xAC			**CSELR2**	
[31]			RSVD	
[30:24]	rw	7'h0	C8S	DMA channel 8 request selection
[23]			RSVD	
[22:16]	rw	7'h0	C7S	DMA channel 7 request selection
[15]			RSVD	
[14:8]	rw	7'h0	C6S	DMA channel 6 request selection
[7]			RSVD	

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[6:0]	rw	7'h0	C5S	DMA channel 5 request selection
0xB0			**DBGSEL**	
[31:4]			RSVD	
[3:0]	rw	4'h0	DBGSEL	Debug data selection
0xB4			**SELR1**	
[31:16]			RSVD	
[15:8]	rw	8'h0	TS	DMA channel 1 trigger selection
[7]			RSVD	
[6:0]	rw	7'h0	CS	DMA channel 1 request selection. It's a mirror register of CSELR1.C1S
0xB8			**SELR2**	
[31:16]			RSVD	
[15:8]	rw	8'h0	TS	DMA channel 2 trigger selection
[7]			RSVD	
[6:0]	rw	7'h0	CS	DMA channel 2 request selection. It's a mirror register of CSELR1.C2S
0xBC			**SELR3**	
[31:16]			RSVD	
[15:8]	rw	8'h0	TS	DMA channel 3 trigger selection
[7]			RSVD	
[6:0]	rw	7'h0	CS	DMA channel 3 request selection. It's a mirror register of CSELR1.C3S
0xC0			**SELR4**	
[31:16]			RSVD	
[15:8]	rw	8'h0	TS	DMA channel 4 trigger selection
[7]			RSVD	
[6:0]	rw	7'h0	CS	DMA channel 4 request selection. It's a mirror register of CSELR1.C4S
0xC4			**SELR5**	
[31:16]			RSVD	
[15:8]	rw	8'h0	TS	DMA channel 5 trigger selection
[7]			RSVD	
[6:0]	rw	7'h0	CS	DMA channel 5 request selection. It's a mirror register of CSELR2.C5S
0xC8			**SELR6**	
[31:16]			RSVD	
[15:8]	rw	8'h0	TS	DMA channel 6 trigger selection
[7]			RSVD	
[6:0]	rw	7'h0	CS	DMA channel 6 request selection. It's a mirror register of CSELR2.C6S
0xCC			**SELR7**	
[31:16]			RSVD	
[15:8]	rw	8'h0	TS	DMA channel 7 trigger selection
[7]			RSVD	
[6:0]	rw	7'h0	CS	DMA channel 7 request selection. It's a mirror register of CSELR2.C7S
0xD0			**SELR8**	
[31:16]			RSVD	
[15:8]	rw	8'h0	TS	DMA channel 8 trigger selection
[7]			RSVD	
[6:0]	rw	7'h0	CS	DMA channel 8 request selection. It's a mirror register of CSELR2.C8S
0xD4			**LISR**	
[31:8]			RSVD	
[7]	r	1'h0	LCIF8	channel 8 list/repetition complete flag
[6]	r	1'h0	LCIF7	channel 7 list/repetition complete flag

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[5]	r	1'h0	LCIF6	channel 6 list/repetition complete flag
[4]	r	1'h0	LCIF5	channel 5 list/repetition complete flag
[3]	r	1'h0	LCIF4	channel 4 list/repetition complete flag
[2]	r	1'h0	LCIF3	channel 3 list/repetition complete flag
[1]	r	1'h0	LCIF2	channel 2 list/repetition complete flag
[0]	r	1'h0	LCIF1	channel 1 list/repetition complete flag
0xD8			**LIFCR**	
[31:8]			RSVD	
[7]	w	1'h0	CLCIF8	channel 8 list/repetition complete flag clear
[6]	w	1'h0	CLCIF7	channel 7 list/repetition complete flag clear
[5]	w	1'h0	CLCIF6	channel 6 list/repetition complete flag clear
[4]	w	1'h0	CLCIF5	channel 5 list/repetition complete flag clear
[3]	w	1'h0	CLCIF4	channel 4 list/repetition complete flag clear
[2]	w	1'h0	CLCIF3	channel 3 list/repetition complete flag clear
[1]	w	1'h0	CLCIF2	channel 2 list/repetition complete flag clear
[0]	w	1'h0	CLCIF1	channel 1 list/repetition complete flag clear
0xDC			**CREPR1**	
[31:10]			RSVD	
[9:0]	rw	10'h0	CNT	repeat counter 0,1: no repetition others: repetition mode. Dma transfer will repeat for CNT times in direct mode. PA and MA may increase after each repetition.
0xE0			**CINCR1**	
[31:16]	rw	16'h0	PINC	peripheral address increment PA will be increased by PINC each time dma transfer done in repetition mode
[15:0]	rw	16'h0	MINC	memory address increment MA will be increased by MINC each time dma transfer done in repetition mode
0xE4			**LCR1**	
[31:2]	rw	30'h0	ADDR	linked-list address bit 31 to 2. address bit 1 and bit 0 is fixed to 0 (word aligned). Write before linked-list start as list start address. Read value indicate bit 31 to 2 of current list address if list has not been triggered, or next list address if current list has been triggered. After all lists finished, read value will be bit 31 to 2 of (last list address + 16)
[1]	r	1'h0	BUSY	linked-list busy 0: linked-list transfer idle 1: linked-list transfer is busy
[0]	w1s	1'h0	START	write 1 to start linked-list transfer. Will be cleared automatically
0xE8			**CREPR2**	
[31:10]			RSVD	
[9:0]	rw	10'h0	CNT	repeat counter 0,1: no repetition others: repetition mode. Dma transfer will repeat for CNT times in direct mode. PA and MA may increase after each repetition.
0xEC			**CINCR2**	
[31:16]	rw	16'h0	PINC	peripheral address increment PA will be increased by PINC each time dma transfer done in repetition mode

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[15:0]	rw	16'h0	MINC	memory address increment MA will be increased by MINC each time dma transfer done in repetition mode
0xF0			**LCR2**	
[31:2]	rw	30'h0	ADDR	linked-list address bit 31 to 2. address bit 1 and bit 0 is fixed to 0 (word aligned). Write before linked-list start as list start address. Read value indicate bit 31 to 2 of current list address if list has not been triggered, or next list address if current list has been triggered. After all lists finished, read value will be bit 31 to 2 of (last list address + 16)
[1]	r	1'h0	BUSY	linked-list busy 0: linked-list transfer idle 1: linked-list transfer is busy
[0]	w1s	1'h0	START	write 1 to start linked-list transfer. Will be cleared automatically
0xF4			**LCR3**	
[31:2]	rw	30'h0	ADDR	linked-list address bit 31 to 2. address bit 1 and bit 0 is fixed to 0 (word aligned). Write before linked-list start as list start address. Read value indicate bit 31 to 2 of current list address if list has not been triggered, or next list address if current list has been triggered. After all lists finished, read value will be bit 31 to 2 of (last list address + 16)
[1]	r	1'h0	BUSY	linked-list busy 0: linked-list transfer idle 1: linked-list transfer is busy
[0]	w1s	1'h0	START	write 1 to start linked-list transfer. Will be cleared automatically
0xF8			**LCR4**	
[31:2]	rw	30'h0	ADDR	linked-list address bit 31 to 2. address bit 1 and bit 0 is fixed to 0 (word aligned). Write before linked-list start as list start address. Read value indicate bit 31 to 2 of current list address if list has not been triggered, or next list address if current list has been triggered. After all lists finished, read value will be bit 31 to 2 of (last list address + 16)
[1]	r	1'h0	BUSY	linked-list busy 0: linked-list transfer idle 1: linked-list transfer is busy
[0]	w1s	1'h0	START	write 1 to start linked-list transfer. Will be cleared automatically
0xFC			**LCR5**	
[31:2]	rw	30'h0	ADDR	linked-list address bit 31 to 2. address bit 1 and bit 0 is fixed to 0 (word aligned). Write before linked-list start as list start address. Read value indicate bit 31 to 2 of current list address if list has not been triggered, or next list address if current list has been triggered. After all lists finished, read value will be bit 31 to 2 of (last list address + 16)
[1]	r	1'h0	BUSY	linked-list busy 0: linked-list transfer idle 1: linked-list transfer is busy
[0]	w1s	1'h0	START	write 1 to start linked-list transfer. Will be cleared automatically
0x100			**LCR6**	

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表 6-10: GPDMA 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:2]	rw	30'h0	ADDR	linked-list address bit 31 to 2. address bit 1 and bit 0 is fixed to 0 (word aligned). Write before linked-list start as list start address. Read value indicate bit 31 to 2 of current list address if list has not been triggered, or next list address if current list has been triggered. After all lists finished, read value will be bit 31 to 2 of (last list address + 16)
[1]	r	1'h0	BUSY	linked-list busy 0: linked-list transfer idle 1: linked-list transfer is busy
[0]	w1s	1'h0	START	write 1 to start linked-list transfer. Will be cleared automatically
0x104			**LCR7**	
[31:2]	rw	30'h0	ADDR	linked-list address bit 31 to 2. address bit 1 and bit 0 is fixed to 0 (word aligned). Write before linked-list start as list start address. Read value indicate bit 31 to 2 of current list address if list has not been triggered, or next list address if current list has been triggered. After all lists finished, read value will be bit 31 to 2 of (last list address + 16)
[1]	r	1'h0	BUSY	linked-list busy 0: linked-list transfer idle 1: linked-list transfer is busy
[0]	w1s	1'h0	START	write 1 to start linked-list transfer. Will be cleared automatically
0x108			**LCR8**	
[31:2]	rw	30'h0	ADDR	linked-list address bit 31 to 2. address bit 1 and bit 0 is fixed to 0 (word aligned). Write before linked-list start as list start address. Read value indicate bit 31 to 2 of current list address if list has not been triggered, or next list address if current list has been triggered. After all lists finished, read value will be bit 31 to 2 of (last list address + 16)
[1]	r	1'h0	BUSY	linked-list busy 0: linked-list transfer idle 1: linked-list transfer is busy
[0]	w1s	1'h0	START	write 1 to start linked-list transfer. Will be cleared automatically

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7 连接外设

7.1 I2C

HPSYS 有 4 个 I2C。

7.1.1 简介

I2C(Inter-Integrated Circuit) 接口同时支持主设备与从设备角色，可作为主设备与 I2C 外设通信，也可作为从设备响应外部的 I2C 主设备。I2C 内置 8 字节 FIFO，可以进行单笔读写，也可通过 DMA 进行批量数据读写。I2C 支持标准模式 (standard-mode)、快速模式 (fast-mode)、增强快速模式 (fast-mode plus) 以及高速模式 (high-speed-mode)，最高速率可达 3.4Mbps。I2C 做主设备时，支持自动任务 (autonomous task) 模式，能够在配置后自动完成读写从设备的完整操作。

7.1.2 主要特性

可同时作为主设备与从设备

- 支持总线多主设备
- 支持标准模式 (最高 100kbps)
- 支持快速模式 (最高 400kbps)
- 支持增强快速模式 (最高 1Mbps)
- 支持高速模式 (最高 3.4Mbps)
- 作为主设备支持访问 7 比特或 10 比特寻址
- 作为从设备支持 7 比特寻址
- 可配置的总线时序
- 支持时钟延展 (clock stretching)
- 8 字节 FIFO，支持 DMA
- 可配置的数字防抖动电路
- 独立的功能时钟，支持系统时钟动态调节
- 自动任务模式 (AT)

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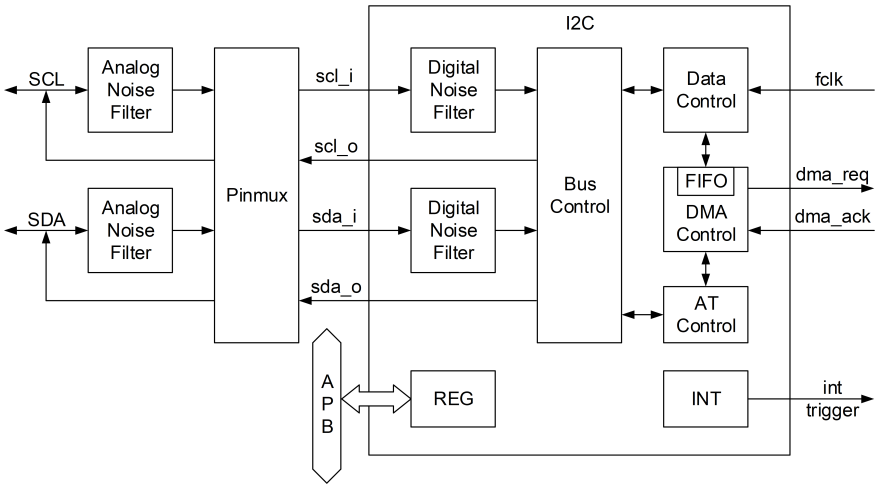


图 7-1: I2C 结构图

7.1.3 I2C 功能描述

7.1.3.1 两线传输

I2C 总线利用 SCL 与 SDA 两根线进行传输，其中 SCL 通常称为时钟线，SDA 通常称为数据线。两根线均为双向传输，且输出均为开漏模式，因此需要在芯片外部增加上拉电阻，阻值应根据最大传输速率决定。I2C 总线空闲时，SCL 与 SDA 均为上拉高电平。可通过 BMR_SCL 和 BMR_SDA 查询当前 I2C 总线信号电平。

7.1.3.2 输入滤波器

SCL 与 SDA 输入信号可经由模拟滤波器和数字滤波器滤除毛刺。模拟滤波器可滤除小于 50ns 的毛刺，在 PINMUX 模块中配置。数字滤波器可通过配置 CR_DNF 选择滤除毛刺的宽度上限，最大可配置为 7 个 fclk 周期 (约 146ns)。

7.1.3.3 传输速率

I2C 的传输速率主要由主设备决定，但当从设备支持时钟延展 (clock stretching) 时，也会受从设备影响。

I2C 接口时序基于 fclk 产生。该时钟来自芯片的外设时钟，独立于系统时钟，因此系统时钟频率的变化不会影响 I2C 的传输速率。需注意系统时钟频率会影响 DMA 搬运的速度，过低时可能造成 DMA 模式下 I2C 的 FIFO 溢出。

根据 I2C 协议，标准模式 (standard-mode) 比特率最高为 100kbps，快速模式 (fast-mode) 比特率最高为 400kbps，增强快速模式 (fast-mode plus) 比特率最高为 1Mbps，高速模式 (high-speed mode) 比特率最高为 3.4Mbps。

标准模式的基础比特率可由下列近似公式计算：

$$bit\_rate = Ffclk/(LCR\_SLV + max(LCR\_SLV, (WCR\_CNT \times 2 + 6)) + 7 + CR\_DNF)$$

其中，Ffclk 为 fclk 的频率 (48MHz)。WCR_CNT 用于调整 SDA 与 SCL 边沿之间的偏移，以保证信号的建立与保持时间满足 I2C 协议，配置合理时不会影响比特率。

快速模式/增强快速模式的基础比特率可由下列近似公式计算：

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$$bitrate = Ffclk/(LCR\_FLV + max(LCR\_FLV, (WCR\_CNT \times 2 + 6)) + 7 + CR\_DNF)$$

7.1.3.4 传输序列

一次完整的 I2C 传输应基于下列传输序列进行：

1. 起始位。主设备发出，启动传输。
2. 7 比特从地址。主设备发出，用于选择从设备。
3. R/nW 比特。主设备发出，标志接收或发送方向。
4. ACK 比特。从设备发出，响应主设备请求。ACK=0 表示响应成功。ACK=1 则传输失败。
5. 8 比特数据。接收时由从设备发出，发送时由主设备发出。根据不同从设备的访问方式，可能代表寄存器地址或数据。
6. ACK 比特。接收时由主设备发出，发送时由从设备发出，是对之前 8 比特数据的响应。
7. 重复步骤 5-6 直至数据完成或出现 ACK=1。
8. 重复起始位 (回到步骤 1) 或停止位。主设备发出，重新启动传输或停止传输。

7.1.3.5 工作模式与状态

I2C 默认处于主模式，可以发起主动传输，但不监控总线上的地址传输。软件启动传输时，I2C 进入主发送或主接收状态。

若将 CR_SLVEN 置 1，则 I2C 进入主从模式，可以发起主动传输，同时监控总线上的地址传输。软件启动传输时，I2C 进入主发送或主接收状态。当监控到起始位之后的 7 位地址与 SAR_ADDR 相符时，I2C 根据 R/nW 比特进入从发送或从接收状态。

7.1.3.6 I2C 初始化流程

1. 配置 I2C 速率模式 CR_MODE，并根据速率配置相关时序寄存器 LCR、WCR 等
2. 配置 IER 使能所需中断
3. 使能 I2C，CR_SCLE=1，CR_IUE=1

7.1.3.7 主发送流程

1. 将从设备地址左移 1 位，拼上最低位 0，写入 DBR。
2. TCR=TCR_START;TCR|=TCR_TB。
3. 轮询 SR_TE 直到为 1，或等待发送完成 TE 中断。
4. SR_TE 写 1 清除标志。检查 SR_NACK，如果为 1 则发送停止位并中止传输。
5. 将待发送数据写入 DBR。
6. TCR=TCR_TB。
7. 轮询 SR_TE 直到为 1，或等待 TE 中断。
8. SR_TE 写 1 清除标志。检查 SR_NACK，如果为 1 则发送停止位并中止传输。
9. 重复步骤 5-8，如果是最后一笔数据则 TCR=TCR_TB|TCR_STOP，停止位会在发送完成后自动产生。

7.1.3.8 主接收流程

1. 将从设备地址左移 1 位，拼上最低位 1，写入 DBR。

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2. TCR=TCR_START;TCR|=TCR_TB。
3. 轮询 SR_TE 直到为 1，或等待 TE 中断。
4. SR_TE 写 1 清除标志。检查 SR_NACK，如果为 1 则发送停止位并中止传输。
5. TCR=TCR_TB。
6. 轮询 SR_RF 直到为 1，或等待接收完成 RF 中断。
7. SR_RF 写 1 清除标志。从 DBR 中获取接收的数据。
8. 重复步骤 5-7，如果是最后一笔数据则 TCR=TCR_TB|TCR_NACK。
9. TCR=TCR_MA，发送停止位。
10. 轮询 SR_UB 直到为 0，停止位发送完毕，TCR=0。

7.1.3.9 从发送流程

1. 当地址检测中断 SAD 触发后，自动回复 ACK。
2. SR_SAD 写 1 清除标志。读取 SR_RWM，1 表示从发送，0 表示从接收。假设当前 SR_RWM 为 1，进入从发送状态。
3. 将待发送数据写入 DBR。
4. TCR=TCR_TB。
5. 轮询 SR_TE 直到为 1，或等待 TE 中断。
6. SR_TE 写 1 清除标志。检查 SR_NACK，如果为 1 则中止传输。
7. 重复步骤 3-6，直到检测到停止位中断 SSD。
8. SR_SSD 写 1 清除标志。

7.1.3.10 从接收流程

1. 当地址检测中断 SAD 触发后，自动回复 ACK。
2. SR_SAD 写 1 清除标志。读取 SR_RWM，1 表示从发送，0 表示从接收。假设当前 SR_RWM 为 0，进入从接收状态。
3. TCR=TCR_TB。
4. 轮询 SR_RF 直到为 1，或等待接收完成 RF 中断。
5. SR_RF 写 1 清除标志。从 DBR 中获取接收的数据。
6. 重复步骤 3-5，如果缓存将满则 TCR=TCR_TB|TCR_NACK，直到检测到停止位中断 SSD。
7. SR_SSD 写 1 清除标志。

7.1.3.11 DMA 传输

I2C 处于主发送或主接收状态时，可以开启 DMA 传输。DMA 仅作用于数据段，不能用于传输从设备地址和 R/nW 比特。I2C 支持单次 DMA 最大 511byte 数据连续传输。如果有更多的数据传输需求，可以再次启动 DMA。

DMA 启动以后，传输过程不需要 CPU 参与，由 I2C 与 DMAC 模块直接交互完成传输，并产生中断 DMADONE。I2C 模块内置 8 字节 FIFO，用于在 DMA 传输过程中缓存数据。如果出现 FIFO 溢出，会产生上溢中断 OF 或下溢中断 UF。如果主发送过程中收到从设备产生的 ACK=1，数据传输会中止，并产生中断 DMADONE。

DMA 传输的字节数通过写 DNR_NDT 配置。剩余待传输字节数可以通过读 DNR_NDT 获取。在中断 DMADONE 发生时，通过读取 DNR_NDT 以及 SR_NACK 可以获知 DMA 传输是否正常完成。

将 CR_LASTSTOP 置 1 可以在本次 DMA 传输完成后自动发送停止位。将 CR_LASTNACK 置 1 可以在本次 DMA

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接收完成后自动回复 ACK=1。

使用 DMA 进行主发送或主接收的流程如下：

1. 将从设备地址左移 1 位，拼上最低位 R/nW，写入 DBR。
2. TCR=TCR_START;TCR|=TCR_TB。
3. 轮询 SR_TE 直到为 1，或等待发送完成 TE 中断。
4. SR_TE 写 1 清除标志。检查 SR_NACK，如果为 1 则发送停止位并中止传输。
5. 配置 DMAC 模块。通道外设选择为当前 I2C，数据宽度为单字节，外设地址为当前 I2C 的 FIFO 寄存器，并启动 DMAC 通道。
6. 配置 I2C 的 DMA。DNR_NDT 设为待传输字节数。如果 DMA 传输完成后需自动发送停止位，则将 CR_LASTSTOP 置 1。如果 DMA 传输完成后需自动回复 ACK=1，则将 CR_LASTNACK 置 1。CR_DMAEN 置 1 使能 DMA。
7. 等待 DMADONE 中断。
8. SR_DMADONE 写 1 清除标志。
9. 如果还需再次启动 DMA，重复步骤 5-8。
10. 轮询 SR_UB 直到为 0，停止位发送完毕。

7.1.3.12 自动任务 (AT) 模式

自动任务模式下，I2C 可作为主设备自主完成一次完整的对从设备的写入或读取操作，包括发起始位，从设备寻址 (写)，从设备寄存器寻址，写数据，重发起始位，从设备寻址 (读)，读数据，发终止位等步骤。从设备的 I2C 地址，寄存器地址，读写数据长度等都可以配置。单次配置 ATR 寄存器，即可触发一次读或写任务。任务完成后会产生中断或事件。

CPU 驱动写单字节 AT 流程

1. 开启 I2C 的 ATE 和 ATD 中断。
2. 将 ATR 寄存器的内容准备好，并单笔写入 ATR。其中 ATR_SLVA 为从设备的 I2C 地址，ATR_REGA 为从设备寄存器地址，待写数据放在 ATR_NDT 的低 8 位，ATR_RWN=0，ATR_TRIG=1,ATR_STOP=1,ATR_SLV=1,ATR_REG=1,ATR_D
3. 等待中断产生。

CPU 驱动读单字节 AT 流程

1. 开启 I2C 的 ATE 和 ATD 中断。
2. 将 ATR 寄存器的内容准备好，并单笔写入 ATR。其中 ATR_SLVA 为从设备的 I2C 地址，ATR_REGA 为从设备寄存器地址，ATR_RWN=1，ATR_TRIG=1,ATR_STOP=1,ATR_SLV=1,ATR_REG=1,ATR_DMA=0。
3. 等待中断产生。读取的数据保存在 DBR 寄存器中。

DMA 驱动写数据 AT 流程

1. 配置 DMAC 通道。
2. CR_LASTSTOP 应当为 1。
3. 开启 I2C 的 ATE 和 ATD 中断。
4. 将 ATR 寄存器的内容准备好，并单笔写入 ATR。其中 ATR_SLVA 为从设备的 I2C 地址，ATR_REGA 为从设备寄存器地址，ATR_NDT 为待写数据长度 (1~511 个字节)，ATR_RWN=0，ATR_TRIG=1, ATR_SLV=1,ATR_REG=1,ATR_DMA
5. 等待中断产生。

DMA 驱动读数据 AT 流程

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1. 配置 DMAC 通道。
2. CR_LASTSTOP 与 CR_LASTNACK 应当为 1。
3. 开启 I2C 的 ATE 和 ATD 中断。
4. 将 ATR 寄存器的内容准备好，并单笔写入 ATR。其中 ATR_SLVA 为从设备的 I2C 地址，ATR_REGA 为从设备寄存器地址，ATR_NDT 为待写数据长度 (1~511 个字节)，ATR_RWN=1，ATR_TRIG=1, ATR_SLV=1,ATR_REG=1,ATR_DMA
5. 等待中断产生。

7.1.3.13 总线异常恢复

由于电气干扰或设备异常，I2C 总线有时会出现卡死，表现为 I2C 发送或接收持续失败。当怀疑总线卡死时，可通过下述方法尝试恢复。

1. 复位 I2C 模块。CR_UR 置 1，等待 100us 后置 0。
2. 如果 BMR_SCL 和 BMR_SDA 均为 1，可将 CR_RSTREQ 置 1，并查询 CR_RSTREQ 直到变为 0。在此期间，I2C 会连续发送 RCCR_RSTCYC 个周期的时钟信号，从设备检测到这类总线信号后或可从异常中恢复。
3. 如果 BMR_SCL 或 BMR_SDA 持续为 0，怀疑上拉电阻失效或从设备挂死，需检查硬件电路或复位从设备。

7.1.4 I2C 寄存器

表 7-1: I2C 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**CR**	Control register
[31]	rw	1'h0	UR	Unit Reset. Software need first assert to reset then deassert to release. 0 = No reset. 1 = Reset I2C module.
[30]	rw	1'h0	RSTREQ	I2C will do bus reset upon this bit set. Will be cleared by HW automatically after RSTCYC cycles of SCL generated. 1 = request for i2c bus reset 0 = bus reset finished
[29]	rw	1'h0	BRGRST	Reset bus related state machine and signals. Will be cleared by HW automatically 1 = request for reset 0 = reset finished
[28:15]			RSVD	
[14:12]	rw	3'h0	DNF	Digital noise filter These bits are used to configure the digital noise filter on SDA and SCL input. The digital filter will filter spikes with a length of up to DNF[3:0]*Tpclk. 0: Digital filter disabled 1: Digital filter enabled and filtering capability up to 1 Tpclk ... 7: digital filter enabled and filtering capability up to 7 Tpclk Note: Digital filter is added to analog filter. Digital filter will introduce delay on SCL and SDA processing, which is essential in hs-mode.
[11]	rw	1'h0	SLVEN	Slave mode Enable for SCL. 0 = Disable slave mode. Will not monitor slave address on I2C bus. 1 = Enable slave mode. Will monitor slave address on I2C bus.
[10]	rw	1'h0	SDAGCD	Glitch cancellation Disable for SDA. 0 = Enable glitch cancellation for SDA 1 = Disable glitch cancellation for SDA

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表 7-1: I2C 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[9]	rw	1'h0	SCLPP	Push-pull mode Enable for SCL. 0 = open drain output for SCL. 1 = Push-pull output for SCL
[8]	rw	1'h0	MSDE	Master Stop Detected Enable: 0 = Master Stop Detect (MSD) status is not enabled. 1 = Master Stop Detect (MSD) status is enabled.
[7]	rw	1'h0	GCD	General Call Disable: 0 = Enable the I2C to respond to general call messages. 1 = Disable I2C response to general call messages as a slave. This bit must be set when sending a master mode general call message from the I2C.
[6]	rw	1'h1	LASTSTOP	Generate STOP for last DMA transfer
[5]	rw	1'h1	LASTNACK	Generate NACK for last DMA Read transfer
[4]	rw	1'h0	DMAEN	DMA Enable for both TX and RX 0 = DMA mode is NOT enabled 1 = DMA mode enabled
[3]	rw	1'h0	SCLE	SCL Enable: 0 = Disables the I2C from driving the SCL line. 1 = Enables the I2C clock output for master-mode operation.
[2]	rw	1'h0	IUE	I2C Unit Enable: 0 = Disables the unit and does not master any transactions or respond to any slave transactions. 1 = Enables the I2C (defaults to slave-receive mode). Software must guarantee the I2C bus is idle before setting this bit.
[1:0]	rw	2'h0	MODE	Bus Mode (Master operation): 2'b00: standard-mode 2'b01: fast-mode and fast-mode plus 2'b10: HS-mode (standard mode when not doing a high speed transfer) 2'b11: HS-mode (fast mode when not doing a high speed transfer) Bus Mode (Slave operation): 2'b0x: HS-mode is disabled. I2C unit uses Standard/Fast mode timing on the SDA pin. 2'b1x: HS-mode is enabled. I2C unit uses HS-mode timing on the SDA pin when a master code is received.
0x04			**TCR**	Transfer Control register
[31:8]			RSVD	
[7]	w1s	1'h0	ABORTDMA	Abort DMA operation. Will be cleared by HW automatically
[6]	w1s	1'h0	RXREQ	Request DMA RX. Will be cleared by HW automatically
[5]	w1s	1'h0	TXREQ	Request DMA TX. Will be cleared by HW automatically

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表 7-1: I2C 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw	1'h0	MA	Master Abort: Used by the I2C in master mode to generate a Stop without transmitting another data byte: 0 = The I2C transmits Stop on if TCR[STOP] is set. 1 = The I2C sends Stop without data transmission. When in master-transmit mode, after transmitting a data byte, the TCR[TB] bit is cleared. When no more data bytes need to be sent, setting master abort bit sends the Stop. The TCR[TB] bit must remain clear. In master-receive mode, when a NAK is sent without a Stop (TCR[STOP] bit was not set) and CPU does not send a repeated Start, setting this bit sends the Stop. Once again, the TCR[TB] bit must remain clear. Master Abort can be done immediately after the address phase (Master Transmit mode only).
[3]	rw	1'h0	NACK	The positive/negative acknowledge control bit, defines the type of acknowledge pulse sent by the I2C when in master receive mode: 0 = Send a positive acknowledge (ACK) pulse after receiving a data byte. 1 = Send a negative acknowledge (NACK) pulse after receiving a data byte. The I2C automatically sends an ACK pulse when responding to its slave address or when responding in slave-receive mode, regardless of the NACK control-bit setting.
[2]	rw	1'h0	STOP	Stop: Used to initiate a Stop condition after transferring the next data byte on the I2C bus when in master mode. In master-receive mode, the NACK control bit must be set in conjunction with the STOP bit. 0 = Do not send a Stop. 1 = Send a Stop.
[1]	rw	1'h0	START	Start: Used to initiate a Start condition to the I2C unit when in master mode. 0 = Do not send a Start pulse. 1 = Send a Start pulse.
[0]	rw	1'h0	TB	Transfer Byte: Used to send or receive a byte on the I2C bus: 0 = Cleared by I2C when the byte is sent/received. 1 = Send/receive a byte. CPU can monitor this bit to determine when the byte transfer has completed. In master or slave mode, after each byte transfer including acknowledge pulse, the I2C holds the SCL line low (inserting wait states) until TB is set.
0x08			**IER**	Interrupt Enable register
[31:18]			RSVD	
[17]	rw	1'h0	ATEIE	Autonomous Task Error Interrupt Enable 0 = Autonomous Task Error interrupt is not enabled 1 = Autonomous Task Error interrupt is enabled
[16]	rw	1'h0	ATDIE	Autonomous Task Done Interrupt Enable 0 = Autonomous Task Done interrupt is not enabled 1 = Autonomous Task Done interrupt is enabled
[15]	rw	1'h0	UFIE	FIFO Underflow Interrupt Enable 0 = FIFO Underflow interrupt is not enabled 1 = FIFO Underflow interrupt is enabled

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表 7-1: I2C 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[14]	rw	1'h0	OFIE	FIFO Overflow Interrupt Enable 0 = FIFO Overflow interrupt is not enabled 1 = FIFO Overflow interrupt is enabled
[13]	rw	1'h0	DMADONEIE	DMA Transaction Done Interrupt Enable 0 = DMA Transaction done interrupt is not enabled. 1 = DMA Transaction done interrupt is enabled.
[12]	rw	1'h0	MSDIE	Master Stop Detected Interrupt Enable: 0 = Disable interrupt. 1 = Enables the I2C unit to interrupt upon detecting a Master Stop sent by the I2C unit.
[11]			RSVD	
[10]	rw	1'h0	BEDIE	Bus Error Detected Interrupt Enable: 0 = Disable interrupt. 1 = Enables the I2C to interrupt for the following I2C bus errors: As a master transmitter, no ACK was detected after a byte was sent. As a slave receiver, the I2C generated a NACK pulse. Software is responsible for guaranteeing that misplaced Start and Stop conditions do not occur.
[9]	rw	1'h0	SADIE	Slave Address Detected Interrupt Enable: 0 = Disable interrupt. 1 = Enables the I2C to interrupt upon detecting a slave address match or a general call address.
[8]	rw	1'h0	GCADIE	General Call Address Detected Interrupt Enable: 0 = Disable interrupt. 1 = Enables the I2C to interrupt when General Call Address Detected.
[7]	rw	1'h0	RFIE	DBR Receive Full Interrupt Enable: 0 = Disable interrupt. 1 = Enables the I2C to interrupt when the DBR has received a data byte from the I2C bus.
[6]	rw	1'h0	TEIE	DBR Transmit Empty Interrupt Enable: 0 = Disable interrupt. 1 = Enables the I2C to interrupt after transmitting a byte onto the I2C bus.
[5]	rw	1'h0	ALDIE	Arbitration Loss Detected Interrupt Enable: 0 = Disable interrupt. 1 = Enables the I2C to interrupt upon losing arbitration while in master mode.
[4]	rw	1'h0	SSDIE	Slave Stop Detected Interrupt Enable: 0 = Disable interrupt. 1 = Enables the I2C to interrupt when it detects a Stop condition while in slave mode.
[3:0]			RSVD	
0x0C			**SR**	Status register
[31:18]			RSVD	
[17]	rw1c	1'h0	ATE	Autonomous Task Error. Asserted when Autonomous Task error occurs. Cleared if write 1
[16]	rw1c	1'h0	ATD	Autonomous Task Done. Asserted when Autonomous Task done. Cleared if write 1 or another autonomous task triggered
[15]	rw1c	1'h0	UF	FIFO Underflow Flag. Asserted when FIFO is empty and a POP request generated without a PUSH. Cleared if write 1

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表 7-1: I2C 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[14]	rw1c	1'h0	OF	FIFO Overflow Flag. Asserted when FIFO is full and a PUSH request generated without a POP. Cleared if write 1
[13]	rw1c	1'h0	DMADONE	DMA Transaction Done. Asserted when both APB and I2C bus have finished transfer. Cleared if write 1
[12]	rw1c	1'h0	MSD	Master Stop Detected: 0 = No Master Stop Detected. 1 = This bit is set by the I2C unit when all of the following are true: This bit is enabled (CR[MSDE] = 1); I2C unit is configured as a master; I2C transmits a STOP signal
[11]	r	1'h0	EBB	Early Bus Busy 0 = I2C bus is idle or the I2C is using the bus (that is, unit busy). 1 = Set when the unit detects that the SCL or SDA line is low without a START condition. Bit will remain set until the I2C unit detects the bus is idle by detecting a STOP condition. Bit will also be set whenever the IBB bit is set.
[10]	rw1c	1'h0	BED	Bus Error Detected: 0 = No error detected. 1 = The I2C sets this bit when it detects one of the following error conditions: As a master transmitter, no ACK was detected on the interface after a byte was sent. As a slave receiver, the I2C generates a NACK pulse. When an error occurs, I2C bus transactions continue. Software must guarantee that misplaced Start and Stop conditions do not occur.
[9]	rw1c	1'h0	SAD	Slave Address Detected: 0 = No slave address was detected. 1 = The I2C detected a seven-bit address that matches the general call address or SAR. An interrupt is signalled when enabled in the CR.
[8]	rw1c	1'h0	GCAD	General Call Address Detected: 0 = No general call address received. 1 = I2C received a general call address.
[7]	rw1c	1'h0	RF	DBR Receive Full: 0 = The DBR has not received a new data byte or the I2C is idle. 1 = The DBR register received a new data byte from the I2C bus. An interrupt is signalled when enabled in the CR.
[6]	rw1c	1'h0	TE	DBR Transmit Empty: 0 = The data byte is still being transmitted. 1 = The I2C has finished transmitting a data byte on the I2C bus. An interrupt is signalled when enabled in the CR.
[5]	rw1c	1'h0	ALD	Arbitration Loss Detected: Used during multi-master operation: 0 = Cleared when arbitration is won or never took place. 1 = Set when the I2C loses arbitration.
[4]	rw1c	1'h0	SSD	Slave Stop Detected: 0 = No Stop detected. 1 = Set when the I2C detects a Stop while in slave-receive or slave-transmit mode.
[3]	r	1'h0	IBB	I2C Bus Busy: 0 = I2C bus is idle or the I2C is using the bus (that is, unit busy). 1 = Set when the I2C bus is busy but local I2C is not involved in the transaction.

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表 7-1: I2C 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[2]	r	1'h0	UB	Unit Busy: 0 = I2C not busy. 1 = Set when local I2C is busy. This is defined as the time between the first Start and Stop.
[1]	r	1'h0	NACK	ACK/NACK Status: 0 = The I2C received or sent an ACK on the bus. 1 = The I2C received or sent a NACK.on the bus. This bit is used in slave-transmit mode to determine when the byte transferred is the last one. This bit is updated after each byte and ACK/NACK information is received.
[0]	r	1'h0	RWM	Read/write Mode: 0 = The I2C is in master-transmit or slave-receive mode. 1 = The I2C is in master-receive or slave-transmit mode. This is the R/nW bit of the slave address. It is cleared automatically by hardware after a Stop state.
0x10			**DBR**	Data Buffer register
[31:8]			RSVD	
[7:0]	rw	8'h0	DATA	use the I2C Data Buffer register to transmit and receive data from the I2C bus. The DBR is accessed by software on one Side and by the I2C Shift register on the other. The DBR receives data coming into the I2C unit after a full byte is received and acknowledged. CPU writes data going out of the I2C to the DBR and sends it to the serial bus. When the I2C is in transmit mode (master or slave), CPU writes data to the DBR over the internal bus. CPU write data to the DBR when a master transaction is initiated or when the DBR transmit-empty interrupt is signalled. Data moves from the DBR to the Shift register when the transfer byte bit is set. The DBR transmit-empty interrupt is signalled (if enabled) when a byte is transferred on the I2C bus and the acknowledge cycle is complete. If the DBR is not written, and a Stop condition is not in place before the I2C bus is ready to transfer the next byte packet, the I2C unit inserts wait states until CPU writes the DBR and sets the transfer byte bit. When the I2C is in receive mode (master or slave), CPU reads DBR data over the internal bus. CPU reads data from the DBR when the DBR receive-full interrupt is signalled. The data moves from the Shift register to the DBR when the acknowledge cycle is complete. The I2C inserts wait states until the DBR is read. After the software reads the DBR, CR[NACK] are written by the software, allowing the next byte transfer to proceed to the I2C bus. In DMA mode, DBR is automatically filled from FIFO in master transmit mode, or fetched and stored in FIFO in master receive mode until DMA done or aborted.
0x14			**SAR**	Slave Address Register
[31:7]			RSVD	
[6:0]	rw	7'h47	ADDR	The seven-bit address to which the I2C responds when in slave-receive mode
0x18			**LCR**	Load Count Register
[31:27]	rw	5'h1	HLVH	Decrementer Load value for High Speed Mode SCL (master mode) for high phase. Thigh=Tfclk*(HLVH+4+DNF)

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表 7-1: I2C 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[26:18]	rw	9'h7	HLVL	Decrementer Load value for High Speed Mode SCL (master mode) for low phase. Tlow=Tfclk*(HLVL+3+DNF). Data rate is generated as 1/(Thigh+Tlow), or fpclk/(HLVH+HLVL+7+2*DNF). 3.2Mbps data rate is generated by default if fclk is 48MHz. HLVL also controls setup time and hold time for START and STOP condition in High Speed Mode(master mode). Thdsta=Tsusta=Tsusto=Tfclk*(HLVL+1)
[17:9]	rw	9'h39	FLV	Decrementer Load value for Fast Mode (or Fast Mode Plus) SCL (master mode) for both high and low phase. Data rate is generated as Ffclk/(FLV+max(FLV,CNT*2+6)+7+DNF) approximately. 400kbps data rate is generated by default if fclk is 48MHz. FLV also controls setup time and hold time for START and STOP condition in Fast Mode(master mode). Thdsta=Tsusta=Tsusto=Tfclk*FLV
[8:0]	rw	9'hED	SLV	Decrementer Load value for Standard Mode SCL (master mode) for both high & low phase. Data rate is generated as Ffclk/(SLV+max(SLV,CNT*2+6)+7+DNF) approximately. 100kbps data rate is generated by default if fclk is 48MHz. SLV also controls setup time and hold time for START and STOP condition in Standard Mode(master mode). Thdsta=Tsusta=Tsusto=Tfclk*SLV
0x1C			**WCR**	Wait Count Register
[31:30]			RSVD	
[29:28]	rw	2'h0	DIV	reserved
[27:18]			RSVD	
[17:13]	rw	5'h0	HSCNT2	N/A
[12:8]	rw	5'h0	HSCNT1	Count value for defining high speed mode hold time. Thddat=Tfclk*max(3+DNF,HSCNT1)
[7:0]	rw	8'hA	CNT	Controls the counter values defining the setup and hold times in standard and fast mode Tvddat=Thddat=Tfclk*(CNT+2) Tsudat=max(Tlow-Thddat,Thddat) Lower counter values may violate setup and hold times.
0x20			**RCCR**	Bus Reset Cycle Counter Register
[31:4]			RSVD	
[3:0]	rw	4'h9	RSTCYC	The cycles of SCL during bus reset
0x24			**BMR**	Bus Monitor Register
[31:2]			RSVD	
[1]	r	1'h1	SCL	continuously reflects the value of the SCL pin. The values of these pins are recorded, so software can determine when the I2C bus is hung and the I2C unit must be reset.
[0]	r	1'h1	SDA	continuously reflects the value of the SDA pin.
0x28			**DNR**	DMA number register
[31:9]			RSVD	
[8:0]	rw	9'h0	NDT	Write as number of data to transfer in byte. Read as left data number to transfer
0x2C			**ATR**	Autonomous Task register
[31:25]	rw	7'h0	SLVA	7-bit I2C address of slave device for autonomous task

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表 7-1: I2C 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[24]	rw	1'h0	RWN	read or write task 0 = write mode. Write data to slave device 1 = read mode. Read data from slave device
[23:16]	rw	8'h0	REGA	register address of slave device for autonomous task
[15]	w1s	1'h0	TRIG	Trigger autonomous task. Will be cleared by HW automatically
[14:13]			RSVD	
[12]	rw	1'h1	STOP	0: tast end without STOP bit in non-DMA mode. In DMA mode, STOP bit depends on CR_LASTSTOP. 1: tast end with STOP bit in non-DMA mode. In DMA mode, STOP bit depends on CR_LASTSTOP.
[11]	rw	1'h1	SLV	0: the first slave address(write) will not be transmitted, however the second slave address(read) will be transmitted when read 1: the first slave address(write) will be transmitted when read and write, and the second slave address(read) will be transmitted when read
[10]	rw	1'h1	REG	0: register address of slave device will not be transmitted 1: register address of slave device will be transmitted
[9]	rw	1'h0	DMA	0 = DMA not enabled during autonomous task. Only single byte data will be transferred. Data to be written should reside in ATR_NDT[7:0], and read data will be stored in DBR_DATA when task completed. 1 = data will be transfered by DMA during autonomous task. Up to 511-byte data will be transferred according to ATR_NDT.
[8:0]	rw	9'h0	NDT	If ATR_DMA asserted, ATR_NDT is the byte number of data to be transferred by DMA during autonomous task. Left data number during transmission could be read from DNR_NDT. If ATR_DMA deasserted, ATR_NDT[7:0] is the data to be written in write mode.
0x30			**FIFO**	FIFO Register
[31:8]			RSVD	
[7:0]	rw	8'h0	DATA	Write to push send data into FIFO. Read to pop received data from FIFO
0x34			**DBG**	Debug Register
[31:0]	r	32'h0	DATA	Debug data

7.2 SPI

HPSYS 有 2 个 SPI。

7.2.1 简介

SPI 支持 4 种通信格式：SSP/SPI/Microwire 以及自定义的帧格式。SSP/SPI 为全双工通信协议，控制器可以配置为 Master 或 Slave 模式。Microwire 为半双工通信协议，控制器仅可配置为 Master 模式。自定义帧格式为半双工模式，控制器仅可配置为 Master 模式。SPI 控制器内置发送/接收 FIFO。发送 FIFO 和接收 FIFO 共享同一个地址，读该地址时访问接受 FIFO，写该地址时访问发送 FIFO。FIFO 支持软件访问模式和 DMA 访问模式。

7.2.2 主要特性

- 支持 3 种通信格式：SSP/SPI/Microwire
- 支持 4 到 32Bit 的数据宽度
- SPI 格式下时钟极性和相位可通过寄存器 SPO 和 SPH 设置

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- 片选信号极性可配
- FIFO 深度为 32Bits×16Entry
- 接收发送都支持 DMA 模式
- HPSYS 中的 SPI 最大时钟频率为 48MHz；LPSYS 中的 SPI 最大时钟频率为 24MHz

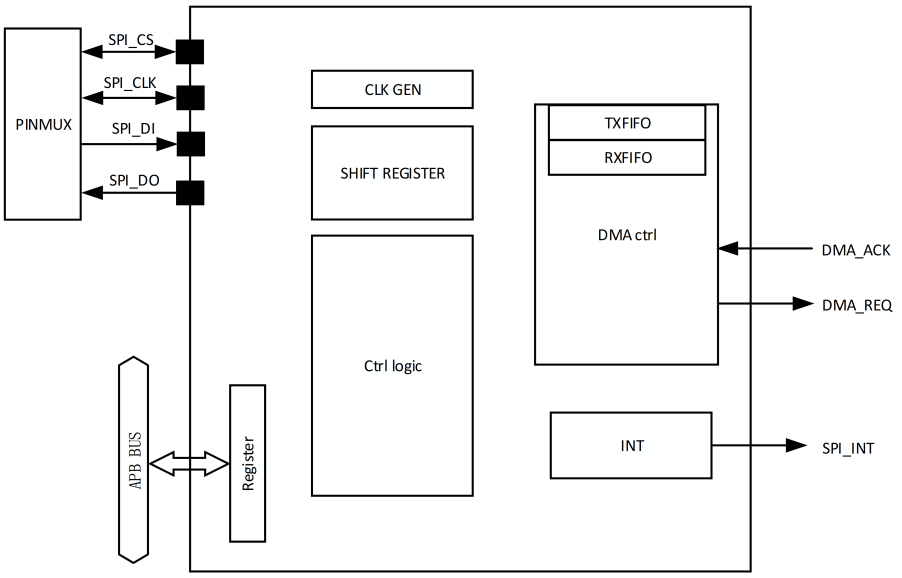


图 7-2: SPI 结构图

7.2.3 通信协议介绍

SSP 协议的通信时序如下：

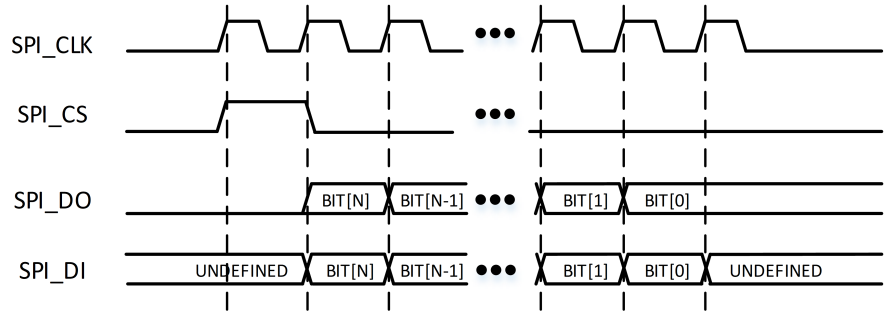


图 7-3: SSP 格式单次数据传输

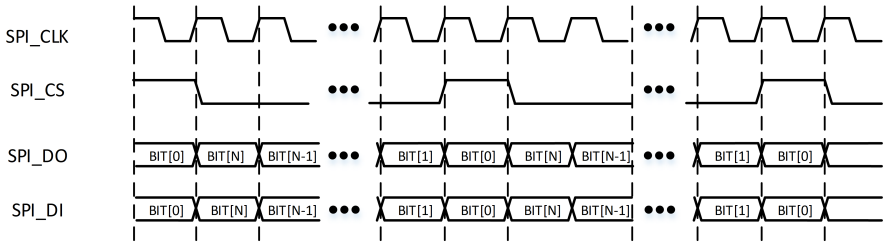


图 7-4: SSP 格式连续数据传输

SPI 协议的通信时序如下：

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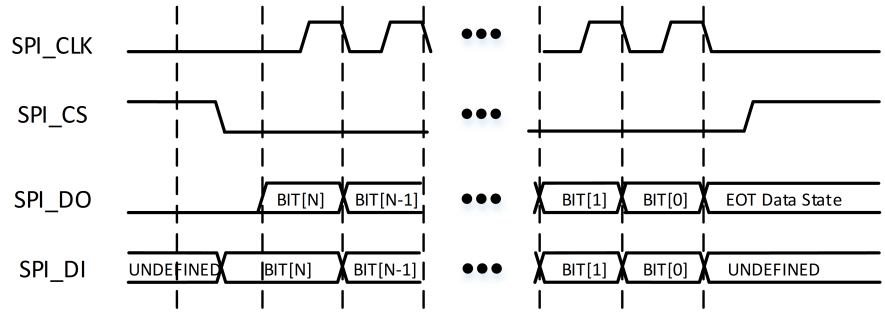


图 7-5: SPI 格式单次数据传输

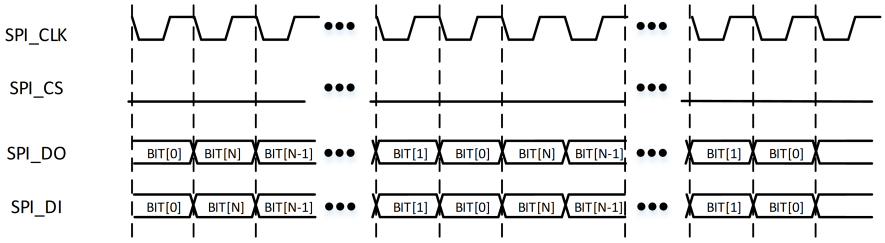


图 7-6: SPI 格式连续数据传输

以上 SPI 格式波形是在 SPO=0, SPH=0 的设置下的波形。SPO/SPH 可以配置为其他组合。

Microwire 协议的通信时序如下：

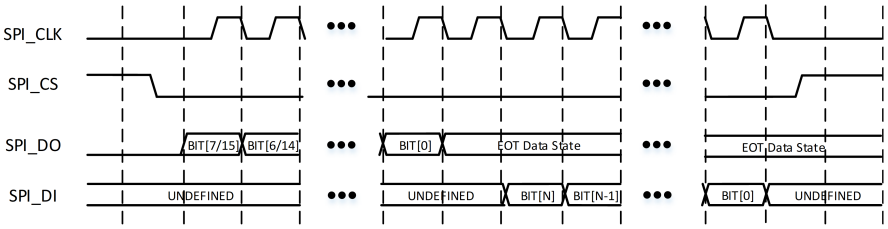


图 7-7: Microwire 格式单次数据传输

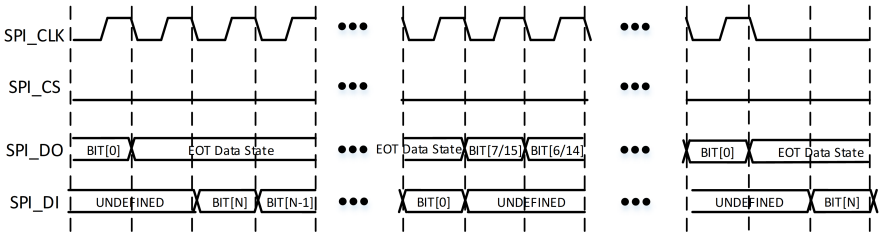


图 7-8: Microwire 格式连续数据传输

自定义帧格式支持读和写两种模式，自定义帧格式通信时序如下：

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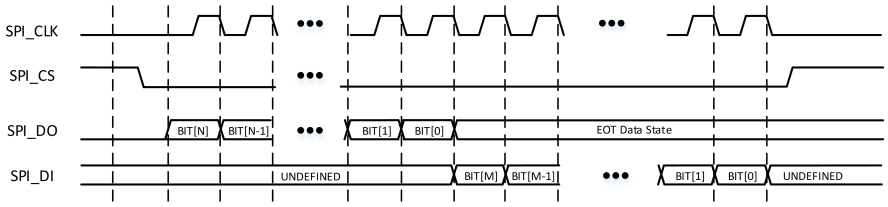


图 7-9: FRAME 读模式数据传输

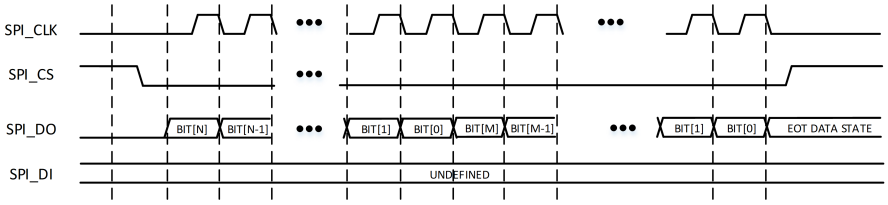


图 7-10: FRAME 写模式数据传输

自定义格式是半双工，支持三线模式和四线模式。

7.2.4 SPI 功能描述

7.2.4.1 通信协议设置

设置 FRF 可以选择通信协议：

- FRF=0：SPI 协议
- FRF=1：SSP 协议
- FRF=2：MicroWire 协议
- FRF=3：自定义帧格式

7.2.4.2 主机/从机设置

SFRMDIR=0，SCLKDIR=0：主机模式，SFRMDIR=1，SCLKDIR=1：从机模式

7.2.4.3 时钟频率设置

SPI 的时钟由源时钟及源时钟分频时钟二选一得到。分频时钟的频率为源时钟频率/CLK_DIV。源时钟频率在 HPSYS 中为 48MHz。设置 SPI 时钟的流程是：

1. 设置 CLK_DIV 配置分频时钟分频比
2. 设置 CLK_SEL 选择时钟来源，CLK_SEL=0：选择分频时钟，CLK_SEL=1：选择源时钟
3. 设置 CLK_SSP_EN 为 1 以使能 SPI 时钟

7.2.4.4 数据宽度设置

支持 4-32bit 的数据宽度，设置 DSS 可以配置数据位宽，数据位宽 =DSS+1。

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7.2.4.5 Microwire 格式数据长度设置

只支持 16/8bit 两种数据长度。数据长度在将 DSS 最高为设置成为 1 时是 16bit，将 DSS 最高位设置为 0 时时 8bit。

7.2.4.6 自定义格式数据长度设置

自定义格式需要定义 HEADER 的长度和数据的长度，即图 7 和图 8 中的 N 和 M。HEADER 的长度通过 FRM_HDR_LENGTH 设置，支持 0-32bit。数据的长度通过 SSPRWOTCCM 设置，长度为 SSPRWOTCCM+1。设置好 SSPRWOTCCM 后需要再将 SET_RWOT_CYCLE 写 1 以使设置生效。

7.2.4.7 自定义格式 HEADER 数据设置

通过写 FRM_HDR_DATA，

7.2.4.8 自定义格式收发模式设置

FRM_MODE=0：在 HEADER 后接收对端发来的数据。

FRM_MODE=1：在 HEADER 后继续向对端发数。

7.2.4.9 三线模式设置

在 SSP 和 SPI 格式下，可以通过软件处理实现实质上的三线半双工通信，从而省一个 GPIO。实现的方式是将 SPI_TRI_WIRE_EN 和 SPI_DI_SEL 都设为 1，在需要 RX 的时候软件将 TXD_OEN 设为 1，往 TXFIFO 写 0，然后读取 RXFIFO 里的数；在需要 TX 的时候软件将 TXD_OEN 设为 0，往 TXFIFO 写待发送数据，不关心 RXFIFO 里的内容。

在自定义格式下也支持三线模式，在写模式下，SPI 控制器始终驱动 IO；在读模式下，在发送 HEADER 时 SPI 控制器驱动 IO，在读数时候由外设驱动 IO，SPI 控制器从 IO 接收数据。软件需要将 SPI_TRI_WIRE_EN/SPI_DI_SEL/FRM_TRI_WIRE_ 都设为 1

7.2.4.10 FIFO 访问

在 TNF 为 1 前提下，CPU 或 DMA 写 DATA 寄存器：往 TXFIFO 中添加需要发送的数据

在 RNE 为 1 前提下，CPU 或 DMA 读 DATA 寄存器：从 RXFIFO 中读取收到的数据

7.2.4.11 DMA 接口配置

将 RSRE 写 1 使能 RX 数据的 DMA 功能。

将 TSRE 写 1 使能 TX 数据的 DMA 功能。

TXFIFO 可以设置 TFL 来设置阈值，在 TXFIFO 中的数少于或等于的 TFT 时候，SPI 控制器会发出 TX_DMA_REQ 给 DMA。

RXFIFO 可以设置 RFL 来设置阈值，在 RXFIFO 中的数多于或等于 RFT 的时候，SPI 控制器会发出 RX_DMA_REQ 给 DMA。

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有的情况下，RX 接收完成后 RXFIFO 里面的数会少于 RFL，从而无法发出 RX_DMA_REQ。这种情况可以通过给 CPU 发中断或者再给 DMA 发 RX_FIFO_REQ 来解决。

给 CPU 发中断需要设置 TIMEOUT 和使能 TINTE，TIMEOUT 值需大于数据长度。完成这两个设置后，如果 RX 结束并且 TIMEOUT 所设置的时间内没有对 RXFIFO 的读写，SPI 控制器会给 CPU 发中断，CPU 通过查看 FIFO 状态寄存器及读 FIFO 来确保所有数据被读走。

通过 DMA 来处理这种情况需要设置 TIMEOUT 和使能 TRAIL，TIMEOUT 值需大于数据长度。完成这两个设置后，如果 RX 结束并且 TIMEOUT 所设置的时间内没有对 RXFIFO 的读写，SPI 控制器会给 DMA 发出 RX_DMA_REQ，DMA 会根据设置处理 RXFIFO 中的数据。

7.2.4.12 SSP/SPI/Microwire 格式通信流程

1. 设置 pinmux
2. 设置 SPI 三线模式（如果需要）
3. 设置通信协议
4. 设置时钟频率
5. 设置数据位宽
6. 设置主从模式
7. 设置 DMA 接口参数（如果需要）
8. 将 SSE 写 1，使能 SPI
9. 访问 FIFO 开始收发

7.2.4.13 自定义格式通信流程

1. 设置 pinmux
2. 设置自定义格式三线模式（如果需要）
3. 设置为 Master 模式
4. 设置通信协议
5. 设置时钟频率
6. 配置 HEADER 数据和数据长度
7. 配置读写模式
8. 设置帧数据长度
9. 设置 DMA 接口参数（如果需要）
10. 将 SSE 写 1，使能 SPI
11. 写 FRM_START 启动自定义格式收发。
12. 访问 FIFO 开始收发

7.2.5 SPI 寄存器

表 7-2: SPI 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			TOP_CTRL	Top Control Register

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表 7-2: SPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31]	rw	1'h0	SSP_WORK_WIDTH_DYN_CHANGE	SSP_WORK_WIDTH_DYN_CHNAGE 1=SP can dynamicly change SSP_TOP_CTRL[9:5] without disabling SSP_TOP_CTRL[0] and re-enabling SSP_TOP_CTRL[0]
[30]	rw	1'h0	TXD_OEN	TXD_OEN 1=TXD is input 0=TXD is output
[29]	rw	1'h0	SPI_TRI_WIRE_EN	SPI_THREE_WIRE_MODE_EN 1=enable
[28]	rw	1'h0	SPI_DI_SEL	Select spi_di source. 0: from port DI. 1: from port DIO.
[27]	rw	1'h0	CLK_SSP_EN	write 0 to diable clk before clk setting is done
[26]	rw	1'h0	CLK_SEL	0: select clk_div as clk_ssp 1: select clk_sys as clk_ssp
[25:19]	rw	7'h0	CLK_DIV	div ratio from clk_sys
[18]	rw	1'b0	TTELP	TXD Three-state Enable On Last Phase 0 = TXDx is three-stated 1/2 clock cycle after the beginning of the LSB 1 = TXDx output signal is three-stated on the clock edge that ends the LSB
[17]	rw	1'b0	TTE	TXD Three-State Enable 0 = TXDx output signal is not three-stated 1 = TXD is three-stated when not transmitting data
[16]	rw	1'b0	SCFR	Slave Clock Free Running 0 = Clock input to SSPSCLKx is continuously running 1 = Clock input to SSPSCLKx is only active during data transfers.
[15]	rw	1'b0	IFS	Invert Frame Signal 0 = SSPSFRMx polarity is determined by the PSP polarity bits 1 = SSPSFRMx will be inverted from normal-SSPSFRMx (as defined by the PSP polarity bits). (Works in all frame formats: SPI, SSP, and PSP)
[14]	rw	1'b0	HOLD_FRAME_LOW	Hold Frame Low Control 1=After this field is set to 1 and the SSP is operating in master mode, the output frame clock ssp_sfrm_gpio will hold low. Used for SPI and NMW Format Rx FIFO Auto Full Control, which makes the frame clock is still low during there's no bit clock, or the data transfers before the stop clock will be discarded.
[13]	rw	1'b0	TRAIL	Trailing Byte 0 = Trailing bytes are handled by the <var Product Number> 1 = Trailing bytes are handled by DMA bursts
[12]	rw	1'b0	LBM	Loopback Mode (Test Mode Bit) 0 = Normal serial port operation is enabled 1 = Output of TX serial shifter is internally connected to input of RX serial shifter
[11]	rw	1'b0	SPH	Motorola SPI SSPSCLK phase setting 0 = SSPSCLKx is inactive until one cycle after the start of a frame and active until 1/2 cycle before the end of a frame 1 = SSPSCLKx is inactive until 1/2 cycle after the start of a frame and active until one cycle before the end of a frame
[10]	rw	1'b0	SPO	Motorola SPI SSPSCLK Polarity Setting 0 = The inactive or idle state of SSPSCLKx is low 1 = The inactive or idle state of SSPSCLKx is high
[9:5]	rw	5'h0	DSS	SSP Work data size, register bits value 0$~$31 indicated data size 1$~$32 bits, usually use data size 8bits, 16bits, 24bits, 32bits
[4]	rw	1'b0	SFRMDIR	SSP Frame (SSPSFRMx) Direction 0 = Master mode, SSPx port drives SSPSFRMx 1 = Slave mode, SSPx port receives SSPSFRMx

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表 7-2: SPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[3]	rw	1'b0	SCLKDIR	SSP Serial Bit Rate Clock (SSPSCLKx) Direction 0 = Master mode, SSPx port drives SSPSCLKx 1 = Slave mode, SSPx port receives SSPSCLKx
[2:1]	rw	2'h0	FRF	Frame Format 0x0 = Motorola* Serial Peripheral Interface (SPI) 0x1 = Texas Instruments* Synchronous Serial Protocol (SSP) 0x2 = National Semiconductor Microwire* 0x3 = Frame mode
[0]	rw	1'b0	SSE	Synchronous Serial Port Enable 0 = SSPx port is disabled 1 = SSPx port is enabled
0x04			**FIFO_CTRL**	FIFO Control Register
[31:20]			RSVD	
[19]	rw	1'b0	STRF	Select FIFO For Efwr (Test Mode Bit) Only when the <Enable FIFO Write/read> field = 1 0 = TXFIFO is selected for both writes and reads through the SSP Data Register 1 = RXFIFO is selected for both writes and reads through the SSP Data Register
[18]	rw	1'h0	EFWR	Enable FIFO Write/read (Test Mode Bit) 0 = FIFO write/read special function is disabled (normal SSPx operational mode) 1 = FIFO write/read special function is enabled
[17]	rw	1'h0	RXFIFO_AUTO_FULL_CTRL	Rx FIFO Auto Full Control: After this field is set to 1 and the SPI controller is operating in master mode, the controller FSM returns to IDLE state and stops the SPI_CLK when Rx FIFO is full. The controller FSM continues transferring data after the RxFIFO is not full. This field is used to avoid an RxFIFO overrun issue. 1: Enable Rx FIFO auto full control
[16]	rw	1'h0	FPCKE	FIFO Packing Enable 0 = FIFO packing mode disabled 1 = FIFO packing mode enabled
[15:14]	rw	2'h0	TXFIFO_WR_ENDIAN	apb_pwdata Write to Tx FIFO Endian 0x0 = txfifo_wdata[31:0] = apb_pwdata[31:0] 0x1 = fifo_wdata[31:0] = apb_pwdata[15:0], apb_pwdata[31:16] 0x2 = txfifo_wdata[31:0] = apb_pwdata[7:0], apb_pwdata[15:8], apb_pwdata[23:16], apb_pwdata[31:24] 0x3 = txfifo_wdata[31:0] = apb_pwdata[23:16], apb_pwdata[31:24], apb_pwdata[7:0], apb_pwdata[15:8]
[13:12]	rw	2'h0	RXFIFO_RD_ENDIAN	apb_prdata Read from Rx FIFO Endian 0x0 = apb_prdata[31:0] = rxfifo_wdata[31:0] 0x1 = apb_prdata[31:0] = rxfifo_wdata[15:0], rxfifo_wdata[31:16] 0x2 = apb_prdata[31:0]= rxfifo_wdata[7:0], rxfifo_wdata[15:8], rxfifo_wdata[23:16], rxfifo_wdata[31:24] 0x3 = apb_prdata[31:0]= rxfifo_wdata[23:16], rxfifo_wdata[31:24], rxfifo_wdata[7:0], rxfifo_wdata[15:8]
[11]	rw	1'h0	RSRE	Receive Service Request Enable 0 = DMA service request is disabled 1 = DMA service request is enabled
[10]	rw	1'h0	TSRE	Transmit Service Request Enable 0 = DMA service request is disabled 1 = DMA service request is enabled
[9:5]	rw	5'h0	RFT	RXFIFO Trigger Threshold This field sets the threshold level at which RXFIFO asserts interrupt. The level should be set to the preferred threshold value minus 1.

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表 7-2: SPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4:0]	rw	5'h0	TFT	TXFIFO Trigger Threshold This field sets the threshold level at which TXFIFO asserts interrupt. The level should be set to the preferred threshold value minus 1.
0x08			**INTE**	Interrupt Enable Register
[31:7]			RSVD	
[6]	rw	1'h0	EBCEI	Enable Bit Count Error Interrupt 0 = Interrupt due to a bit count error is disabled 1 = Interrupt due to a bit count error is enabled
[5]	rw	1'h0	TIM	Transmit FIFO Underrun Interrupt Mask 0 = TUR events generate an SSP interrupt 1 = TUR events do NOT generate an SSP interrupt
[4]	rw	1'h0	RIM	Receive FIFO Overrun Interrupt Mask 0 = ROR events generate an SSP interrupt 1 = ROR events do NOT generate an SSP interrupt
[3]	rw	1'h0	TIE	Transmit FIFO Interrupt Enable 0 = TXFIFO threshold-level-reached interrupt is disabled 1 = TXFIFO threshold-level-reached interrupt is enabled
[2]	rw	1'h0	RIE	Receive FIFO Interrupt Enable 0 = RXFIFO threshold-level-reached interrupt is disabled 1 = RXFIFO threshold-level-reached interrupt is enabled
[1]	rw	1'h0	TINTE	Receiver Time-out Interrupt Enable 0 = Receiver time-out interrupt is disabled 1 = Receiver time-out interrupt is enabled
[0]	rw	1'h0	PINTE	Peripheral Trailing Byte Interrupt Enable 0 = Peripheral trailing byte interrupt is disabled 1 = Peripheral trailing byte interrupt is enabled
0x0C			**TO**	SPI Time Out Register
[31:24]			RSVD	
[23:0]	r	24'h0	TIMEOUT	Timeout Value TIMEOUT value is the value (0 to 2<super 24>-1) that defines the time-out interval. The time-out interval is given by the equation shown in the TIMEOUT Interval Equation.
0x10			**STATUS**	Status Register
[31:24]			RSVD	
[23]	r	1'h0	OSS	Odd Sample Status 0 = RxFIFO entry has two samples 1 = RxFIFO entry has one sample Note that this bit needs to be looked at only when FIFO Packing is enabled (<FIFO Packing Enable> field in SSP FIFO Control Register is set). Otherwise, this bit is zero. When SSPx port is in Packed mode and the CPU is used instead of DMA to read the RxFIFO, the CPU should make sure that <Receive FIFO Not Empty> = 1 AND this field = 0 before it attempts to read the RxFIFO.

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表 7-2: SPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[22]	r	1'h0	TX_OSS	TX FIFO Odd Sample Status When SSPx port is in packed mode, the number of samples in the TX FIFO is: (<Transmit FIFO Level>*2 + this field), when <Transmit FIFO Not Full> = 1 32, when <Transmit FIFO Not Full> = 0. The TX FIFO cannot accept new data when <Transmit FIFO Not Full> = 1 and <Transmit FIFO Level> = 15 and this field = 1. (The TX FIFO has 31 samples). 0 = TxFIFO entry has an even number of samples 1 = TxFIFO entry has an odd number of samples Note that this bit needs to be read only when FIFO Packing is enabled (<FIFO Packing Enable> in the SSP FIFO Control Register is set). Otherwise, this bit is zero.
[21]	w1c	1'h0	BCE	Bit Count Error 0 = The SSPx port has not experienced a bit count error 1 = The SSPSFRMx signal was asserted when the bit counter was not zero
[20]	w1c	1'h0	ROR	Receive FIFO Overrun 0 = RXFIFO has not experienced an overrun 1 = Attempted data write to full RXFIFO, causes an interrupt request
[19]			RSVD	
[18:15]	r	4'h0	RFL	Receive FIFO Level This field is the number of entries minus one in RXFIFO. When the value 0x1F is read, the RXFIFO is either empty or full, and software should read the <Receive FIFO Not Empty> field.
[14]	r	1'h0	RNE	Receive FIFO Not Empty 0 = RXFIFO is empty 1 = RXFIFO is not empty
[13]	r	1'h0	RFS	Receive FIFO Service Request 0 = RXFIFO level is at or below RFT threshold (RFT) or SSPx port is disabled 1 = RXFIFO level exceeds RFT threshold (RFT), causes an interrupt request
[12]	w1c	1'h0	TUR	Transmit FIFO Underrun 0 = The TXFIFO has not experienced an underrun 1 = A read from the TXFIFO was attempted when the TXFIFO was empty, causes an interrupt if it is enabled (<Transmit FIFO Underrun Interrupt Mask> in the SSP INT EN Register is 0)
[11]			RSVD	
[10:7]	r	4'h0	TFL	Transmit FIFO Level This field is the number of entries in TXFIFO.When the value 0x0 is read, the TXFIFO is either empty or full, and software should read the <Transmit FIFO Not Full> field.
[6]	r	1'h0	TNF	Transmit FIFO Not Full 0 = TXFIFO is full 1 = TXFIFO is not full
[5]	r	1'h0	TFS	Transmit FIFO Service Request 0 = TX FIFO level exceeds the TFT threshold (TFT + 1) or SSPx port disabled 1 = TXFIFO level is at or below TFT threshold (TFT + 1), causes an interrupt request
[4]	w1c	1'h0	EOC	End Of Chain 0 = DMA has not signaled an end of chain condition 1 = DMA has signaled an end of chain condition
[3]	w1c	1'h0	TINT	Receiver Time-out Interrupt 0 = No receiver time-out is pending 1 = Receiver time-out pending, causes an interrupt request

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表 7-2: SPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[2]	w1c	1'h0	PINT	Peripheral Trailing Byte Interrupt 0 = No peripheral trailing byte interrupt is pending 1 = Peripheral trailing byte interrupt is pending
[1]	r	1'h0	CSS	Clock Synchronization Status 0 = The SSPx port is ready for slave clock operations 1 = The SSPx port is currently busy synchronizing slave mode signals
[0]	r	1'h0	BSY	SSP Busy 0 = SSPx port is idle or disabled 1 = SSPx port is currently transmitting or receiving framed data
0x14			**DATA**	SPI DATA Register
[31:0]	rw	32'h0	DATA	DATA This field is used for data to be written to the TXFIFO read from the RXFIFO.
0x18			**FRM_HDR_DATA**	Frame Header Register
[31:0]	rw	32'h0	HDR_DATA	frame header data, including cmd addr ect
0x1C			**TOP_CTRL2**	Top CTRL Register2
[31:16]	rw	16'h0	SSPRWOTCCM	It's just total ssp_sclk_gpio Cycles The value of this register defines the total number of ssp_sclk_gpio cycles when SSP works in master and RWOT mode. When the rwot_counter matches this value, SSP returns to IDLE state and does not output ssp_sclk_gpio anymore.
[15]			RSVD	
[14]	rw	1'b0	SELECT_GPIO_CLKI	use clki from as rx clock
[13]	rw	1'b0	INV_RX_CLK	invert rx clk for large io timing margin
[12]	rw	1'b0	FRM_MODE	frame mode 0: rx only after header 1: tx only after header
[11]	rw	1'b0	FRM_TRI_WIRE_EN	1: auto te switch between hdr and rx 0: 4 wire mode
[10:6]	rw	5'hf	FRM_HDR_LENGTH	frame header data length in bits:
[5]	w1c	1'b0	FRM_START	frame header data, including cmd addr ect
[4]	rw	1'h0	MASK_RWOT_LAST_SAMPLE	Mask last_sample_flag in RWOT Mode 1= Mask 0 = Unmask
[3]	rw	1'h0	CLR_RWOT_CYCLE	Clear SSP Internal rwot_counter This field clears the rwot_counter to 0. This field is self cleared by SSP after SSE = 1. 1 = Clear rwot_counter
[2]	rw	1'h0	SET_RWOT_CYCLE	Set RWOT Cycle This field is used to set the value of the SSP_RWOT_CCM register to the SSP internal rwot_counter. This field is self-cleared by SSP after SSE = 1. 1 = Set rwot_counter
[1]	rw	1'h0	CYCLE_RWOT_EN	Enable SSP RWOT Cycle Counter Mode 1 = Enable
[0]	rw	1'h0	RWOT	Receive Without Transmit 0 = Transmit/receive mode 1 = Receive without transmit mode
0x20			**RWOT_CVWRn**	SSP RWOT Counter Value Write for Red Request Register
[31:0]	rw	32'h0	SSPRWOTCVWR	SSPRWOTCVWR This register prevents the risk of instability on rwot_counter value reading, it's only valid after SSP has been enabled Write 0 = No effect Write 1 = Capture value of rwot_counter Read: Returns the captured value of rwot_counter

7.3 USART

HPSYS 有 3 个 USART(串口)。

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7.3.1 简介

通用异步收发器支持全双工模式，提供高达 6 Mbps 的波特率和多种可配置的数据格式，为与外部标准化设备通信提供了灵活而有效的数据交互手段。同时它还支持 DMA，实现多包收发。

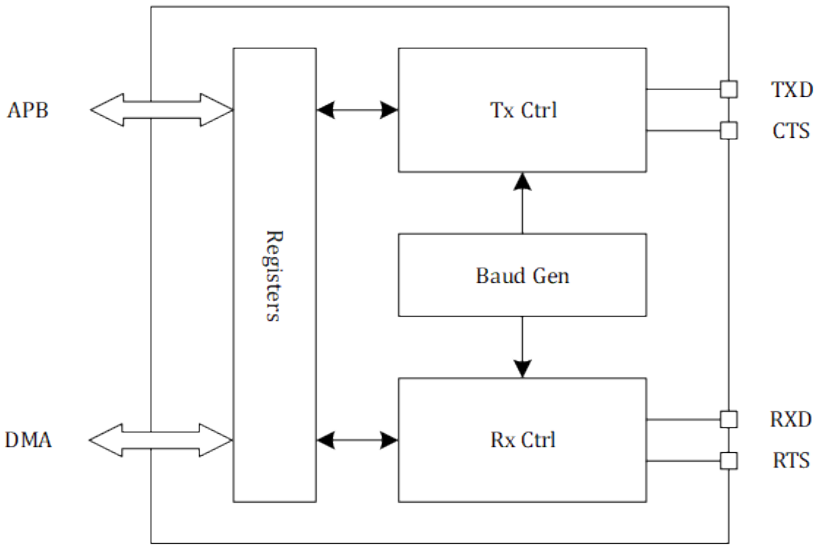


图 7-11: 通用异步收发器

7.3.2 主要特性

- 全双工异步通信
- 可配置 16 倍过采样或 8 倍过采样，选择时钟容忍度优先或者频率优先
- 灵活波特率配置，当输入时钟为 48 MHz 且过采样率为 16 时，波特率为 3 Mbps
- 可配置包长度（7/8/9 bits）
- 可配置停止位（1/2 bits）
- 硬件流控（CTS/RTS）
- DMA 多包发送和接收
- 接收奇偶校验和发送奇偶生成
- 接收和发送中断，以及其他错误中断

7.3.3 数据帧格式

起始位 低电平，固定 1 位。接收端在空闲态检测到 RXD 为低后进入起始位状态。

数据域 7、8 或 9 位，宽度由 CR1.M 选择。

数据域宽度为数据位与校验位合计的总位数：PCE = 0 时全部为数据位；PCE = 1 时，数据域的最后一位为校验位，实际数据位数为总位数减 1。

校验位 1 位，仅当 CR1.PCE = 1 时有效。CR1.PS = 0 为偶校验，PS = 1 为奇校验。发送端在移位前根据 TDR 内容预计算校验位（偶校验时数据位与校验位中 “1” 的个数为偶数）；接收端在数据域末位之后采样校验位，与本

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地计算值比较，不一致时置位 PE 标志。PCE=1 时，发送校验位按 TDR[8:0] 全部 9 位异或计算，写 TDR 时数据域宽度以上的位（含校验位位置）应写 0，否则校验结果受影响；接收端 RDR 中数据域宽度以上的位（含校验位）为移位填充值。

停止位 高电平，1 位或 2 位，由 CR2.STOP 选择（STOP[1] = 0 为 1 位，STOP[1] = 1 为 2 位；STOP[0] 不影响长度）。接收端在数据位与校验位（若使能）结束后，对第一个停止位的中心采样，采样值为低电平时置位 FE（帧错误）标志；配置 2 个停止位时，第二个停止位不做帧错误检查。发生 FE 时数据仍正常写入 RDR，FE 为粘滞标志，需向 ICR.FECF 写 1（W1C）清除，中断由 CR3.EIE 使能。

波特率

1. **时钟来源：** uclk（48 MHz）
2. **分频机制：** 12 位整数 + 4 位小数的分数分频（BRR[15:4] = 整数部分，BRR[3:0] = 小数部分（1/16 分辨率））

   OVER8（CR1 bit14）不改变 uclk_baud 的频率，只改变每个 UART 位占多少拍 uclk_baud：
   - over_mode=0（16 倍）：每数据位 = 16 拍 uclk_baud
   - over_mode=1（8 倍）：每数据位 = 8 拍 uclk_baud
3. **计算公式：**

$$\mathrm{DIV} = \frac{f_{\mathrm{uclk}}}{f_{\mathrm{baud}} \times \mathrm{over\_mode}}$$

配置步骤：

1. 按目标模式计算分频比
2. 整数部分写入 BRR[15:4]（INT），小数部分 = (DIV − INT) × 16（16 倍模式）四舍五入取 0–15 写入 BRR[3:0]（FRAC）

注：可以先配 BRR 再使能 UE。

7.3.4 收发流程

发送流程

1. TE=1 后，等待 ISR.TXE = 1（TDR 空）；
2. 写 TDR[8:0]（数据低位对齐，超出数据域的位写 0）。写入后 TDR 内容在起始位结束时（起始位与首个数据位的边界，帧开始后 1 个位周期）被锁存进移位寄存器，TXE 随即置 1。
3. 连续发送时，在 TXE 重新置 1 后写入下一字节；停止位结束时刻若 TDR 已有数据，自动背靠背发送，帧间无间隙；
4. 需确认整帧（含停止位）发完时，等待 ISR.TC = 1 或使能 TC 中断。

TX 冲刷：写 RQR.TXFRQ = 1，放弃 TDR 中尚未锁存的数据（TXE 置 1，该数据不再发送）；正在传输的当前帧完整发完，状态机在停止位结束后回到空闲态，TDR 寄存器内容不清零。

接收流程

1. RE=1 后接收状态机自动监测 RXD，收到完整帧时数据锁存入 RDR 并置 RXNE；
2. 看到 ISR.RXNE = 1 后读 RDR（低 9 位有效，数据低位对齐）；读 RDR 即清除 RXNE；

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3. 读 RDR 前检查 PE/FE/NE/ORE 标志判断本帧是否有错；出错帧的数据仍会锁存，软件可自行丢弃；
4. RDR 为单级缓冲：旧数据未读时新帧到达且 CR3.OVRDIS = 0 则置 ORE（新数据丢弃、RDR 保留旧值）；OVRDIS = 1 则新数据直接覆盖旧值且不置 ORE。及时读 RDR（或使能 DMA）是避免 ORE 的关键。

RX 冲刷：写 RQR.RXFRQ = 1，清除 RXNE，允许下一帧数据直接写入 RDR（等效于丢弃当前未读数据）。RDR 寄存器内容不清零，冲刷后读 RDR 仍返回旧值，仅因 RXNE=0 而无效。

7.3.5 中断

中断服务程序应先读 ISR 识别事件源，再处理并清除对应标志。注意：读 ISR 不清除标志，清除必须通过 ICR 写 1 或读/写数据寄存器。

中断源	使能位	ISR 标志位	清除方式	触发条件
接收数据	CR1.RXNEIE	RXNE	读 RDR 或 RQR.RXFRQ	RDR 有新数据
发送寄存器空	CR1.TXEIE	TXE	写 TDR	TDR 可写，可提示写下一数据
发送完成	CR1.TCIE	TC	ICR.TCCF	整帧（含停止位）发完
奇偶错误	CR1.PEIE	PE	ICR.PECF	校验位与本地计算不符
错误（帧/噪声/溢出）	CR3.EIE	FE / NE / ORE	ICR.FECF / NCF / ORECF	停止位为低 / 表决不一致 / RDR
CTS 变化	CR3.CTSE + CR3.CTSIE	CTSIF	ICR.CTSCF	CTS 电平变化（需 CTSE=1）
空闲线	CR1.IDLEIE	IDLE	ICR.IDLECF	收帧后线路空闲一个完整帧周期

7.3.6 硬件流控

CTS

- 使能：CR3.CTSE = 1。CTS 为高电平有效：对端把 CTS 拉高即请求本端暂停发送。
- 生效边界是帧边界：CTS 为高期间，状态机不启动新帧；正在发送的帧完整发完、不截断；TDR 中已写入的数据保留不丢失。
- CTS 恢复低电平后，下一帧在下一个采样边界立即启动；被推迟的数据不因等待而丢失。
- 需要感知 CTS 变化时同时置 CR3.CTSIE = 1，CTS 电平变化产生 CTSIF 中断（ICR.CTSCF 清除）。

RTS

- 使能：CR3.RTSE = 1 且 RE = 1；RTS 为低电平有效输出。
- 接收空闲时 RTS 为高（无效）；收帧进入数据域后，剩余待采数据位数等于 MISCR.RTSBIT（默认 2）的采样点时刻 RTS 拉低，通知发送方：本帧即将收完、接收缓冲即将占满，请暂缓发送。
- CPU 读出 RDR（或写 RQR.RXFRQ）后 RTS 恢复高电平。

使用流程

1. 配置波特率：写 BRR，此步可在 UE=1 之前完成；
2. 配置帧格式：CR1.M（数据位宽）、CR1.PCE/PS（校验）、CR2.STOP（停止位）、CR1.OVER8（过采样）；
3. 使能外设：CR1.UE = 1，uclk 域收发逻辑复位释放，TXD 恢复空闲高电平，接收状态机开始监测 RXD；
4. 使能发送：CR1.TE = 1；按需使能中断（CR1.TXEIE/TCIE）、DMA（CR3.DMAT）、CTS 流控（CR3.CTSE）；

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5. 使能接收：CR1.RE = 1；按需使能中断（CR1.RXNEIE/PEIE/IDLEIE、CR3.EIE）、DMA（CR3.DMAR）、RTS 流控（CR3.RTSE）；
6. 开始传输：写 TDR 开始发送；接收侧在中断服务中读 RDR。

关闭 USART 时置 CR1.UE = 0：uclk 域收发逻辑复位、收发停止，TXD 恢复高电平；BRR 等寄存器配置保留（分频器复位不受 UE 影响）。

7.3.7 USART 寄存器

USART1 的基地址是 0x50084000。

USART2 的基地址是 0x50085000。

USART3 的基地址是 0x50086000。

表 7-3: USART 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**CR1**	Control Register 1
[31:29]			RSVD	
[28:27]	rw	2'h2	M	Mode bit indicates the length of the packet, including data bits and parity. Stop bits not included. 0: 6 bits (e.g. 6 data bits + no parity bit) 1: 7 bits (e.g. 6 data bits + 1 parity bit) 2: 8 bits (e.g. 7 data bits + 1 parity bit, or 6 data bits + 2 parity bits) 3: 9 bits (e.g. 8 data bits + 1 parity bit, or 7 data bits + 2 parity bits)
[26]			RSVD	
[25]			RSVD	
[24:20]			RSVD	
[19:15]			RSVD	
[14]	rw	1'h0	OVER8	Oversampling mode 0: Oversampling by 16 1: Oversampling by 8
[13]			RSVD	
[12]			RSVD	
[11]			RSVD	
[10]	rw	1'h0	PCE	Parity check enable. If enabled, parity bit is inserted at the MSB position 0: parity check disabled 1: parity check enabled
[9]	rw	1'h0	PS	Parity select 0: even parity 1: odd parity
[8]	rw	1'h0	PEIE	Parity error interrupt enable 0: interrupt disabled 1: interrupt is generated whenever PE=1 in the ISR register
[7]	rw	1'h0	TXEIE	Tx empty interrupt enable 0: interrupt disabled 1: interrupt is generated whenver TXE=1 in the ISR register
[6]	rw	1'h0	TCIE	Transfer compelete interrupt enable 0: interrupt disabled 1: interrupt is generated whenever TC=1 in the ISR register

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表 7-3: USART 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[5]	rw	1'h0	RXNEIE	Rx not empty interrupt enable 0: interrupt disabled 1: interrupt is generated whenever RXNE=1 in the ISR register
[4]	rw	1'h0	IDLEIE	Idle line interrupt enable 0: interrupt disabled 1: interrupt is generated whenever IDLE=1 in the ISR register
[3]	rw	1'h0	TE	Transmitter enable 0: transmitter is disabled 1: transmitter is enabled
[2]	rw	1'h0	RE	Receiver enable 0: receiver is disabled 1: receiver is enabled
[1]			RSVD	
[0]	rw	1'h0	UE	USART enable 0: disabled 1: enabled
0x04			**CR2**	Control Register 2
[31:24]			RSVD	
[23]			RSVD	
[22:21]			RSVD	
[20]			RSVD	
[19]			RSVD	
[18]			RSVD	
[17]			RSVD	
[16]			RSVD	
[15]			RSVD	
[14]			RSVD	
[13:12]	rw	2'h0	STOP	Stop bits 0/1: 1 stop bit 2/3: 2 stop bits
[11]			RSVD	
[10]			RSVD	
[9]			RSVD	
[8]			RSVD	
[7]			RSVD	
[6]			RSVD	
[5]			RSVD	
[4]			RSVD	
[3:0]			RSVD	
0x08			**CR3**	Control Register 3
[31:25]			RSVD	
[24]			RSVD	
[23]			RSVD	
[22]			RSVD	
[21:20]			RSVD	
[19:17]			RSVD	
[16]			RSVD	
[15]			RSVD	

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表 7-3: USART 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[14]			RSVD	
[13]			RSVD	
[12]	rw	1'h0	OVRDIS	Overrun disable 0: overrun error flag (ORE) will be set if new data received but previous data not read. New data will not overwrite the content in RDR register. 1: overrun disabled. If new data is received before previous data is read, the new data will overwrite the content in RDR register and ORE flag remains unset.
[11]	rw	1'h0	ONEBIT	One bit sampling mode 0: 3-bit sampling mode, the sampling value is determined by the voted result out of 3 bits 1: 1-bit sampling mode
[10]	rw	1'h0	CTSIE	CTS interrupt enable 0: interrupt disabled 1: interrupt is generated whenever CTSIF=1 in the ISR register
[9]	rw	1'h0	CTSE	CTS enable 0: CTS hardware flow control disabled 1: CTS hardware flow control enabled, data is transmitted only when CTS input is asserted low
[8]	rw	1'h0	RTSE	RTS enable 0: RTS hardware flow control disabled 1: RTS hardware flow control enabled, RTS output is asserted low when new data can be received
[7]	rw	1'h0	DMAT	Transmitter DMA enable 0: DMA mode disabled for transmission 1: DMA mode enabled for transmission
[6]	rw	1'h0	DMAR	Receiver DMA enable 0: DMA mode disabled for reception 1: DMA mode enabled for reception
[5]			RSVD	
[4]			RSVD	
[3]			RSVD	
[2]			RSVD	
[1]			RSVD	
[0]	rw	1'h0	EIE	Error interrupt enable 0: interrupt disabled 1: interrupt is generated whenever FE=1 or ORE=1 or NF=1 in the ISR register
0x0C			**BRR**	Baud Rate Register
[31:16]			RSVD	
[15:4]	rw	12'h3	INT	Integer part of baud rate prescaler If OVER8 = 0, Baud Rate = 48000000 / (INT + FRAC/16) / 16 If OVER8 = 1, Baud Rate = 48000000 / (INT + FRAC/16) / 8 For example: OVER=0, INT=3, FRAC=0, Baud Rate = 48000000/(3+0)/16 = 1Mbps OVER=0, INT=3, FRAC=4, Baud Rate = 48000000/(3+4/16)/16 = 923077 = 921600 + 1.6$10 extperthousand$ OVER=1, INT=52, FRAC=1, Baud Rate = 48000000/(52+1/16)/8 = 115246 = 115200 + 0.4$10 extperthousand$
[3:0]	rw	4'h0	FRAC	Fractional part of baud rate prescaler
0x18			**RQR**	Request Register

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表 7-3: USART 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:5]			RSVD	
[4]	w	1'h0	TXFRQ	Tx data flush request Reserved-Do not modify
[3]	w	1'h0	RXFRQ	Rx data flush request. Write 1 to clear the RXNE flag and discard the current data in RDR
[2]			RSVD	
[1]			RSVD	
[0]			RSVD	
0x1C			**ISR**	Interrupt and Status Register
[31:26]			RSVD	
[25]			RSVD	
[24:23]			RSVD	
[22]			RSVD	
[21]			RSVD	
[20]			RSVD	
[19]			RSVD	
[18]			RSVD	
[17]			RSVD	
[16]			RSVD	
[15]			RSVD	
[14]			RSVD	
[13]			RSVD	
[12]			RSVD	
[11]			RSVD	
[10]	r	1'h0	CTS	CTS input. Read this bit to get the raw status of the CTS line.
[9]	r	1'h0	CTSIF	CTS interrupt flag. This bit is set by hardware whenever CTS input toggles. 0: no change on the CTS line 1: there is a change on the CTS line
[8]			RSVD	
[7]	r	1'h1	TXE	Tx data empty 0: data is ready in TDR 1: data is already transferred to shift register, i.e. transmission is in progress or complete
[6]	r	1'h1	TC	transmission complete. This bit is set by hardware if the transmission is complete 0: transmission is not complete 1: transmission is complete
[5]	r	1'h0	RXNE	Rx data not empty. This bit is set by hardware when the received data is transferred into RDR register. 0: data is not received 1: data is ready in RDR to be read
[4]	r	1'h0	IDLE	Idle line detected 0: no idle line is detected 1: idle line is detected
[3]	r	1'h0	ORE	Overrun error. When new data is received but Rx buffer is not empty (i.e. previous data is not read yet), ORE is asserted and current RDR content is not lost. This feature can be disabled by set CR3_OVRDIS to 1. 0: no overrun error 1: overrun error is detected

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表 7-3: USART 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[2]	r	1'h0	NF	Noise flag. Noise means the samping values in the 3-bit sampling mode are not the same. 0: no noise is detected 1: noise is detected
[1]	r	1'h0	FE	Framing error. This bit is set by hardware when stop bit is not correctly received 0: no framing error is detected 1: framing error is detected
[0]	r	1'h0	PE	Parity error. This bit is set when a parity error is detected in the received packet. 0: no parity error 1: parity error detected
0x20			**ICR**	Interrupt flag Clear Register
[31:21]			RSVD	
[20]			RSVD	
[19:18]			RSVD	
[17]			RSVD	
[16:13]			RSVD	
[12]			RSVD	
[11]			RSVD	
[10]			RSVD	
[9]	w1c	1'h0	CTSCF	CTS clear flag. Writing 1 to this bit clears the CTSIF flag in the ISR register.
[8]			RSVD	
[7]			RSVD	
[6]	w1c	1'h0	TCCF	Transmission complete clear flag. Writing 1 to this bit clears the TC flag in the ISR register.
[5]			RSVD	
[4]	w1c	1'h0	IDLECF	Idle line detected clear flag. Writing 1 to this bit clears the IDLECF flag in the ISR register.
[3]	w1c	1'h0	ORECF	Overrun error clear flag. Writing 1 to this bit clears the ORE flag in the ISR register.
[2]	w1c	1'h0	NCF	Noise detected clear flag. Writing 1 to this bit clears the NF flag in the ISR register.
[1]	w1c	1'h0	FECF	Framing error clear flag. Writing 1 to this bit clears the FE flag in the ISR register.
[0]	w1c	1'h0	PECF	Parity error clear flag. Wriring 1 to this bit clears the PE flag in the ISR register.
0x24			**RDR**	Receive Data Register
[31:9]			RSVD	
[8:0]	r	9'h0	RDR	Received data
0x28			**TDR**	Transmit Data Register
[31:9]			RSVD	
[8:0]	rw	9'h0	TDR	Transmit data
0x2C			**MISCR**	Miscellaneous Register
[31]	rw	1'h0	AUTOCAL	
[30:8]			RSVD	
[7:4]	rw	4'h2	RTSBIT	assert RTS ahead of the frame completion (in number of bits) Reserved-Do not modify
[3:0]	rw	4'h6	SMPLINI	initial sample count, count down from this value to zero to reach the middle of the start bit in Rx Reserved-Do not modify
0x30			**DRDR**	Debug Receive Data Register
[31:0]	r	32'h0	DATA	

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表 7-3: USART 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x34			**DTDR**	Debug Receive Data Register
[31:0]	rw	32'h0	DATA	
0x38			**EXR**	Mutual Exclusive Register
[31:5]			RSVD	
[4]	r	1'b0	ID	
[3:1]			RSVD	
[0]	rw	1'h1	BUSY	

7.4 CAN

HPSYS 有 2 个 CAN。

CAN(Controller Area Network) 兼容 CAN 协议 2.0b，不支持 CAN FD。CAN 的基础传输速率可配置，内部包含接收 FIFO 与发送 FIFO，支持多帧自动收发、自动重传、抢占发送等功能。CAN 包含灵活可配置的接收 ID 自动过滤器，仅在接收 FIFO 中保存过滤后的帧。发现总线和收发异常时，CAN 具有完备的错误通知机制。

CAN 主要特性:

- 兼容 CAN 2.0b，不支持 CAN FD
- 可配置数据率至 1Mbps
- 支持基础帧和扩展帧
- 帧数据长度可达 8byte
- 接收 FIFO 深度 7，发送 FIFO 深度 7+1
- 16 个灵活配置的 ID 过滤器
- 支持帧抢占发送
- 错误检测与通知机制

7.5 USB

本芯片集成了一路全速（FS）USB2.0 Host/Device 接口，符合 USB 2.0 的协议规范，具有如下功能：

- 软件可配置的端点设置，支持挂起/恢复
- 支持动态 FIFO 大小
- 支持会话请求协议和主机协商协议
- 支持全速以及慢速模式
- 片内集成 USB2.0 FS PHY
- 拥有 ep0~ep7 8 个通道，其中 ep2~ep4 只支持 rx(即 host 只支持 IN，device 只支持 OUT)，ep2~ep4 只支持 tx(即 host 只支持 OUT，device 只支持 IN)

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8 模拟外设

8.1 GPADC

8.1.1 简介

GPADC 是一个 12bit 精度 SARADC，支持 0-3.3V 输入电压，输出为 12bit 数据。输入电压可为单端或差分，输出数据可通过 APB 总线或 DMA 接口读取。

8.1.2 主要特性

- 支持 3.3V AVDD
- 输入电压范围：0~3.3V，12Bit 分辨率
- 支持单端输入和双端输入
- 支持 7 路单端模拟输入和 1 路专用电池电压测量输入或 3 对差分模拟输入
- 支持单次测量模式和循环测量模式
- 每次测量可以划分为 8 个时隙，各时隙可以单独配置模拟输入通道
- 支持软件（写寄存器）和硬件（如计时器）触发方式
- 支持 DMA 通道
- 采样频率可配，最高采样频率 4MHz
- 转换完成后产生中断

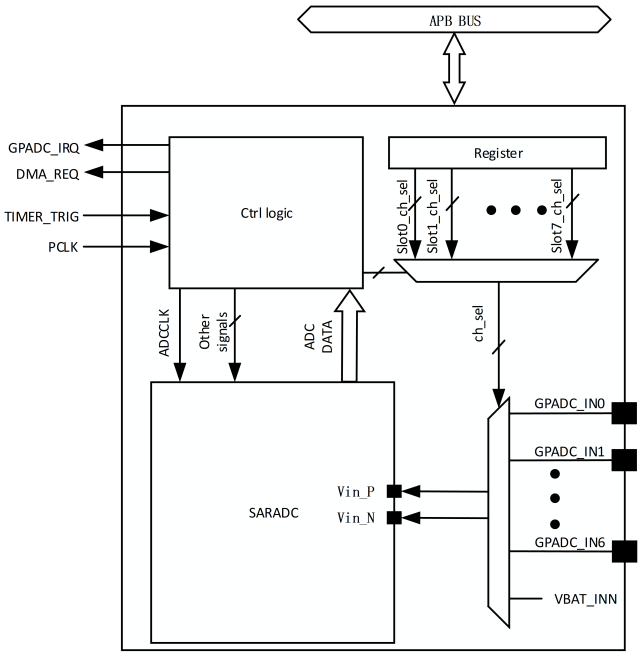


图 8-1: GPADC 框图

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8.1.3 功能描述

8.1.3.1 GPADC 时钟产生

GPADC 时钟由 HPSYS PCLK 分频产生，通过配置 ADC_CTRL_REG 的 DATA_SAMP_DLY 和 ADC_CTRL_REG2 中的 CONV_WIDTH 和 SAMP_WIDTH 设置 ADCCLK 频率，计算公式为：

$$f_{ADCCLK} = f_{PCLK}/(DATA\_SAMP\_DLY + CONV\_WIDTH + SAMP\_WIDTH + 2)$$

因为 ADCCLK 由 PCLK 分频产生，设置 ADCCLK 频率时需要注意确认 PCLK 频率。

8.1.3.2 时隙配置

每一轮 GPADC 采样，共有 8 个时隙按顺序依次工作，通过设置 ADC_SLOT*_REG 中的 SLOT_EN 每个时隙可单独使能或禁用；通过设置 ADC_SLOT*_REG 中的 PCHNL_SEL 和 NCHNL_SEL，可独立配置各时隙的输入通道。

8.1.3.3 单端/差分模式

将寄存器 ADC_CFG_REG 中的 ANAU_GPADC_SE 置为 1，则 GPADC 为单端输入模式，只需设置各时隙对应配置寄存器中的 PCHNL_SEL 来选择输入通道。

将寄存器 ADC_CFG_REG 中的 ANAU_GPADC_SE 置为 0，则 GPADC 为差分输入模式，设置各时隙对应配置寄存器中的 PCHNL_SEL 和 NCHNL_SEL 来选择 Vin_P 和 Vin_N 对应的输入通道。

8.1.3.4 输入通道选择

GPADC 共有 8 路输入通道，8 路输入通道中，第 0-6 路通过 PAD 连到外部，第 7 路连接到内部节点测电池电压。

通过设置 ADC_SLOT*_REG 中的 PCHNL_SEL 和 NCHNL_SEL，可配置各时隙所要采样的输入通道。

如果为单端模式，只需设置 PCHNL_SEL 来选择输入通道。

8.1.3.5 采样模式

若 ADC_CTRL_REG 中的 ADC_OP_MODE 置 0，则 GPADC 处于单次采样模式，该模式下每次启动 GPADC 后，GPADC 将按照各时隙配置完成一轮采样，然后回到等待触发状态。

若 ADC_CTRL_REG 中的 ADC_OP_MODE 置 1，则 GPADC 处于连续采样模式，该模式下每次启动 GPADC 后，GPADC 将循环按照各时隙配置循环进行采样。将 ADC_CTRL_REG 的 ADC_STOP 置 1 可使 GPADC 回到等待触发状态。

8.1.3.6 启动 GPADC

- 写寄存器启动
  将寄存器 ADC_CTRL_REG 中的 ADC_START 置 1，可以启动 GPADC。
  触发 GPADC 后，如果 GPADC 处于单次采样模式，则完成一轮采样后，回到等待触发状态。如果 GPADC 处于连续采样模式，则需将 ADC_CTRL_REG 的 ADC_STOP 置 1 使 GPADC 回到等待触发状态。

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- Timer 触发

  GPADC 支持 TIMER 触发，使能 TIMER 触发功能需要将 ADC_CTRL_REG 中的 TIMER_TRIG_EN 置为 1。共有 8 个触发源，可通过寄存器 ADC_CTRL_REG 中的 TIMER_TRIG_SRC_SEL 选择触发源。对应关系如下表：

TIMER_TRIG_SRC_SEL	TRIG_SRC
0	GPTIM1 TRGO
1	GPTIM2 TRGO
2	APTIM1 TRGO
3	BTIM1 TRGO
4	BTIM2 TRGO
5	GPTIM1 CH0 输出
6	GPTIM1 CH1 输出
7	GPTIM1 CH2 输出

  触发 GPADC 后，如果 GPADC 处于单次采样模式，则完成一轮采样后，回到等待触发状态。如果 GPADC 处于连续采样模式，则需将 ADC_CTRL_REG 的 ADC_STOP 置 1 使 GPADC 回到等待触发状态。

8.1.3.7 数据访问

GPADC 转换得到的数据可以通过以下两种方式访问：

- 寄存器读取

  软件可以通过读寄存器直接读取 GPADC 转换结果。各时隙对应数据存放在寄存器 ADC_RDATA* 中，寄存器和各时隙数据的对应关系如下表：

ADC_RDATA0[31:0]	
SLOT1_RDATA	SLOT0_RDATA
ADC_RDATA1[31:0]	
SLOT3_RDATA	SLOT2_RDATA
ADC_RDATA2[31:0]	
SLOT5_RDATA	SLOT4_RDATA
ADC_RDATA3[31:0]	
SLOT7_RDATA	SLOT6_RDATA

  在寄存器 ADC_RDATA* 中，各时隙对应的 GPADC 输出数据的 LSB 向右对齐到寄存器的 0 比特或者 16 比特。以 ADC_RDATA0 为例说明时隙数据在寄存器里的对齐方式，对齐方式如下表：

SLOT0_RDATA（ADC_RDATA0[31:16]）																SLOT0_RDATA（ADC_RDATA0[15:0]）															
0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

- DMA 模式

  通过 HPSYS 中的 DMAC1 读取 GPADC 的转换结果。使用流程为：

  将寄存器 ADC_CTRL_REG 的 DMA_EN 置 1。

  将 DMA 的源地址设置为 0x5007034。ADC 数据在该地址的对齐方式是：

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Bit[15：0]															
0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

其他 DMA 设置参考 DMAC 章节。

8.1.3.8 通知机制

GPADC 在结束采样转换的时会产生中断，上报给 CPU。

该中断可以通过给寄存器 GPADC_IRQ 的 GPADC_IMR 置 1 来屏蔽。

该中断可以通过给寄存器 GPADC_IRQ 的 GPADC_ICR 置 1 来清中断。

8.1.3.9 系统设置依赖关系

GPADC 的时钟由 HPSYS PCLK 分频产生，设置频率时需明确 HPSYS PCLK 频率。

GPADC 可外接的 7 路通道，通过 PAD 和外部被测电压相连。使用时，要做相应的 PINMUX 设置。GPADC channel 和 PAD 的对应关系为：

GPADC channel	PAD	CH_SEL_value
GPADC_CH0	PAD_PA28	0
GPADC_CH1	PAD_PA29	1
GPADC_CH2	PAD_PA30	2
GPADC_CH3	PAD_PA31	3
GPADC_CH4	PAD_PA32	4
GPADC_CH5	PAD_PA33	5
GPADC_CH6	PAD_PA34	6

在 CH_SEL 值为 7 并将 HPSYS_CFG 模块中 ANAU_CR 寄存器的 EN_VBAT_MON 置 1 时，选择内部测量电池电压的采样点，采样点电压由电池电压经过内部分压电阻得到，电阻的分压比为 0.5，分压比有出厂校准。

GPADC 工作时候需要使能 ANAU 中的 bandgap，将 HPSYS_CFG 模块中 ANAU_CR 寄存器的 EN_BG 置 1 以打开该 bandgap。

8.1.3.10 配置启动流程

使用 GPADC 一般经过以下流程：

- 配置 PINMUX。
- 配置 GPADC 时钟频率，输入通路选择等信息。
- 将 HPSYS_CFG 寄存器 ANAU_CR 中的 EN_BG 置 1 使能 Bandgap。
- 将寄存器 ADC_CFG_REG1 中的 ANAU_GPADC_LDOREF_EN 置 1 使能给 GPADC 提供参考电压的 LDO。
- 将寄存器 ADC_CTRL_REG 中的 FRC_EN_ADC 置 1，使能 GPADC 模块。
- 触发 GPADC，开始采样，读取数据。
- 采样完成后将寄存器 ADC_CTRL_REG 中的 FRC_EN_ADC 置 0，关闭 GPADC 模块。如果是连续采样模式还需要先将寄存器 ADC_CTRL_REG 中的 ADC_STOP 先置 1 再置 0 来中断采样流程。
- 将寄存器 ADC_CFG_REG1 中的 ANAU_GPADC_LDOREF_EN 置 0 关闭给 GPADC 提供参考电压的 LDO。
- Bandgap 与 TSEN 模块共用，推荐不关闭。

过程需要满足一些电路稳定时间。

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- Pinmux 配置后，PAD 连到输入通道的电压需要一定的稳定时间。
- 打开 bandgap 后，再打开提供参考电压的 LDO, LDO 需要 200us 稳定时间。
- 使能 GPADC 后需要至少 200us 稳定时间。
- 最后通过写寄存器触发或 Timer 触发启动 GPADC。

8.1.4 GPADC 寄存器

GPADC 的基地址是 0x50087000。

表 8-1: GPADC 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**ADC_CFG_REG1**	ADC Analog Config Register 1
[31:30]			RSVD	
[29:25]	rw	5'h16	ANAU_GPADC_CMM	Tune CDAC CM voltage 375mV range (increasing) / 25mV step, 8: for 0.5V Vcm,in
[24:22]	rw	3'h3	ANAU_GPADC_CMPCL	Tune ADC comparator CL= 3: 40f, range: 10fF (0) ~ 80fF (7) / 10fF step
[21:20]	rw	2'h2	ANAU_GPADC_VSP	Set comparator input CM in sampling phase, 0.539V (0) / 0.578V (1) / 0.642V (2) / 0.784V (3)
[19]	rw	1'h0	ANAU_GPADC_LDOREF_EN	Enable LDORF for ADC VREF
[18:15]	rw	4'hA	ANAU_GPADC_LDOVREF_SEL	Set reference voltage for LDOREF, range = 0.35V(0) ~ 0.65V(15), step = 20mV
[14:12]	rw	3'h1	ANAU_GPADC_SEL_PCH	Select P-side input channel for GPADC, 0 for channel 0, 7 for channel 7, effective when force on
[11:9]	rw	3'h0	ANAU_GPADC_SEL_NCH	Select N-side input channel for GPADC, 0 for channel 0, 7 for channel 7, effective when force on
[8]	rw	1'h0	ANAU_GPADC_MUTE	Short GPADC P & N input to CMREF, i.e., VREF/2
[7]	rw	1'h0	ANAU_GPADC_SE	Set GPADC in single-ended mode, signal range at P-input: 0 ~ VREF
[6]	rw	1'h0	ANAU_GPADC_EN_V18	
[5:3]	rw	3'h2	ANAU_GPADC_CL_DLY	
[2]	rw	1'h0	ANAU_GPADC_P_INT_EN	
[1]			RSVD	
[0]	rw	1'h0	ANAU_GPADC_CMREF_FAST_EN	
0x04			**ADC_Slot0_REG**	ADC Slot0 Config Register
[31:14]			RSVD	
[13:11]	rw	3'h1	NCHNL_SEL	
[10:8]	rw	3'h0	PCHNL_SEL	
[7:1]			RSVD	
[0]	rw	1'h1	SLOT_EN	
0x08			**ADC_Slot1_REG**	ADC Slot1 Config Register
[31:14]			RSVD	
[13:11]	rw	3'h1	NCHNL_SEL	
[10:8]	rw	3'h0	PCHNL_SEL	
[7:1]			RSVD	
[0]	rw	1'h1	SLOT_EN	
0x0C			**ADC_Slot2_REG**	ADC Slot2 Config Register
[31:14]			RSVD	
[13:11]	rw	3'h1	NCHNL_SEL	
[10:8]	rw	3'h0	PCHNL_SEL	
[7:1]			RSVD	

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表 8-1: GPADC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[0]	rw	1'h1	SLOT_EN	
0x10			**ADC_Slot3_REG**	ADC Slot3 Config Register
[31:14]			RSVD	
[13:11]	rw	3'h1	NCHNL_SEL	
[10:8]	rw	3'h0	PCHNL_SEL	
[7:1]			RSVD	
[0]	rw	1'h1	SLOT_EN	
0x14			**ADC_Slot4_REG**	ADC Slot4 Config Register
[31:14]			RSVD	
[13:11]	rw	3'h1	NCHNL_SEL	
[10:8]	rw	3'h0	PCHNL_SEL	
[7:1]			RSVD	
[0]	rw	1'h1	SLOT_EN	
0x18			**ADC_Slot5_REG**	ADC Slot5 Config Register
[31:14]			RSVD	
[13:11]	rw	3'h1	NCHNL_SEL	
[10:8]	rw	3'h0	PCHNL_SEL	
[7:1]			RSVD	
[0]	rw	1'h1	SLOT_EN	
0x1C			**ADC_Slot6_REG**	ADC Slot6 Config Register
[31:14]			RSVD	
[13:11]	rw	3'h1	NCHNL_SEL	
[10:8]	rw	3'h0	PCHNL_SEL	
[7:1]			RSVD	
[0]	rw	1'h1	SLOT_EN	
0x20			**ADC_Slot7_REG**	ADC Slot7 Config Register
[31:14]			RSVD	
[13:11]	rw	3'h1	NCHNL_SEL	
[10:8]	rw	3'h0	PCHNL_SEL	
[7:1]			RSVD	
[0]	rw	1'h1	SLOT_EN	
0x24			**ADC_RDATA0**	ADC Read Data0
[31:28]			RSVD	
[27:16]	r	12'h0	SLOT1_RDATA	
[15:12]			RSVD	
[11:0]	r	12'h0	SLOT0_RDATA	
0x28			**ADC_RDATA1**	ADC Read Data1
[31:28]			RSVD	
[27:16]	r	12'h0	SLOT3_RDATA	
[15:12]			RSVD	
[11:0]	r	12'h0	SLOT2_RDATA	
0x2C			**ADC_RDATA2**	ADC Read Data2
[31:28]			RSVD	
[27:16]	r	12'h0	SLOT5_RDATA	
[15:12]			RSVD	
[11:0]	r	12'h0	SLOT4_RDATA	
0x30			**ADC_RDATA3**	ADC Read Data3
[31:28]			RSVD	

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表 8-1: GPADC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[27:16]	r	12'h0	SLOT7_RDATA	
[15:12]			RSVD	
[11:0]	r	12'h0	SLOT6_RDATA	
0x34			**ADC_DMA_RDATA**	ADC Read Data For DMA
[31:29]			RSVD	
[28:16]	r	13'h0	DMA_RDATA_RAW	
[15:13]			RSVD	
[12:0]	r	13'h0	DMA_RDATA	
0x38			**ADC_CTRL_REG**	ADC Control Register
[31:21]			RSVD	
[20:17]	rw	4'h4	DATA_SAMP_DLY	
[16]	rw	1'b0	DMA_DATA_SEL	0: combined data 1: raw data
[15]	rw	1'b0	TIMER_TRIG_TYP	0: pulse no edge detect needed 1: level,need edge detect
[14:12]	rw	3'h0	TIMER_TRIG_SRC_SEL	Timer trigger source select
[11]	rw	1'b0	FRC_EN_ADC	Enable GPADC core
[10]	rw	1'b0	CHNL_SEL_FRC_EN	Enable input channel setting in ADC_CFG_REG1
[9]	rw	1'b1	TIMER_TRIG_EN	Enable timer trigger function
[8]			RSVD	
[7]	rw	1'b1	DMA_EN	Enable DMA interface
[6:3]	rw	4'h6	INIT_TIME	GPADC will wait INIT_TIME ADCCLK cycles to start sample/conversion after being trigged
[2]	rw	1'b0	ADC_STOP	Write 1 to stop GPADC in continuous mode(need write 0 to clear)
[1]	w1s	1'b0	ADC_START	Write 1 to start GPADC,(don't need clear)
[0]	rw	1'b0	ADC_OP_MODE	0: single conversion mode 1: continuous conversion mode
0x3C			**ADC_CTRL_REG2**	ADC Control Register2
[31:24]	rw	8'h80	CONV_WIDTH	
[23:0]	rw	24'h8000	SAMP_WIDTH	
0x40			**GPADC_STATUS**	GPADC Status Register
[31:12]			RSVD	
[11:9]	r	3'h0	CUR_SLOT	
[8:1]	r	8'h0	SLOT_DONE	
[0]	r	1'h0	ADC_DONE	
0x44			**GPADC_IRQ**	GPADC IRQ Register
[31:4]			RSVD	
[3]	r	1'b0	GPADC_ISR	
[2]	r	1'b0	GPADC_IRSR	
[1]	rw	1'b0	GPADC_IMR	
[0]	w1s	1'b0	GPADC_ICR	

8.2 TSEN

8.2.1 简介

TSEN 通过采样内部温敏电阻的电压将温度转换为数字编码，帮助系统实时监控芯片温度。

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8.2.2 主要特性

- 分辨率为 0.2°C
- 支持温度范围为-40°C 到 125°C
- 主持轮询或中断方式读数

8.2.3 功能描述

8.2.3.1 时钟信号

TSEN 的工作时钟由 LPSYS 的 PCLK 分频而来。分频比由寄存器 TSEN_CTRL_REG 中的 ANAU_TSEN_CLK_DIV 来设置。频率计算关系为:

$$ftsen = fpclk/ANAU\_TSEN\_CLK\_DIV$$

8.2.3.2 读数流程

转换结果从寄存器 TSEN_RDATA 读取, 读取后的结果通过如下公式转换为温度：

$$Temp = (Dec(TSEN_RDATA) + 3000)/10100 * 749.2916 - 277.5391$$

通过轮询读数的流程：

启动 TSEN 后，轮询寄存器 TSEN_IRQ 中的 TSEN_IRSR，当 TSEN_IRSR 值为 1 时，标志温度数据已转换完成，。读数后将寄存器 TSEN_IRQ 中的 TSEN_ICR 置 1, 将 TSEN_IRSR 清零。

通过中断读数的流程：

使能 TSEN 中断，并将寄存器 TSEN_IRQ 中的 TSEN_IMR 置 0，启动 TSEN，转换完成后会给 CPU 发出 TSEN_IRQ 中断。处理中断, 将寄存器 TSEN_IRQ 中的 TSEN_ICR 置 1 清中断，读数。

8.2.3.3 使用过程

TSEN 的工作需要按照以下流程。

1. 根据 PCLK 频率配置分频比，TSEN 的时钟频率应为 1MHz 或 2MHz。
2. 将 HPSYS_CFG 寄存器 ANAU_CR 中的 EN_BG 置 1，打开 Bandgap。
3. 将寄存器 TSEN_CTRL_REG 中的 ANAU_TSEN_EN 置 1，使能 TSEN 的时钟。
4. 将寄存器 TSEN_CTRL_REG 中的 ANAU_TSEN_PU 置 1，ANAU_TSEN_RUN 置 0。
5. 将寄存器 TSEN_CTRL_REG 中的 ANAU_TSEN_RSTB 先置 0 再置 1，低电平至少 20us。
6. 将寄存器 TSEN_CTRL_REG 中的 ANAU_TSEN_RUN 置 1，通过轮询或中断方式读取结果。也可以等待 3ms 绝对时间后读数。
7. 关闭 TSEN：将寄存器 TSEN_CTRL_REG 中的 ANAU_TSEN_RUN/ANAU_TSEN_PU/ANAU_TSEN_EN 置 0，ANAU_TSEN_RSTB 置 1。
8. Bandgap 与 GPADC 共用，推荐不关闭，如需关闭需注意不干扰 GPADC 的工作。

8.2.4 TSEN 寄存器

TSEN 的基地址是 0x50089000。

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表 8-2: TSEN 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**TSEN_CTRL_REG**	TSEN Analog Control Register
[31:18]			RSVD	
[17:12]	rw	6'h30	ANAU_TSEN_CLK_DIV	gen tsen clk by divide hclk by anau_tsen_clk_div
[11]	rw	1'h0	ANAU_TSEN_EN	Enable tsen digital module
[10]	r	1'h0	ANAU_TSEN_RDY	tsen ready
[9]	rw	1'h0	ANAU_TSEN_SER_PAR_SEL	serial-parallel output selection
[8]	rw	1'b0	ANAU_TSEN_SGN_EN	signature-mode enable
[7:6]	rw	2'h1	ANAU_TSEN_FCK_SEL	select internal clock frequency
[5:3]	rw	3'h1	ANAU_TSEN_IG_VBE	bias current selection to tune vba
[2]	rw	1'h0	ANAU_TSEN_RUN	enable tsen run
[1]	rw	1'h1	ANAU_TSEN_RSTB	resetb for tsen
[0]	rw	1'h0	ANAU_TSEN_PU	power up tsen
0x04			**TSEN_RDATA**	Tsen Read Data
[31:12]			RSVD	
[11:0]	r	12'h0	TSEN_RDATA	
0x08			**TSEN_IRQ**	Tsen IRQ Register
[31:4]			RSVD	
[3]	r	1'b0	TSEN_ISR	
[2]	r	1'b0	TSEN_IRSR	
[1]	rw	1'b0	TSEN_IMR	
[0]	w1s	1'b0	TSEN_ICR	

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9 定时器

9.1 ATIM

HPSYS 有 2 个 ATIM，工作时钟是 pclk_hpsys，应注意在系统动态调节频率时计数可能受到影响。

9.1.1 简介

ATIM (Advanced Timer) 基于一个 32 比特计数器，可实现计时、测量输入信号的脉冲长度 (输入捕获) 或者产生输出波形 (输出比较和 PWM) 等功能。ATIM 支持 6 路带死区保护的 PWM 互补输出，支持多路 PWM 同时换相，并有 2 路刹车输入可快速将输出切换至安全状态。计数器本身可以进行递增、递减或者递增/递减计数，计数时钟可选系统 PCLK、IO 输入信号或级联输入信号，并可进行 1~65536 倍的预分频。ATIM 共有 6 个通道，可以分别独立配置为输入捕获或输出模式。计数、输入捕获和输出比较的结果可以产生中断、DMA 请求或 PTC 事件。ATIM 包含主从模式接口，可以进行多级级联，实现多级计数或同步触发等功能。

9.1.2 主要特性

- 32 位递增、递减、递增/递减自动重装载计数器
- 16 位可编程 (可以实时修改) 预分频器，计数器时钟频率的分频系数为 1~65536 之间的任意数值
- 16 位可配置重复计数
- 支持单笔计数模式 (OPM)，当重复计数完成后自动停止计数器
- 6 个独立通道
  - 通道 1~3 可分别配置为输入或输出模式，其中每个通道可输出两路带死区保护的互补 PWM
  - 通道 4 可配置为输入或输出模式，可输出单路 PWM
  - 通道 5~6 可配置为输出比较模式
- 输入模式
  - 上升沿/下降沿捕获
  - PWM 脉宽和周期捕获 (需占用两个通道)
  - 可选 4 个输入端口之一或 1 个外部触发端口，支持防抖动滤波和预降频
- 输出模式
  - 强制输出高/低电平
  - 计数到比较值时输出高/低/翻转电平
  - PWM 输出，可配脉宽和周期
  - 多通道 PWM 组合输出，可产生有相互关系的多路 PWM
  - 单脉冲/重触发单脉冲模式输出
- 主从模式
  - 支持多计数器互连，可在作为主设备产生控制信号的同时，作为从设备被外部输入或其它主设备控制
  - 控制模式包括复位、触发、门控等
  - 支持多计数器同步启动、复位等
- 编码模式输入，控制计数器递增/递减计数

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- 支持用于定位的霍尔传感器电路
- 2 路刹车输入，支持防抖动滤波，可将输出快速置于安全状态。刹车信号源包括：
  - CPU 异常
  - 比较器
  - 外部输入
  - 软件触发
- 如下事件发生时产生中断/DMA 请求/PTC 触发：
  - 更新：计数器递增溢出/递减溢出，计数器初始化 (通过软件或者内部/外部触发)
  - 触发事件 (计数器启动、停止、初始化或者由内部/外部触发计数)
  - 输入捕获
  - 输出比较
  - 刹车
  - 换相

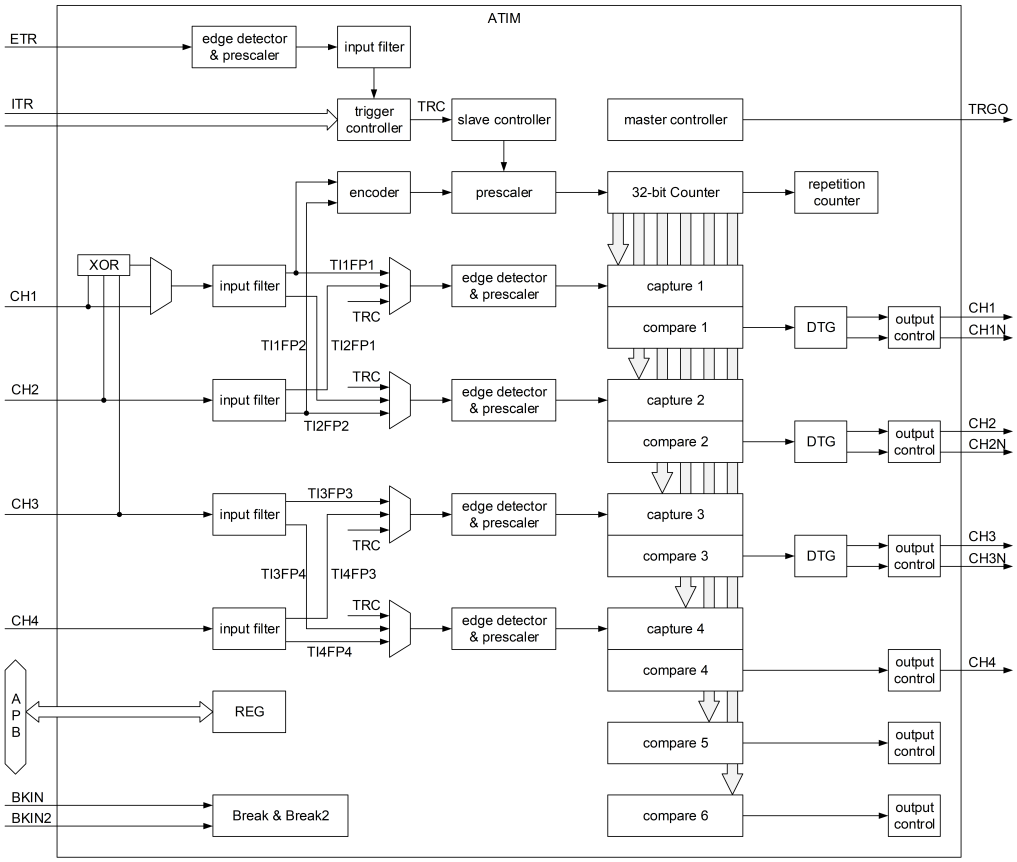


图 9-1: ATIM 结构图

9.1.3 ATIM 功能描述

9.1.3.1 计数器

ATIM 的各项功能均基于一个 32 比特的计数器。计数器基于事件计数，最基本的事件是一个 PCLK 时钟的翻转。根据不同配置，其它计数事件包括外部输入的翻转、其它定时器的输出翻转、正交编码器接口解码输出等。

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计数事件经过预分频处理才会真正进入计数器。预分频的次数介于 1 到 65536 之间 (PSC+1)，即仅当发生了 (PSC+1) 次计数事件，计数器的值才真正改变一次。

计数器共有三种计数模式：递增，递减以及中心对齐。在递增计数模式下 (CR1_CMS=0 且 CR1_DIR=0)，计数器从 0 计数到自动重载值 ARR，然后重新从 0 开始计数并产生计数器上溢事件。在递减计数模式下 (CR1_CMS=0 且 CR1_DIR=1)，计数器从 ARR 开始递减计数到 0，然后重新从 ARR 开始计数并产生计数器下溢事件。在中心对齐模式下 (CR1_CMS 不为 0)，计数器从 0 开始计数到 ARR-1，产生计数器上溢事件，然后从 ARR 开始向下计数到 1 并产生计数器下溢事件，之后从 0 开始重新计数。

计数值可以通过 CNT 读出。计数的方向可以从 CR1_DIR 读出。

9.1.3.2 更新事件 (UEV)

更新事件用于标志一个计数单元的结束。最基本的更新事件产生于每次计数器上溢或下溢时 (未开启重复计数时)。软件将 EGR_UG 置 1 时，也将产生更新事件。更新事件可以产生中断、DMA 请求以及 PTC 触发，是定时器最基本的一项通知功能。

通过软件将 CR1_UDIS 置 1 可禁止产生更新事件。这可避免向预装载寄存器写入新值时更新影子寄存器。在 UDIS 位写入 0 之前不会产生任何更新事件。

如果 CR1_URS（更新请求选择）已置 1，则将 EGR_UG 置 1 会生成更新事件，但不会将 UIF 标志置 1（因此，不会发送任何中断或 DMA 请求）。这样一来，如果在发生捕获事件时将计数器清零，将不会同时产生更新中断和捕获中断。

发生更新事件时，将重新装载 RCR，ARR 以及 PSC 寄存器，且将更新标志 SR_UIF 置 1（CR1_URS=0 时）。该功能可以保证修改这些计数器的基本参数不影响当前计数单元，在下一个计数周期才生效。

9.1.3.3 重复计数

如果配置了重复计数器 (RCR>0)，每次计数器上溢或下溢时重复计数器会递减，并仅当重复计数器为 0 时才产生更新事件。更新事件发生时，重复计数器会重新装载 RCR 的值。

重复计数器的当前值不能读出。

9.1.3.4 影子寄存器

对 RCR，ARR 以及 PSC 寄存器的修改不会直接体现在当前计数单元中，而是等到更新事件发生时才真正更新进去。在更新事件发生前，计数器真正使用的是影子寄存器中的值。这样即使在计数中动态改变这些寄存器的值，也不会影响到当前计数单元的完整性，对于 PWM 输出等应用场景很有意义。

如果 CR1_APRE 为 0，ARR 寄存器将在配置后实时生效，不用等到更新事件发生。

输出比较寄存器 CCRx 也有影子寄存器。当 CCMRx_OCxPE 为 0 时，配置的 CCRx 会立即生效，否则要等到更新事件发生时才生效。

9.1.3.5 主从模式

定时器可同时处于主模式与从模式。主模式是指该定时器可以输出 TRGO 信号至芯片上其它定时器的 ITR 输入，用于控制其它定时器的计数行为。从模式是指该定时器的计数行为受外部输入 ETR，其它定时器输出至该定时

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器的 ITR 信号，或定时器的通道输入 CHx 的控制。

多个定时器可通过主从模式实现定时器同步，以实现多级分频、同时启动、门控计数等功能。

主模式可在不同事件发生时输出 TRGO 信号，如更新、使能、输入捕获、输出比较等，由 CR2_MMS 选择。

从模式可以选择计数器复位、触发启动、计数使能、计数事件等行为，由 SMCR_SMS 选择。从模式依赖的触发信号 TRGI 可灵活配置，可以在 ETR，ITR 以及通道输入中选择，并可选择信号极性，进行预分频、滤波等操作。

- 定时器处于复位从模式 (SMCR_SMS=0100) 时，当 TRGI 发生变化时，计数器及其预分频器重新初始化。如果 CR1_URS 为 0，则会生成更新事件 UEV，然后所有预装载寄存器 ARR 和 CCRx 都将更新。
- 定时器处于门控从模式 (SMCR_SMS=0101) 时，当 TRGI 满足高电平或低电平要求时才进行计数，否则计数器不变。
- 定时器处于触发从模式 (SMCR_SMS=0110) 时，软件不需配置 CR1_CEN 开启计数，而是当 TRGI 满足特定触发要求时自动启动计数器。
- 定时器处于外部时钟从模式 (SMCR_SMS=0111) 时，计数事件修改为 TRGI 的上升沿，仅当 TRGI 发生翻转时才进行计数。
- 定时器处于复位触发从模式 (SMCR_SMS=1000) 时，TRGI 满足特定触发要求时复位计数器并自动重新开启。

9.1.3.6 通道输入输出

定时器的部分通道可以独立配置为输入捕获模式 (CCMRx_CCxS!=0) 或输出模式 (CCMRx_CCxS=0)。

在输入捕获模式下，通道在对应的触发信号有效时，将计数器的值记录进 CCRx，并产生中断等通知信号。该触发信号可在 ETR，ITR 以及通道输入 CHx 中选择，并可选择信号极性，进行预分频、滤波等操作。通道产生的通知信号包括中断、DMA 请求、PTC 触发等。输入捕获模式可实现记录外部信号改变的时刻、测量 PWM 周期和占空比等功能。

在输出模式下，通道将比较计数器的值与 CCRx 的大小，在通道输出 CHx/CHxN 上产生固定电平，或产生基于本通道以及其它通道比较结果的 PWM 输出信号，并产生中断等通知信号。产生 PWM 信号的脉冲个数、频率、占空比、相位等参数均可调节。多个通道还可以联合产生特定关系的 PWM 组合，如带死区保护的 6 路互补 PWM 等。通道产生的通知信号包括中断、DMA 请求、PTC 触发等。

在输出模式下，一旦出现紧急情况，可以通过断路输入信号 BKIN 和 BKIN2 紧急关闭输出使能，或将输出置于预设电平，以保护定时器连接的外部电路。

9.1.3.7 输入捕获模式

在输入捕获模式下，当通道相应的触发信号检测到跳变沿后，将使用 CCRx 来锁存计数器的值。发生捕获事件时，会将相应的 SR_CCxIF 标志置 1，并可发送中断、DMA 请求（如果已使能）或 PTC 触发信号。如果发生捕获事件时 SR_CCxIF 标志已处于高位，则会将重复捕获标志 SR_CCxOF 置 1。可通过软件将 SR_CCxIF 清零，方法是向 SR_CCxIF 写入 0，或读取存储在 CCRx 中的已捕获数据。向 SR_CCxOF 写入 0 后会将其清零。

以下示例说明了如何在 CH1 输入出现上升沿时将计数器的值捕获到 CCR1 中，具体操作步骤如下：

1. 选择有效输入：通道 1 要连接到 CH1 输入，因此向 CCMR1_CC1S 写入 01。
2. 根据连接到定时器的信号，对所需的输入滤波带宽进行配置。

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假设 CH1 信号边沿变化时，最多在 5 个 PCLK 周期内发生抖动，需将滤波带宽设置为大于 5 个 PCLK 周期。将 CCMR1_IC1F 设置为 0011(0x3)，则在检测到连续 8 个采样点（以 PCLK 频率采样）均为新电平后，可以确认 CH1 的跳变沿。

3. 将 CCER_CC1P 和 CCER_CC1NP 写 0，选择 CH1 上的有效转换边沿为上升沿。
4. 对输入预分频器进行编程。
   在本例中我们希望每次有效转换时都执行捕获操作，因此禁用预分频器（CCMR1_IC1PS 写 00）。
5. CCER_CC1E 置 1，使能通道 1，允许将计数器的值捕获到 CCR1 中。
6. 如果需要，可将 DIER_CC1IE 置 1 来使能相关中断请求，或将 DIER_CC1DE 置 1 来使能 DMA 请求。

配置完成后，通道将在 CH1 输入出现上升沿时执行下列操作：

1. CCR1 寄存器记录计数器的值。
2. SR_CCxIF 标志置 1（中断标志）。如果至少发生了两次连续捕获，但 SR_CCxIF 未被清零，这样 SR_CCxOF 捕获溢出标志会被置 1。
3. 根据 CCER_CC1IE 生成中断。
4. 根据 DIER_CC1DE 生成 DMA 请求。

要处理重复捕获，建议在读出 SR_CCxOF 之前读取数据。这样可避免丢失在读取 SR_CCxOF 之后与读取数据之前可能出现的重复捕获信息。

通过软件将 EGR_CCxG 置 1 可立即产生一次捕获，并生成通道捕获中断和 DMA 请求。

9.1.3.8 PWM 输入捕获

PWM 输入捕获是输入捕获的一种扩展应用，可用于测量 PWM 输入信号的周期和占空比。为实现该功能，需要将两个通道都配置为输入捕获模式，触发信号分别映射成输入 PWM 的正边沿和负边沿，并开启计数器复位的从模式。

以下示例说明了如何用通道 1 和通道 2 测量从 CH1 输入的 PWM 的周期和占空比，具体操作步骤如下：

1. 选择通道 1 的有效输入为 CH1 输入，因此向 CCMR1_CC1S 写入 01。
2. 选择通道 1 输入信号的有效极性（用于在 CCR1 中捕获和计数器清零），将 CCER_CC1P 和 CCER_CC1NP 写 0，选择 CH1 上的有效转换边沿为上升沿。
3. 选择通道 2 的有效输入也为 CH1 输入，向 CCMR1_CC2S 写入 10(0x2)。
4. 选择通道 2 输入信号的有效极性（用于 CCR2 捕获），将 CCER_CC2P 写 1，CCER_CC1NP 写 0，选择 CH1 上的有效转换边沿为下降沿。
5. 设置从模式控制信号为 CH1，向 SMCR_TS 写入 101(0x5)，选择 TI1FP1。
6. 将从模式控制器配置为复位模式，向 SMCR_SMS 写入 0100(0x4)。
7. 使能通道 1 和通道 2，将 CCER_CC1E 和 CCER_CC2E 置 1。

配置完成后，在每个 CH1 的上升沿，计数器的值被记录在 CCR1 中，同时计数器被复位并重新开始计数；在每个 CH1 的下降沿，计数器的值被记录在 CCR2 中。将 CCR1 的值乘以 PCLK 的周期，可以算出 PWM 的周期。将 CCR2 的值乘以 PCLK 的周期，可以算出 PWM 高电平持续的时间，从而得到 PWM 的占空比。

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9.1.3.9 输出比较模式

在输出比较模式下，当计数值与 CCRx 满足一定关系时，可以在对应 CHx 及 CHxN 上产生特定输出，通常用于控制输出波形，或指示已经过某一时间段。

具体而言，通道将在 CCRx 与计数器之间相匹配时执行下列操作：

1. 将为相应的 CHx 和 CHxN 输出分配一个可编程值，该值由比较模式寄存器 CCMRx_OCxM 和输出极性寄存器 CCER_CCxP/CCxNP 定义。匹配时，输出引脚既可保持其电平（CCMRx_OCxM=0000），也可设置为有效电平 (CCMRx_OCxM=0001)、无效电平 (CCMRx_OCxM=0010) 或进行翻转 (CCMRx_OCxM=0011)。
2. 将中断状态寄存器标志 SR_CCxIF 置 1。
3. 根据 CCER_CC1IE 生成中断。
4. 根据 DIER_CC1DE 和 CR2_CCDS 生成 DMA 请求。

配置 CCMRx_OCxPE，可将 CCRx 寄存器配置为带或不带影子寄存器。当 CCMRx_OCxPE 为 0 时，软件修改 CCRx 实时生效，可通过在每次中断中修改下一次匹配的 CCRx 来实现自定义波形的输出。

将 BDTR_MOE 设为 1 后 CH 和 CHxN 输出才生效。

9.1.3.10 基础 PWM 输出

利用输出比较模式，定时器可以产生周期、占空比、相位可控的多路 PWM 输出。PWM 输出的周期由 ARR 决定，占空比由 CCRx 决定。PWM 输出有多种模式，由每个通道的 CCMRx_OCxM 各自独立选择。最基本的单路 PWM 输出只需要占用一个通道，采用基础的 PWM 模式即可实现。复杂的 PWM 信号，或 PWM 组合则需要占用多个通道，并需仔细分配每个通道的 PWM 模式以及 CCRx。

在基础的 PWM 模式下，计数器值 CNT 与 CCRx 进行比较，并根据计数器的当前计数方向产生包含有效电平或无效电平的比较输出信号 OCxREF。有效电平的极性可通过 CCER_CCxP 配置，并根据 CCER_CCxE 和 BDTR_MOE 等寄存器使能 CHx 输出。将 BDTR_MOE 设为 1 后 PWM 输出才生效。

如在递增计数模式下，配置 CCMR1_OC1M 和 CCMR1_OC2M 为 0110(0x6)，则 PWM 输出如图9-2。其中计数值 CNT 小于 CCR1/2 时，输出高电平，否则输出低电平。

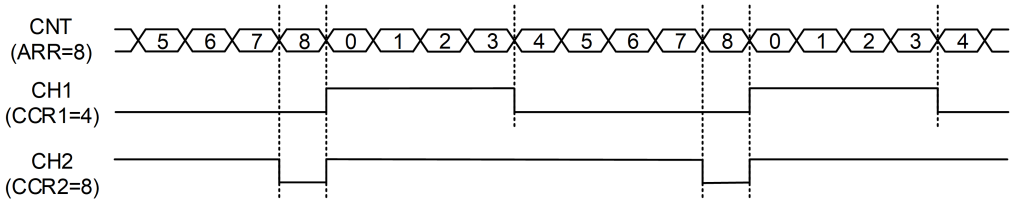


图 9-2: 递增计数模式下的 PWM 输出

如在中心对齐计数模式下，配置 CCMR1_OC1M 和 CCMR1_OC2M 为 0110(0x6)，则 PWM 输出如图9-3。其中递增阶段计数值 CNT 小于 CCR1/2 时，输出高电平，否则输出低电平；递减阶段计数值 CNT 大于 CCR1/2 时，输出低电平，否则输出高电平。

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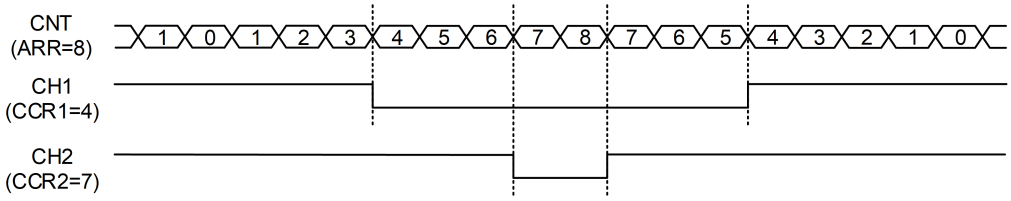


图 9-3: 中心对齐计数模式下的 PWM 输出

9.1.3.11 不对称 PWM 输出

在不对称 PWM 模式下，生成的两个 PWM 信号之间存在可编程相移。该模式仅限于计数器处于中心对齐模式时。生成的两个 PWM 信号频率相同，由 ARR 的值确定，而占空比和相移则各由一对 CCRx 寄存器确定。每一路输出 PWM 占用两个 CCRx 寄存器，分别控制递增计数和递减计数期间的行为，这样 PWM 的上升沿和下降沿时间点可以分别配置。CCR1 和 CCR2 共同控制 CH1/2 的输出，CCR3 和 CCR4 共同控制 CH3/4 的输出。

CH1/2 以及 CH3/4 可以独立选择不同的不对称 PWM 模式，配置 CCMRx_OCxM 为 1110(0xe) 或 1111(0xf)。

如配置 CCMR1_OC1M 和 CCMR2_OC3M 为 1110(0xe)，则 PWM 输出如图9-4。其中递增阶段 (0->ARR-1) 计数值 CNT 小于 CCR1/3 时，输出高电平，否则输出低电平；递减阶段 (ARR->1) 计数值 CNT 大于 CCR2/4 时，输出低电平，否则输出高电平。

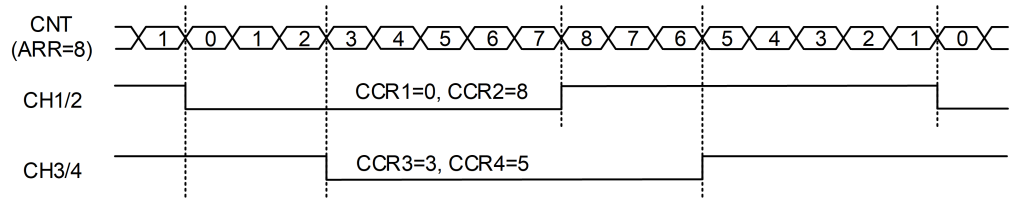


图 9-4: 不对称 PWM 输出

9.1.3.12 组合 PWM 输出

在组合 PWM 模式下，生成的两个 PWM 信号之间存在可编程延时和相移。计数器处于递增、递减或中心对齐模式均可，生成的两个 PWM 信号频率相同，由 ARR 的值确定，而占空比和相移则各由一对 CCRx 寄存器确定。每一路输出 PWM 占用两个 CCRx 寄存器，是由两路基础 PWM 输出波形的逻辑与运算或者逻辑或运算组合而成。CCR1 和 CCR2 共同控制 CH1/2 的输出，CCR3 和 CCR4 共同控制 CH3/4 的输出。

CH1/2 以及 CH3/4 可以独立选择不同的组合 PWM 模式，配置 CCMRx_OCxM 为 1100(0xc) 或 1101(0xd)。当 CH1 或 CH3 配置为组合 PWM 模式 1100(0xc) 时，CH2 或 CH4 必须配置为 0111(0x7) 或 1101(0xd) 或 1111(0xf)。当 CH1 或 CH3 配置为组合 PWM 模式 1101(0xd) 时，CH2 或 CH4 必须配置为 0110(0x6) 或 1100(0xc) 或 1110(0xe)。

如配置 CCMR1_OC1M 为 1101(0xd)，CCMR1_OC2M 为 0110(0x6)，CCMR2_OC3M 为 1100(0xc)，CCMR2_OC4M 为 0111(0x7)，则 PWM 输出如图9-5。其中计数值 CNT 小于 CCR1/4 时，OC1REF/OC4REF 为低电平，否则为高电平；计数值 CNT 小于 CCR2/3 时，OC2REF/OC3REF 为高电平，否则为低电平。CH1 输出是 OC1REF 和 OC2REF 的逻辑与运算。CH3 输出是 OC3REF 和 OC4REF 的逻辑或运算。

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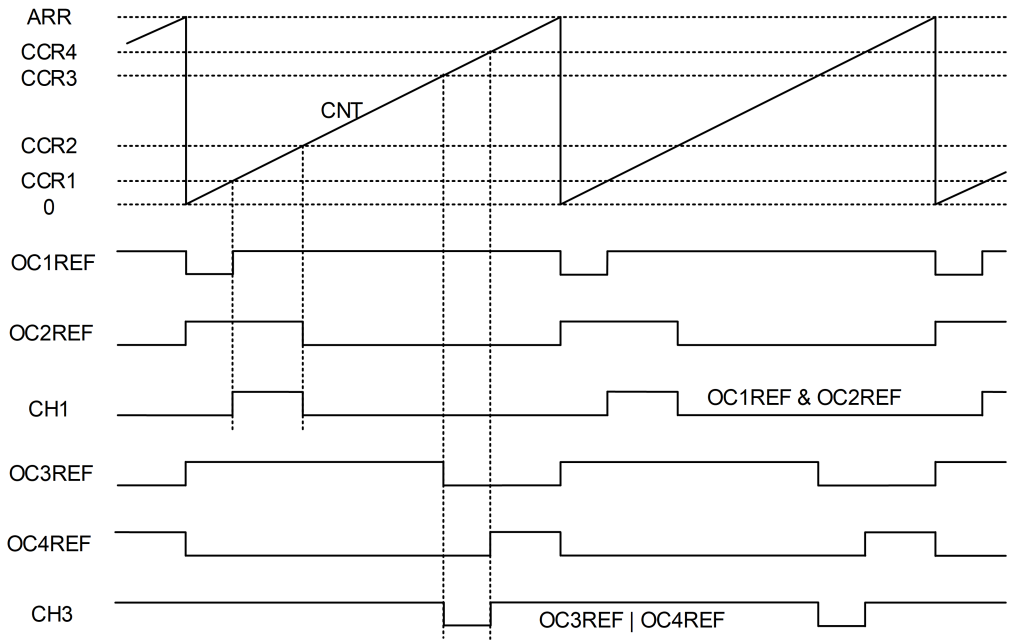


图 9-5: 组合 PWM 输出

9.1.3.13 带死区的互补 PWM 输出

ATIM 可以输出两路相位相反的互补 PWM 信号 CHx 与 CHxN，并在两路信号跳变的边沿插入一定延时。这段延时通常称为死区，用户必须根据与输出相连接的器件及其特性（如电平转换器的固有延迟、开关器件产生的延迟等）来调整死区时间。

ATIM 的通道 1/2/3 每个均可输出一组互补 PWM 信号，最多可同时输出 3 组共 6 路互补信号。其中每路输出可以通过 CCER_CCxP 和 CCER_CCxNP 独立选择输出极性。将 BDTR_MOE 以及对应通道的 CCER_CCxE 和 CCER_CCxNE 配置成 1 使能互补输出。

互补输出的示例如图9-6。CHx 的上升沿相对该通道产生的参考输出 OCxREF 的上升沿有一个死区时间的延时，而 CHxN 的上升沿相对该通道的 OCxREF 的下降沿有一个死区时间的延时。

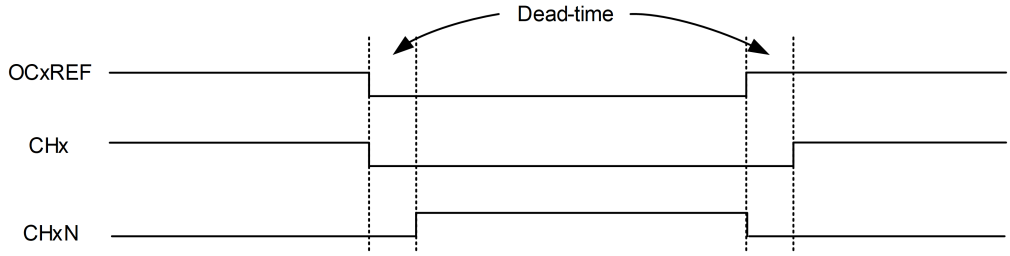


图 9-6: 带死区的互补 PWM 输出

死区时间在一定范围内可调节。当 BDTR_DTPSC 为 0 时，死区时间为 BDTR_DTG 乘以 PCLK 周期。当 BDTR_DTPSC 为 1 时，死区时间为 BDTR_DTG 乘以 16 倍 PCLK 周期。假如 PCLK 为 120MHz，死区时间可调范围为 0~136us。

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9.1.3.14 紧急断路

断路功能的目的是保护由 ATIM 产生的 PWM 信号所驱动的功率开关。两个断路输入 BKIN 和 BKIN2 通常连接到功率级和三相逆变器的故障输出。激活时，断路电路会关闭 PWM 输出，并将其强制为预定义的安全状态。也可选择一些芯片内部事件来触发输出关断。BKIN 可以在死区持续时间后将输出强制为预定义的电平（有效或无效）。BKIN 能够将输出强制为无效状态。

断路期间的输出使能信号和输出电平取决于多个控制位：BDTR_MOE 允许通过软件使能/禁止输出；BDTR_OSSI 定义定时器将输出控制在无效状态下，还是释放控制权给 GPIO 控制器（通常使其处于高阻态模式）；CR2_OISx/OISxN 将输出设置为关断电平（有效或无效）。

ATIM 复位后，断路功能处于禁止状态，BDTR_MOE 处于低电平。将 BDTR_BKE/BKE2 置 1，可使能断路功能。可通过配置 BDTR_BKP/BKP2 选择断路输入的极性。也可由软件配置 EGR_BG/B2G 产生断路事件，不依赖于 BDTR_BKE/BKE2 的值。

断路电路内部还实施了写保护，用以保护应用的安全。通过该功能，用户可冻结多个参数配置，如死区持续时间、输出极性和禁止时的状态、PWM 模式、断路使能和极性等。该功能通过写 AF1_LOCK 寄存器实现，从 3 种保护级别中进行选择。

9.1.3.15 6 步 PWM

6 步 PWM 需要在 PWM 输出过程中的某一时刻同时切换各通道的 PWM 模式，可以通过 ATIM 的换向事件 (COM) 实现。当通道使用互补输出时，CCMRx_OCxM、CCER_CCxE 和 CCER_CCxNE 有预装载机制。用户可以预先编程下一步骤的配置，当发生换向事件时，预装载寄存器将传输到影子寄存器，同时更改所有通道的配置。COM 可由软件通过将 EGR_COM 置 1 生成，也可以由硬件在输入触发信号的上升沿生成。发生换向事件时，SR_COMIF 将会置 1。这时，如果 DIER_COMIE 为 1，将产生中断；如果 DIER_COMDE 为 1，将产生 DMA 请求。

9.1.3.16 单脉冲模式

将 CR1_OPM 写 1 可以使能单脉冲模式。该模式下计数器启动以后一旦发生更新事件，就会自动停止计数。该模式可以用于单次计数，或在一个激励信号的触发下启动，并在一段可编程的延时后产生一个脉宽可编程的脉冲。

例如，希望实现这样的功能，在 CH2 输入引脚检测到上升沿时，经过一定时间延迟，在 CH1 上产生单个一定宽度的正脉冲。配置方法如下：

1. CCMR1_CC2S=01，以将 TI2FP2 映射到通道 2。
2. CCER_CCxP 和 CCER_CCxNP 写 0，TI2FP2 反应 CH2 上升沿的变化。
3. SMCR_TS=110(0x6)，将 TI2FP2 配置为从模式控制器的触发 TRGI。
4. SMCR_SMS=110(0x6)，将从模式控制器配置为触发模式，触发后开启计数。
5. 根据需要的时间延迟与脉冲宽度配置 ARR 与 CCR1，定义时间延迟与脉冲宽度。
6. CCMR1_OC1M=0111(0x7)，配置为正脉冲 PWM。
7. CR1_OPM=1，一次触发只产生一个脉冲。
8. EGR_UG=1，手动刷新 ARR 与 CCR1 寄存器。

从模式为触发模式时不需要手动使能 CR1_CEN，一旦检测到触发信号生效，计数器就会自动使能。

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9.1.3.17 编码器接口模式

编码器接口模式下，通道 1 和通道 2 可以用于连接外部正交编码器，将外部编码器的信号转化为定时器的计数值变化，从而获知外部编码器的工作状态。

如果计数器仅在 CH1 边沿处计数，SMCR_SMS 配置为 0001；如果计数器仅在 CH2 边沿处计数，SMCR_SMS 配置为 0010(0x2)；如果计数器在 CH1 和 CH2 边沿处均计数，SMCR_SMS 配置为 0011(0x3)。CCER_CC1P/CC2P 用于选择 CH1 和 CH2 极性。如果需要，还可对输入滤波器进行编程。两个输入的信号转换序列会产生计数脉冲和方向信号，根据该信号转换序列，计数器相应递增或递减计数，同时硬件对 CR1_DIR 进行相应修改。

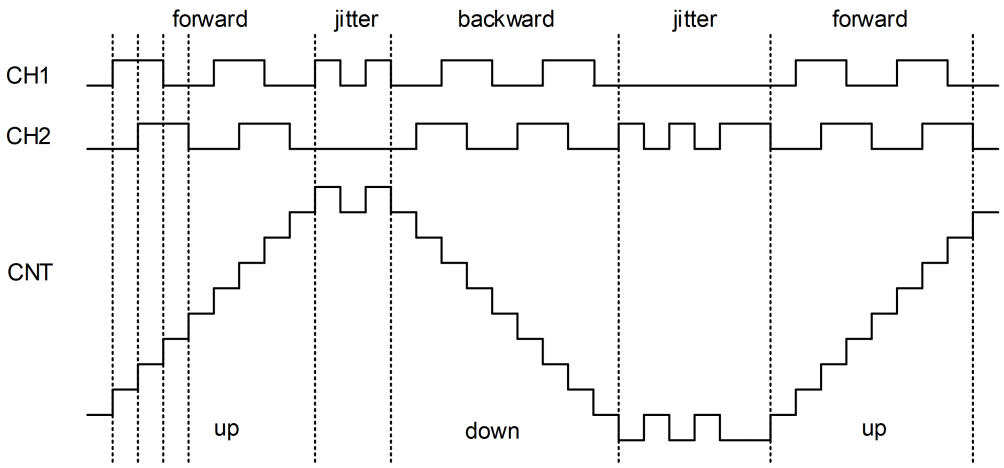
编码器接口模式下，计数器的计数事件是正交编码器接口的解码输出。计数器仅在 0 到 ARR 之间进行连续计数（根据计数的具体方向，从 0 递增计数到 ARR，或从 ARR 递减计数到 0）。因此，在启动前必须先配置 ARR。同样，捕获、比较、重复计数器和触发输出功能继续正常工作。在此模式下，计数器会根据正交编码器的速度和方向自动进行修改，因此，其内容始终表示编码器的位置。计数方向对应于所连传感器的旋转方向。下表汇总了可能的组合（假设 CH1 和 CH2 不同时切换）。

SMCR_SMS	条件	CH1 上升沿	CH1 下降沿	CH2 上升沿	CH2 下降沿
0001 或 0011	CH2=0	递增	递减	/	/
	CH2=1	递减	递增	/	/
0010 或 0011	CH1=0	/	/	递减	递增
	CH1=1	/	/	递增	递减

下图示意了计数器如何根据正交编码器的信号变化进行计数的，配置如下：

CCMR1_CC1S=01（CH1 映射到通道 1 上），CCMR2_CC2S=01（CH2 映射到通道 2 上），

CCER_CC1P/CC1NP/CC2P/CC2NP=0，SMCR_SMS=0011(0x3)，CR1_CEN=1。



9.1.3.18 定时器同步

多个定时器可通过主从模式连接在一起，实现定时器同步，以完成多级分频、同时启动、门控计数等功能。

将主模式定时器的 TRGO 设置为更新事件 (CR2_MMS=010)，连接至另一个设置为外部时钟从模式 (SMCR_SMS = 0111) 的定时器，可以实现定时器级联计数。此时主模式定时器相当于从模式定时器的预分频，计数总位宽等

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于两个定时器各自的位宽相加。

将主模式定时器的 TRGO 设置为计数使能 (CR2_MMS=001)，连接至另一个设置为触发从模式 (SMCR_SMS=0110) 的定时器，可以实现定时器同步启动，从而对齐多个定时器的开启时机。

将主模式定时器的 TRGO 设置为比较输出 (CR2_MMS=100)，连接至另一个设置为门控从模式 (SMCR_SMS=0101) 的定时器，可以实现门控 PWM 输出。主模式定时器可以对从模式定时器输出的 PWM 载波进行调制输出。

9.1.3.19 通知机制

ATIM 能够产生中断、DMA 请求、PTC 触发等多种通知机制。能够触发通知的事件主要包括更新事件、触发事件、比较器匹配、输入捕获、断路输入、换向事件等。DIER 寄存器可以控制各种事件是否产生中断和 DMA 请求。各事件状态可在 SR 寄存器中查询。

9.1.4 ATIM 寄存器

ATIM1 的基地址是 0x50004000。ATIM2 的基地址是 0x50005000。

表 9-1: ATIM 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**CR1**	TIM control register 1
[31:12]			RSVD	
[11]	rw	1'h0	UIFREMAP	UIF status bit remapping 0: No remapping. UIF status bit is not copied to CNT register bit 31 1: Remapping enabled. UIF status bit is copied to CNT register bit 31.
[10:8]			RSVD	
[7]	rw	1'h0	ARPE	Auto-reload preload enable 0: ARR register is not buffered 1: ARR register is buffered
[6:5]	rw	2'h0	CMS	Center-aligned mode selection 00: Edge-aligned mode. The counter counts up or down depending on the direction bit (DIR). 01: Center-aligned mode 1. The counter counts up and down alternatively. Output compare interrupt flags of channels configured in output (CCxS=00 in CCMRx register) are set only when the counter is counting down. 10: Center-aligned mode 2. The counter counts up and down alternatively. Output compare interrupt flags of channels configured in output (CCxS=00 in CCMRx register) are set only when the counter is counting up. 11: Center-aligned mode 3. The counter counts up and down alternatively. Output compare interrupt flags of channels configured in output (CCxS=00 in CCMRx register) are set both when the counter is counting up or down.
[4]	rw	1'h0	DIR	Direction 0: Counter used as upcounter 1: Counter used as downcounter
[3]	rw	1'h0	OPM	One-pulse mode 0: Counter is not stopped at update event 1: Counter stops counting at the next update event (clearing the bit CEN)

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[2]	rw	1'h0	URS	Update request source This bit is set and cleared by software to select the UEV event sources. 0: Any of the following events generate an update interrupt or DMA request if enabled. These events can be: Counter overflow/underflow Setting the UG bit Update generation through the slave mode controller 1: Only counter overflow/underflow generates an update interrupt or DMA request if enabled.
[1]	rw	1'h0	UDIS	Update disable This bit is set and cleared by software to enable/disable UEV event generation. 0: UEV enabled. The Update (UEV) event is generated by one of the following events: Counter overflow/underflow Setting the UG bit Update generation through the slave mode controller Buffered registers are then loaded with their preload values. 1: UEV disabled. The Update event is not generated, shadow registers keep their value (ARR, PSC, CCRx). However the counter and the prescaler are reinitialized if the UG bit is set or if a hardware reset is received from the slave mode controller.
[0]	rw	1'h0	CEN	Counter enable 0: Counter disabled 1: Counter enabled External clock, gated mode and encoder mode can work only if the CEN bit has been previously set by software. However trigger mode can set the CEN bit automatically by hardware. CEN is cleared automatically in one-pulse mode, when an update event occurs.
0x04			**CR2**	TIM control register 2
[31:19]			RSVD	
[18]	rw	1'h0	OIS6	Output Idle state 6 (OC6 output)
[17]			RSVD	
[16]	rw	1'h0	OIS5	Output Idle state 5 (OC5 output)
[15]			RSVD	
[14]	rw	1'h0	OIS4	Output Idle state 4 (OC4 output)
[13]	rw	1'h0	OIS3N	Output Idle state 3 (OC3N output)
[12]	rw	1'h0	OIS3	Output Idle state 3 (OC3 output)
[11]	rw	1'h0	OIS2N	Output Idle state 2 (OC2N output)
[10]	rw	1'h0	OIS2	Output Idle state 2 (OC2 output)
[9]	rw	1'h0	OIS1N	Output Idle state 1 (OC1N output) 0: OC1N=0 after a dead-time when MOE=0 1: OC1N=1 after a dead-time when MOE=0 This bit, as well as other OISxN, can not be modified as long as LOCK level 1, 2 or 3 has been programmed
[8]	rw	1'h0	OIS1	Output Idle state 1 (OC1 output) 0: OC1=0 (after a dead-time if OC1N is implemented) when MOE=0 1: OC1=1 (after a dead-time if OC1N is implemented) when MOE=0 This bit, as well as other OISx, can not be modified as long as LOCK level 1, 2 or 3 has been programmed

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7]	rw	1'h0	TI1S	TI1 selection 0: The CH1 pin is connected to TI1 input 1: The CH1, CH2 and CH3 pins are connected to the TI1 input (XOR combination)
[6:4]	rw	3'h0	MMS	Master mode selection These bits allow to select the information to be sent in master mode to slave timers for synchronization (TRGO). The combination is as follows: 000: Reset - the UG bit from the EGR register is used as trigger output (TRGO). If the reset is generated by the trigger input (slave mode controller configured in reset mode) then the signal on TRGO is delayed compared to the actual reset. 001: Enable - the Counter enable signal, CNT_EN, is used as trigger output (TRGO). It is useful to start several timers at the same time or to control a window in which a slave timer is enabled. The Counter Enable signal is generated by a logic OR between CEN control bit and the trigger input when configured in gated mode. When the Counter Enable signal is controlled by the trigger input, there is a delay on TRGO, except if the master/slave mode is selected. 010: Update - The update event is selected as trigger output (TRGO). For instance a master timer can then be used as a prescaler for a slave timer. 011: Compare Pulse - The trigger output send a positive pulse when the CC1IF flag is to be set (even if it was already high), as soon as a capture or a compare match occurred. (TRGO) 100: Compare - OC1REFC signal is used as trigger output (TRGO) 101: Compare - OC2REFC signal is used as trigger output (TRGO) 110: Compare - OC3REFC signal is used as trigger output (TRGO) 111: Compare - OC4REFC signal is used as trigger output (TRGO)
[3]	rw	1'h0	CCDS	Capture/compare DMA selection 0: CCx DMA request sent when CCx event occurs 1: CCx DMA requests sent when update event occurs
[2]	rw	1'h0	CCUS	Capture/compare control update selection 0: When capture/compare control bits are preloaded (CCPC=1), they are updated by setting the COMG bit only 1: When capture/compare control bits are preloaded (CCPC=1), they are updated by setting the COMG bit or when an edge occurs on TRGI after Trigger selection This bit acts only on channels that have a complementary output.
[1]			RSVD	
[0]	rw	1'h0	CCPC	Capture/compare preloaded control 0: CCxE, CCxNE and OCxM bits are not preloaded 1: CCxE, CCxNE and OCxM bits are preloaded, after having been written, they are updated only when a commutation event (COM) occurs (COMG bit set or edge detected on TRGI after Trigger selection, depending on the CCUS bit). This bit acts only on channels that have a complementary output.
0x08			**SMCR**	TIM slave mode control register
[31:20]			RSVD	

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[19:16]	rw	4'h0	SMS	Slave mode selection When external signals are selected the active edge of the trigger signal (TRGI) is linked to the polarity selected on the external input. 0000: Slave mode disabled. 0001: Encoder mode 1 - Counter counts up/down on TI1FP1 edge depending on TI2FP2 level. 0010: Encoder mode 2 - Counter counts up/down on TI2FP2 edge depending on TI1FP1 level. 0011: Encoder mode 3 - Counter counts up/down on both TI1FP1 and TI2FP2 edges depending on the level of the other input. 0100: Reset Mode - Rising edge of the selected trigger input (TRGI) reinitializes the counter and generates an update of the registers. 0101: Gated Mode - The counter clock is enabled when the trigger input (TRGI) is high. The counter stops (but is not reset) as soon as the trigger becomes low. Both start and stop of the counter are controlled. 0110: Trigger Mode - The counter starts at a rising edge of the trigger TRGI (but it is not reset). Only the start of the counter is controlled. 0111: External Clock Mode 1 - Rising edges of the selected trigger (TRGI) clock the counter. 1000: Combined reset + trigger mode - Rising edge of the selected trigger input (TRGI) reinitializes the counter, generates an update of the registers and starts the counter.
[15]	rw	1'h0	ETP	External trigger polarity This bit selects whether ETR or ETR is used for trigger operations 0: ETR is non-inverted, active at high level or rising edge 1: ETR is inverted, active at low level or falling edge
[14]	rw	1'h0	ECE	External clock enable This bit enables External clock mode 2. 0: External clock mode 2 disabled 1: External clock mode 2 enabled. The counter is clocked by any active edge on the ETRF signal.
[13:12]	rw	2'h0	ETPS	External trigger prescaler External trigger signal ETRP frequency must be at most 1/4 of CK_INT frequency. A prescaler can be enabled to reduce ETRP frequency. It is useful when inputting fast external clocks. 00: Prescaler OFF 01: ETRP frequency divided by 2 10: ETRP frequency divided by 4 11: ETRP frequency divided by 8

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11:8]	rw	4'h0	ETF	External trigger filter This bit-field then defines the frequency used to sample ETRP signal and the length of the digital filter applied to ETRP. The digital filter is made of an event counter in which N consecutive events are needed to validate a transition on the output: 0000: No filter, sampling is done at fCLK 0001: fSAMPLING=fCLK, N=2 0010: fSAMPLING=fCLK, N=4 0011: fSAMPLING=fCLK, N=8 0100: fSAMPLING=fCLK/2, N=6 0101: fSAMPLING=fCLK/2, N=8 0110: fSAMPLING=fCLK/4, N=6 0111: fSAMPLING=fCLK/4, N=8 1000: fSAMPLING=fCLK/8, N=6 1001: fSAMPLING=fCLK/8, N=8 1010: fSAMPLING=fCLK/16, N=5 1011: fSAMPLING=fCLK/16, N=6 1100: fSAMPLING=fCLK/16, N=8 1101: fSAMPLING=fCLK/32, N=5 1110: fSAMPLING=fCLK/32, N=6 1111: fSAMPLING=fCLK/32, N=8
[7]	rw	1'h0	MSM	Master/Slave mode 0: No action 1: The effect of an event on the trigger input (TRGI) is delayed to allow a perfect synchronization between the current timer and its slaves (through TRGO). It is useful if we want to synchronize several timers on a single external event.
[6:4]	rw	3'h0	TS	Trigger selection This bit-field selects the trigger input to be used to synchronize the counter. 000: Internal Trigger 0 (ITR0) 001: Internal Trigger 1 (ITR1) 010: Internal Trigger 2 (ITR2) 011: Internal Trigger 3 (ITR3) 100: TI1 Edge Detector (TI1F_ED) 101: Filtered Timer Input 1 (TI1FP1) 110: Filtered Timer Input 2 (TI2FP2) 111: External Trigger input (ETRF)
[3:0]			RSVD	
0x0C			**DIER**	TIM DMA/Interrupt enable register
[31:18]			RSVD	
[17]	rw	1'h0	CC6IE	Capture/Compare 6 interrupt enable 0: CC6 interrupt disabled. 1: CC6 interrupt enabled
[16]	rw	1'h0	CC5IE	Capture/Compare 5 interrupt enable 0: CC5 interrupt disabled. 1: CC5 interrupt enabled
[15]			RSVD	
[14]	rw	1'h0	TDE	Trigger DMA request enable 0: Trigger DMA request disabled. 1: Trigger DMA request enabled.

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[13]	rw	1'h0	COMDE	COM DMA request enable 0: COM DMA request disabled 1: COM DMA request enabled
[12]	rw	1'h0	CC4DE	Capture/Compare 4 DMA request enable 0: CC4 DMA request disabled. 1: CC4 DMA request enabled
[11]	rw	1'h0	CC3DE	Capture/Compare 3 DMA request enable 0: CC3 DMA request disabled. 1: CC3 DMA request enabled.
[10]	rw	1'h0	CC2DE	Capture/Compare 2 DMA request enable 0: CC2 DMA request disabled. 1: CC2 DMA request enabled.
[9]	rw	1'h0	CC1DE	Capture/Compare 1 DMA request enable 0: CC1 DMA request disabled. 1: CC1 DMA request enabled.
[8]	rw	1'h0	UDE	Update DMA request enable 0: Update DMA request disabled. 1: Update DMA request enabled
[7]	rw	1'h0	BIE	Break interrupt enable 0: Break interrupt disabled 1: Break interrupt enabled
[6]	rw	1'h0	TIE	Trigger interrupt enable 0: Trigger interrupt disabled. 1: Trigger interrupt enabled
[5]	rw	1'h0	COMIE	COM interrupt enable 0: COM interrupt disabled 1: COM interrupt enabled
[4]	rw	1'h0	CC4IE	Capture/Compare 4 interrupt enable 0: CC4 interrupt disabled. 1: CC4 interrupt enabled
[3]	rw	1'h0	CC3IE	Capture/Compare 3 interrupt enable 0: CC3 interrupt disabled. 1: CC3 interrupt enabled
[2]	rw	1'h0	CC2IE	Capture/Compare 2 interrupt enable 0: CC2 interrupt disabled. 1: CC2 interrupt enabled.
[1]	rw	1'h0	CC1IE	Capture/Compare 1 interrupt enable 0: CC1 interrupt disabled. 1: CC1 interrupt enabled
[0]	rw	1'h0	UIE	Update interrupt enable 0: Update interrupt disabled. 1: Update interrupt enabled
0x10			**SR**	TIM status register
[31:18]			RSVD	
[17]	rw0c	1'h0	CC6IF	Compare 6 interrupt flag
[16]	rw0c	1'h0	CC5IF	Compare 5 interrupt flag
[15]			RSVD	
[14]			RSVD	

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[13]	rw0c	1'h0	SBIF	System Break interrupt flag This flag is set by hardware as soon as the system break input goes active. It can be cleared by software if the system break input is not active. This flag must be reset to re-start PWM operation. 0: No break event occurred. 1: An active level has been detected on the system break input. An interrupt is generated if BIE=1 in the DIER register.
[12]	rw0c	1'h0	CC4OF	Capture/Compare 4 overcapture flag
[11]	rw0c	1'h0	CC3OF	Capture/Compare 3 overcapture flag
[10]	rw0c	1'h0	CC2OF	Capture/Compare 2 overcapture flag
[9]	rw0c	1'h0	CC1OF	Capture/Compare 1 overcapture flag This flag is set by hardware only when the corresponding channel is configured in input capture mode. It is cleared by software by writing it to '0'. 0: No overcapture has been detected. 1: The counter value has been captured in CCR1 register while CC1IF flag was already set
[8]	rw0c	1'h0	B2IF	Break 2 interrupt flag This flag is set by hardware as soon as the break 2 input goes active. It can be cleared by software if the break 2 input is not active. 0: No break event occurred. 1: An active level has been detected on the break 2 input. An interrupt is generated if BIE=1 in the DIER register.
[7]	rw0c	1'h0	BIF	Break interrupt flag This flag is set by hardware as soon as the break input goes active. It can be cleared by software if the break input is not active. 0: No break event occurred. 1: An active level has been detected on the break input. An interrupt is generated if BIE=1 in the DIER register.
[6]	rw0c	1'h0	TIF	Trigger interrupt flag This flag is set by hardware on trigger event. It is set when the counter starts or stops when gated mode is selected. It is cleared by software. 0: No trigger event occurred. 1: Trigger interrupt pending.
[5]	rw0c	1'h0	COMIF	COM interrupt flag This flag is set by hardware on COM event (when Capture/compare Control bits - CCxE, CCxNE, OCxM - have been updated). It is cleared by software. 0: No COM event occurred. 1: COM interrupt pending.
[4]	rw0c	1'h0	CC4IF	Capture/Compare 4 interrupt flag
[3]	rw0c	1'h0	CC3IF	Capture/Compare 3 interrupt flag
[2]	rw0c	1'h0	CC2IF	Capture/Compare 2 interrupt flag

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	rw0c	1'h0	CC1IF	Capture/Compare 1 interrupt flag If channel CC1 is configured as output: This flag is set by hardware when the counter matches the compare value and in retriggerable one pulse mode. It is cleared by software. 0: No match. 1: The content of the counter CNT has matched the content of the CCR1 register. If channel CC1 is configured as input: This bit is set by hardware on a capture. It is cleared by software or by reading the CCR1 register. 0: No input capture occurred. 1: The counter value has been captured in CCR1 register.
[0]	rw0c	1'h0	UIF	Update interrupt flag This bit is set by hardware on an update event. It is cleared by software. 0: No update occurred 1: Update interrupt pending. This bit is set by hardware when the registers are updated: - At overflow or underflow regarding the repetition counter value (update if repetition counter = 0) and if UDIS=0 in the CR1 register. - When CNT is reinitialized by software using the UG bit in EGR register, if URS=0 and UDIS=0 in the CR1 register. - When CNT is reinitialized by a trigger event, if URS=0 and UDIS=0 in the CR1 register.
0x14			**EGR**	Event generation register
[31:9]			RSVD	
[8]	w	1'h0	B2G	Break 2 generation This bit is set by software in order to generate an event, it is automatically cleared by hardware. 0: No action 1: A break 2 event is generated. MOE bit is cleared and B2IF flag is set. Related interrupt can occur if enabled.
[7]	w	1'h0	BG	Break generation This bit is set by software in order to generate an event, it is automatically cleared by hardware. 0: No action 1: A break event is generated. MOE bit is cleared and BIF flag is set. Related interrupt or DMA transfer can occur if enabled.
[6]	w	1'h0	TG	Trigger generation This bit is set by software in order to generate an event, it is automatically cleared by hardware. 0: No action 1: The TIF flag is set in SR register. Related interrupt or DMA transfer can occur if enabled.
[5]	w	1'h0	COMG	Capture/Compare control update generation This bit can be set by software, it is automatically cleared by hardware 0: No action 1: When CCPC bit is set, it allows to update CCxE, CCxNE and OCxM bits This bit acts only on channels having a complementary output.
[4]	w	1'h0	CC4G	Capture/compare 4 generation
[3]	w	1'h0	CC3G	Capture/compare 3 generation
[2]	w	1'h0	CC2G	Capture/compare 2 generation

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	w	1'h0	CC1G	Capture/compare 1 generation This bit is set by software in order to generate an event, it is automatically cleared by hardware. 0: No action 1: A capture/compare event is generated on channel 1: If channel CC1 is configured as output: CC1IF flag is set, Corresponding interrupt or DMA request is sent if enabled. If channel CC1 is configured as input: The current value of the counter is captured in CCR1 register. The CC1IF flag is set, the corresponding interrupt or DMA request is sent if enabled. The CC1OF flag is set if the CC1IF flag was already high.
[0]	w	1'h0	UG	Update generation This bit can be set by software, it is automatically cleared by hardware. 0: No action 1: Re-initialize the counter and generates an update of the registers. The prescaler counter is cleared too (anyway the prescaler ratio is not affected). The counter is cleared if the center-aligned mode is selected or if DIR=0 (upcounting), else it takes the auto-reload value (ARR) if DIR=1 (downcounting).
0x18			**CCMR1**	TIM capture/compare mode register 1
[31:28]	rw	4'h0	OC2M	Output compare 2 mode
[27]	rw	1'h0	OC2PE	Output compare 2 preload enable
[26:25]			RSVD	
[24]	rw	1'h0	OC2CE	Output compare 2 clear enable

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[23:20]	rw	4'h0	OC1M	Output compare 1 mode These bits define the behavior of the output reference signal OC1REF from which OC1 and OC1N are derived. OC1REF is active high whereas OC1 and OC1N active level depends on CC1P and CC1NP bits. 0000: Frozen - The comparison between the output compare register CCR1 and the counter CNT has no effect on the outputs. 0001: Set channel 1 to active level on match. OC1REF signal is forced high when the counter CNT matches the capture/compare register 1 (CCR1). 0010: Set channel 1 to inactive level on match. OC1REF signal is forced low when the counter CNT matches the capture/compare register 1 (CCR1). 0011: Toggle - OC1REF toggles when CNT=CCR1. 0100: Force inactive level - OC1REF is forced low. 0101: Force active level - OC1REF is forced high. 0110: PWM mode 1 - In upcounting, channel 1 is active as long as CNT<CCR1 else inactive. In downcounting, channel 1 is inactive (OC1REF=0) as long as CNT>CCR1 else active (OC1REF=1). 0111: PWM mode 2 - In upcounting, channel 1 is inactive as long as CNT<CCR1 else active. In downcounting, channel 1 is active as long as CNT>CCR1 else inactive. 1000: Retriggerable OPM mode 1 - In up-counting mode, the channel is active until a trigger event is detected (on TRGI signal). Then, a comparison is performed as in PWM mode 1 and the channels becomes inactive again at the next update. In down-counting mode, the channel is inactive until a trigger event is detected (on TRGI signal). Then, a comparison is performed as in PWM mode 1 and the channels becomes inactive again at the next update. 1001: Retriggerable OPM mode 2 - In up-counting mode, the channel is inactive until a trigger event is detected (on TRGI signal). Then, a comparison is performed as in PWM mode 2 and the channels becomes inactive again at the next update. In down-counting mode, the channel is active until a trigger event is detected (on TRGI signal). Then, a comparison is performed as in PWM mode 1 and the channels becomes active again at the next update. 1010: Reserved, 1011: Reserved, 1100: Combined PWM mode 1 - OC1REF has the same behavior as in PWM mode 1. OC1REFC is the logical OR between OC1REF and OC2REF. 1101: Combined PWM mode 2 - OC1REF has the same behavior as in PWM mode 2. OC1REFC is the logical AND between OC1REF and OC2REF. 1110: Asymmetric PWM mode 1 - OC1REF has the same behavior as in PWM mode 1. OC1REFC outputs OC1REF when the counter is counting up, OC2REF when it is counting down. 1111: Asymmetric PWM mode 2 - OC1REF has the same behavior as in PWM mode 2. OC1REFC outputs OC1REF when the counter is counting up, OC2REF when it is counting down. These bits can not be modified as long as LOCK level 3 has been programmed and CC1S=00 (the channel is configured in output). On channels having a complementary output, this bit field is preloaded. If the CCPC bit is set in the CR2 register then the OC1M active bits take the new value from the preloaded bits only when a COM event is generated.

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[19]	rw	1'h0	OC1PE	Output compare 1 preload enable 0: Preload register on CCR1 disabled. CCR1 can be written at anytime, the new value is taken in account immediately. 1: Preload register on CCR1 enabled. Read/Write operations access the preload register. CCR1 preload value is loaded in the active register at each update event. These bits can not be modified as long as LOCK level 3 has been programmed and CC1S='00' (the channel is configured in output).
[18:17]			RSVD	
[16]	rw	1'h0	OC1CE	Output compare 1 clear enable 0: OC1Ref is not affected by the ETRF input 1: OC1Ref is cleared as soon as a High level is detected on ETRF input
[15:12]	rw	4'h0	IC2F	Input capture 2 filter
[11:10]	rw	2'h0	IC2PSC	Input capture 2 prescaler
[9:8]	rw	2'h0	CC2S	Capture/Compare 2 selection This bit-field defines the direction of the channel (input/output) as well as the used input. 00: CC2 channel is configured as output 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is working only if an internal trigger input is selected through the TS bit (SMCR register)
[7:4]	rw	4'h0	IC1F	Input capture 1 filter This bit-field defines the frequency used to sample TI1 input and the length of the digital filter applied to TI1. The digital filter is made of an event counter in which N consecutive events are needed to validate a transition on the output: 0000: No filter, sampling is done at fCLK 0001: fSAMPLING=fCLK, N=2 0010: fSAMPLING=fCLK, N=4 0011: fSAMPLING=fCLK, N=8 0100: fSAMPLING=fCLK/2, N=6 0101: fSAMPLING=fCLK/2, N=8 0110: fSAMPLING=fCLK/4, N=6 0111: fSAMPLING=fCLK/4, N=8 1000: fSAMPLING=fCLK/8, N=6 1001: fSAMPLING=fCLK/8, N=8 1010: fSAMPLING=fCLK/16, N=5 1011: fSAMPLING=fCLK/16, N=6 1100: fSAMPLING=fCLK/16, N=8 1101: fSAMPLING=fCLK/32, N=5 1110: fSAMPLING=fCLK/32, N=6 1111: fSAMPLING=fCLK/32, N=8

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[3:2]	rw	2'h0	IC1PSC	Input capture 1 prescaler This bit-field defines the ratio of the prescaler acting on CC1 input (IC1). The prescaler is reset as soon as CC1E=0 (CCER register). 00: no prescaler, capture is done each time an edge is detected on the capture input 01: capture is done once every 2 events 10: capture is done once every 4 events 11: capture is done once every 8 events
[1:0]	rw	2'h0	CC1S	Capture/Compare 1 selection This bit-field defines the direction of the channel (input/output) as well as the used input. 00: CC1 channel is configured as output 01: CC1 channel is configured as input, IC1 is mapped on TI1 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channel is configured as input, IC1 is mapped on TRC. This mode is working only if an internal trigger input is selected through TS bit (SMCR register)
0x1C			**CCMR2**	TIM capture/compare mode register 2
[31:28]	rw	4'h0	OC4M	Output compare 4 mode
[27]	rw	1'h0	OC4PE	Output compare 4 preload enable
[26:25]			RSVD	
[24]	rw	1'h0	OC4CE	Output compare 4 clear enable
[23:20]	rw	4'h0	OC3M	Output compare 3 mode
[19]	rw	1'h0	OC3PE	Output compare 3 preload enable
[18:17]			RSVD	
[16]	rw	1'h0	OC3CE	Output compare 3 clear enable
[15:12]	rw	4'h0	IC4F	Input capture 4 filter
[11:10]	rw	2'h0	IC4PSC	Input capture 4 prescaler
[9:8]	rw	2'h0	CC4S	Capture/Compare 4 selection This bit-field defines the direction of the channel (input/output) as well as the used input. 00: CC4 channel is configured as output 01: CC4 channel is configured as input, IC4 is mapped on TI4 10: CC4 channel is configured as input, IC4 is mapped on TI3 11: CC4 channel is configured as input, IC4 is mapped on TRC. This mode is working only if an internal trigger input is selected through TS bit (SMCR register)
[7:4]	rw	4'h0	IC3F	Input capture 3 filter
[3:2]	rw	2'h0	IC3PSC	Input capture 3 prescaler
[1:0]	rw	2'h0	CC3S	Capture/Compare 3 selection This bit-field defines the direction of the channel (input/output) as well as the used input. 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped on TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped on TRC. This mode is working only if an internal trigger input is selected through TS bit (SMCR register)
0x20			**CCER**	Capture/Compare enable register

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:22]			RSVD	
[21]	rw	1'h0	CC6P	Capture/Compare 6 output Polarity.
[20]	rw	1'h0	CC6E	Capture/Compare 6 output enable.
[19]			RSVD	
[18]			RSVD	
[17]	rw	1'h0	CC5P	Capture/Compare 5 output Polarity.
[16]	rw	1'h0	CC5E	Capture/Compare 5 output enable.
[15]	rw	1'h0	CC4NP	Capture/Compare 4 complementary output polarity
[14]			RSVD	
[13]	rw	1'h0	CC4P	Capture/Compare 4 output Polarity.
[12]	rw	1'h0	CC4E	Capture/Compare 4 output enable.
[11]	rw	1'h0	CC3NP	Capture/Compare 3 complementary output polarity
[10]	rw	1'h0	CC3NE	Capture/Compare 3 complementary output enable
[9]	rw	1'h0	CC3P	Capture/Compare 3 output Polarity.
[8]	rw	1'h0	CC3E	Capture/Compare 3 output enable.
[7]	rw	1'h0	CC2NP	Capture/Compare 2 complementary output polarity
[6]	rw	1'h0	CC2NE	Capture/Compare 2 complementary output enable
[5]	rw	1'h0	CC2P	Capture/Compare 2 output Polarity.
[4]	rw	1'h0	CC2E	Capture/Compare 2 output enable.
[3]	rw	1'h0	CC1NP	Capture/Compare 1 complementary output polarity CC1 channel configured as output: 0: OC1N active high. 1: OC1N active low. CC1 channel configured as input: This bit is used in conjunction with CC1P to define the polarity of TI1FP1 and TI2FP1. Refer to CC1P description. On channels having a complementary output, this bit is preloaded. If the CCPC bit is set in the CR2 register then the CC1NP active bit takes the new value from the preloaded bit only when a Commutation event is generated. This bit as well as other CCxNP is not writable as soon as LOCK level 2 or 3 has been programmed and CC1S=00 (channel configured as output).
[2]	rw	1'h0	CC1NE	Capture/Compare 1 complementary output enable 0: Off - OC1N is not active. OC1N level is then function of MOE, OSSI, OSSR, OIS1, OIS1N and CC1E bits. 1: On - OC1N signal is output on the corresponding output pin depending on MOE, OSSI, OSSR, OIS1, OIS1N and CC1E bits. On channels having a complementary output, this bit is preloaded. If the CCPC bit is set in the CR2 register then the CC1NE active bit takes the new value from the preloaded bit only when a Commutation event is generated.

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	rw	1'h0	CC1P	Capture/Compare 1 output Polarity. CC1 channel configured as output: 0: OC1 active high 1: OC1 active low CC1 channel configured as input: CC1NP/CC1P bits select TI1FP1 and TI2FP1 polarity for trigger or capture operations. 00: noninverted/rising edge. Circuit is sensitive to TIxFP1 rising edge (capture, trigger in reset, external clock or trigger mode), TIxFP1 is not inverted (trigger in gated mode, encoder mode). 01: inverted/falling edge. Circuit is sensitive to TIxFP1 falling edge (capture, trigger in reset, external clock or trigger mode), TIxFP1 is inverted (trigger in gated mode, encoder mode). 10: reserved, do not use this configuration. 11: noninverted/both edges. Circuit is sensitive to both TIxFP1 rising and falling edges (capture, trigger in reset, external clock or trigger mode), TIxFP1 is not inverted (trigger in gated mode). This configuration must not be used for encoder mode. On channels having a complementary output, this bit is preloaded. If the CCPC bit is set in the CR2 register then the CC1P active bit takes the new value from the preloaded bit only when a Commutation event is generated. This bit as well as other CCxP is not writable as soon as LOCK level 2 or 3 has been programmed.
[0]	rw	1'h0	CC1E	Capture/Compare 1 output enable CC1 channel configured as output: 0: Off - OC1 is not active. OC1 level is then function of MOE, OSSI, OSSR, OIS1, OIS1N and CC1NE bits. 1: On - OC1 signal is output on the corresponding output pin depending on MOE, OSSI, OSSR, OIS1, OIS1N and CC1NE bits. CC1 channel configured as input: This bit determines if a capture of the counter value can actually be done into the input capture/compare register 1 (CCR1) or not. 0: Capture disabled. 1: Capture enabled. On channels having a complementary output, this bit is preloaded. If the CCPC bit is set in the CR2 register then the CC1E active bit takes the new value from the preloaded bit only when a Commutation event is generated.
0x24			**CNT**	Counter
[31:0]	rw	32'h0	CNT	bit 30 to 0 is the lower bits of counter value bit 31 depends on IUFREMAP in CR1. If UIFREMAP = 1 this bit is a read-only copy of the UIF bit of the ISR register If UIFREMAP = 0 this bit is counter value bit 31
0x28			**PSC**	Prescaler
[31:16]			RSVD	
[15:0]	rw	16'h0	PSC	Prescaler value The counter clock frequency is fCLK/(PSC+1). PSC contains the value to be loaded in the active prescaler register at each update event (including when the counter is cleared through UG bit of EGR register or through trigger controller when configured in "reset mode").
0x2C			**ARR**	Auto-reload register

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	ARR	Auto-reload value ARR is the value to be loaded in the actual auto-reload register.
0x30			**RCR**	Repetition counter register
[31:16]			RSVD	
[15:0]	rw	16'h0	REP	Repetition counter value These bits allow the user to set-up the update rate of the compare registers when preload registers are enable, as well as the update interrupt generation rate, if this interrupt is enable. Each time the REP_CNT related downcounter reaches zero, an update event is generated and it restarts counting from REP value. As REP_CNT is reloaded with REP value only at the repetition update event, any write to the RCR register is not taken in account until the next repetition update event. It means in PWM mode (REP+1) corresponds to the number of PWM periods in edge-aligned mode or the number of half PWM period in center-aligned mode..
0x34			**CCR1**	Capture/Compare register 1
[31:0]	rw	32'h0	CCR1	Capture/Compare 1 value If channel CC1 is configured as output: CCR1 is the value to be loaded in the actual capture/compare 1 register (preload value).It is loaded permanently if the preload feature is not selected in the CCMR1 register (bit OC1PE). Else the preload value is copied in the active capture/compare 1 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signaled on OC1 output. If channel CC1is configured as input: CCR1 is the counter value transferred by the last input capture 1 event (IC1).
0x38			**CCR2**	Capture/Compare register 2
[31:0]	rw	32'h0	CCR2	Capture/Compare 2 value If channel CC2 is configured as output: CCR2 is the value to be loaded in the actual capture/compare 2 register (preload value).It is loaded permanently if the preload feature is not selected in the CCMR1 register (bit OC2PE). Else the preload value is copied in the active capture/compare 2 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signalled on OC2 output. If channel CC2 is configured as input: CCR2 is the counter value transferred by the last input capture 2 event (IC2).
0x3C			**CCR3**	Capture/Compare register 3
[31:0]	rw	32'h0	CCR3	Capture/Compare value If channel CC3 is configured as output: CCR3 is the value to be loaded in the actual capture/compare 3 register (preload value).It is loaded permanently if the preload feature is not selected in the CCMR2 register (bit OC3PE). Else the preload value is copied in the active capture/compare 3 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signalled on OC3 output. If channel CC3is configured as input: CCR3 is the counter value transferred by the last input capture 3 event (IC3).
0x40			**CCR4**	Capture/Compare register 4

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	CCR4	Capture/Compare value 1. if CC4 channel is configured as output (CC4S bits): CCR4 is the value to be loaded in the actual capture/compare 4 register (preload value).It is loaded permanently if the preload feature is not selected in the CCMR2 register (bit OC4PE). Else the preload value is copied in the active capture/compare 4 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signalled on OC4 output. 2. if CC4 channel is configured as input (CC4S bits in CCMR4 register): CCR4 is the counter value transferred by the last input capture 4 event (IC4).
0x44			**BDTR**	TIM break and dead-time register
[31]	rw	1'h0	OSSR	Off-state selection for Run mode This bit is used when MOE=1 on channels having a complementary output which are configured as outputs. OSSR is not implemented if no complementary output is implemented in the timer. 0: When inactive, OC/OCN outputs are disabled (the timer releases the output control, forces a Hi-Z state). 1: When inactive, OC/OCN outputs are enabled with their inactive level as soon as CCxE=1 or CCxNE=1 (the output is still controlled by the timer). This bit can not be modified as soon as the LOCK level 2 has been programmed.
[30]	rw	1'h0	OSSI	Off-state selection for Idle mode This bit is used when MOE=0 due to a break event or by a software write, on channels configured as outputs. 0: When inactive, OC/OCN outputs are disabled (the timer releases the output control, imposes a Hi-Z state). 1: When inactive, OC/OCN outputs are first forced with their inactive level then forced to their idle level after the deadtime. The timer maintains its control over the output. This bit can not be modified as soon as the LOCK level 2 has been programmed.
[29]	rw	1'h0	BK2BID	Break2 bidirectional
[28]	rw	1'h0	BKBID	Break Bidirectional 0: Break input BRK in input mode 1: Break input BRK in bidirectional mode In the bidirectional mode (BKBID bit set to 1), the break input is configured both in input mode and in open drain output mode. Any active break event asserts a low logic level on the Break input to indicate an internal break event to external devices. This bit cannot be modified as long as LOCK level 1 has been programmed (LOCK bits in BDTR register).
[27]	rw	1'h0	BK2DSRM	Break2 Disarm
[26]	rw	1'h0	BKDSRM	Break Disarm 0: Break input BRK is armed 1: Break input BRK is disarmed This bit is cleared by hardware when no break source is active. The BKDSRM bit must be set by software to release the bidirectional output control (open-drain output in Hi-Z state) and then be polled it until it is reset by hardware, indicating that the fault condition has disappeared.

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[25]	rw	1'h0	BK2P	BK2P: Break 2 polarity 0: Break input BRK2 is active low 1: Break input BRK2 is active high This bit cannot be modified as long as LOCK level 1 has been programmed.
[24]	rw	1'h0	BK2E	Break 2 enable This bit enables the complete break 2 protection. 0: Break2 function disabled 1: Break2 function enabled This bit cannot be modified as long as LOCK level 1 has been programmed.
[23:20]	rw	4'h0	BK2F	Break 2 filter This bit-field defines the frequency used to sample BRK2 input and the length of the digital filter applied to BRK2. The digital filter is made of an event counter in which N consecutive events are needed to validate a transition on the output: 0000: No filter, BRK2 acts asynchronously 0001: fSAMPLING=fCLK, N=2 0010: fSAMPLING=fCLK, N=4 0011: fSAMPLING=fCLK, N=8 0100: fSAMPLING=fCLK/2, N=6 0101: fSAMPLING=fCLK/2, N=8 0110: fSAMPLING=fCLK/4, N=6 0111: fSAMPLING=fCLK/4, N=8 1000: fSAMPLING=fCLK/8, N=6 1001: fSAMPLING=fCLK/8, N=8 1010: fSAMPLING=fCLK/16, N=5 1011: fSAMPLING=fCLK/16, N=6 1100: fSAMPLING=fCLK/16, N=8 1101: fSAMPLING=fCLK/32, N=5 1110: fSAMPLING=fCLK/32, N=6 1111: fSAMPLING=fCLK/32, N=8 This bit cannot be modified as long as LOCK level 1 has been programmed.

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[19:16]	rw	4'h0	BKF	Break filter This bit-field defines the frequency used to sample BRK input and the length of the digital filter applied to BRK. The digital filter is made of an event counter in which N consecutive events are needed to validate a transition on the output: 0000: No filter, BRK acts asynchronously 0001: fSAMPLING=fCLK, N=2 0010: fSAMPLING=fCLK, N=4 0011: fSAMPLING=fCLK, N=8 0100: fSAMPLING=fCLK/2, N=6 0101: fSAMPLING=fCLK/2, N=8 0110: fSAMPLING=fCLK/4, N=6 0111: fSAMPLING=fCLK/4, N=8 1000: fSAMPLING=fCLK/8, N=6 1001: fSAMPLING=fCLK/8, N=8 1010: fSAMPLING=fCLK/16, N=5 1011: fSAMPLING=fCLK/16, N=6 1100: fSAMPLING=fCLK/16, N=8 1101: fSAMPLING=fCLK/32, N=5 1110: fSAMPLING=fCLK/32, N=6 1111: fSAMPLING=fCLK/32, N=8 This bit cannot be modified as long as LOCK level 1 has been programmed.
[15]	rw	1'h0	MOE	Main output enable This bit is cleared asynchronously by hardware as soon as one of the break inputs is active (BRK or BRK2). It is set by software or automatically depending on the AOE bit. It is acting only on the channels which are configured in output. 0: In response to a break 2 event. OC and OCN outputs are disabled In response to a break event or if MOE is written to 0: OC and OCN outputs are disabled or forced to idle state depending on the OSSI bit. 1: OC and OCN outputs are enabled if their respective enable bits are set (CCxE, CCxNE in CCER register).
[14]	rw	1'h0	AOE	Automatic output enable 0: MOE can be set only by software 1: MOE can be set by software or automatically at the next update event (if none of the break inputs BRK and BRK2 is active) This bit cannot be modified as long as LOCK level 1 has been programmed.
[13]	rw	1'h0	BKP	Break polarity 0: Break input BRK is active low 1: Break input BRK is active high This bit cannot be modified as long as LOCK level 1 has been programmed.
[12]	rw	1'h0	BKE	Break enable This bit enables the complete break protection. 0: Break function disabled 1: Break function enabled This bit cannot be modified as long as LOCK level 1 has been programmed.
[11]	rw	1'h0	DTPSC	Dead-time prescaler This bit-field enables dead-time prescaler. 0: dead-time is tCLK*(DTG+1) if DTG is not zero 1: dead-time is tCLK*(DTG+1)*16 if DTG is not zero This bit cannot be modified as long as LOCK level 1 has been programmed.

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[10]			RSVD	
[9:0]	rw	10'h0	DTG	Dead-time generator setup This bit-field, together with DTPSC, defines the duration of the dead-time inserted between the complementary outputs. If DTG=0, dead-time is disabled. Example if tCLK=8.33ns (120MHz), dead-time possible values are: 16.67ns to 8533.33 ns by 8.33 ns steps if DTPSC=0, 266.67ns to 136.53 us by 133.33 ns steps if DTPSC=1 This bit cannot be modified as long as LOCK level 1 has been programmed.
0x54			**CCMR3**	TIM capture/compare mode register 3
[31:28]	rw	4'h0	OC6M	Output compare 6 mode
[27]	rw	1'h0	OC6PE	Output compare 6 preload enable
[26:25]			RSVD	
[24]	rw	1'h0	OC6CE	Output compare 6 clear enable
[23:20]	rw	4'h0	OC5M	Output compare 5 mode
[19]	rw	1'h0	OC5PE	Output compare 5 preload enable
[18:17]			RSVD	
[16]	rw	1'h0	OC5CE	Output compare 5 clear enable
[15]	rw	1'h0	GC5C3	Group Channel 5 and Channel 3 Distortion on Channel 3 output: 0: No effect of OC5REF on OC3REFC 1: OC3REFC is the logical AND of OC3REFC and OC5REF This bit can either have immediate effect or be preloaded and taken into account after an update event (if preload feature is selected in TIMxCCMR2).
[14]	rw	1'h0	GC5C2	Group Channel 5 and Channel 2 Distortion on Channel 2 output: 0: No effect of OC5REF on OC2REFC 1: OC2REFC is the logical AND of OC2REFC and OC5REF This bit can either have immediate effect or be preloaded and taken into account after an update event (if preload feature is selected in TIMxCCMR1).
[13]	rw	1'h0	GC5C1	Group Channel 5 and Channel 1 Distortion on Channel 1 output: 0: No effect of OC5REF on OC1REFC5 1: OC1REFC is the logical AND of OC1REFC and OC5REF This bit can either have immediate effect or be preloaded and taken into account after an update event (if preload feature is selected in TIMxCCMR1).
[12:0]			RSVD	
0x58			**CCR5**	Capture/Compare register 5
[31:0]	rw	32'h0	CCR5	Capture/Compare 5 value CCR5 is the value to be loaded in the actual capture/compare 5 register (preload value). It is loaded permanently if the preload feature is not selected in the CCMR3 register (bit OC5PE). Else the preload value is copied in the active capture/compare 5 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signaled on OC5 output.
0x5C			**CCR6**	Capture/Compare register 6

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	CCR6	Capture/Compare 6 value CCR6 is the value to be loaded in the actual capture/compare 6 register (preload value). It is loaded permanently if the preload feature is not selected in the CCMR3 register (bit OC6PE). Else the preload value is copied in the active capture/compare 6 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signaled on OC6 output.
0x60			**AF1**	Alternate function option register
[31:30]	rw	2'h0	LOCK	Lock configuration These bits offer a write protection against software errors. 00: LOCK OFF - No bit is write protected. 01: LOCK Level 1 = OISx and OISxN bits in CR2 register, BK2BID, BKBID, BK2DSRM, BKDSRM, BK2P, BK2E, BK2F[3:0], BKF[3:0], AOE, BKP, BKE, OSSI, OSSR, DTPSC and DTG bits in BDTR register, AF1 register and AF2 register can no longer be written. 10: LOCK Level 2 = LOCK Level 1 + CC Polarity bits (CCxP/CCxNP bits in CCER register, as long as the related channel is configured in output through the CCxS bits) as well as OSSR and OSSI bits can no longer be written. 11: LOCK Level 3 = LOCK Level 2 + CC Control bits (OCxM and OCxPE bits in CCMRx registers, as long as the related channel is configured in output through the CCxS bits) can no longer be written. The LOCK bits can be written to non-zero only once after reset.
[29:16]			RSVD	
[15:14]	rw	2'h0	ETRSEL	ETR source selection 00: ETR input is connected to I/O 01: LPCOMP output1 (if LPCOMP integrated) 10: LPCOMP output2 (if LPCOMP integrated) 11: ETR input is connected to I/O This bit cannot be modified as long as LOCK level 1 has been programmed.
[13:12]			RSVD	
[11]	rw	1'h0	BKCMP2P	BRK LPCOMP output2 polarity This bit selects the LPCOMP output2 sensitivity (if LPCOMP integrated). It must be programmed together with the BKP polarity bit. 0: LPCOMP output2 is active high 1: LPCOMP output2 is active low This bit cannot be modified as long as LOCK level 1 has been programmed.
[10]	rw	1'h0	BKCMP1P	BRK LPCOMP output1 polarity This bit selects the LPCOMP output1 sensitivity (if LPCOMP integrated). It must be programmed together with the BKP polarity bit. 0: LPCOMP output1 is active high 1: LPCOMP output1 is active low This bit cannot be modified as long as LOCK level 1 has been programmed.
[9]	rw	1'h0	BKINP	BRK BKIN input polarity This bit selects the BKIN input sensitivity. It must be programmed together with the BKP polarity bit. 0: BKIN input is active high 1: BKIN input is active low This bit cannot be modified as long as LOCK level 1 has been programmed.
[8:3]			RSVD	

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[2]	rw	1'h0	BKCMP2E	BRK LPCOMP output2 enable This bit enables the LPCOMP output2 (if LPCOMP integrated) for the timer's BRK input. LPCOMP output2 is 'ORed' with the other BRK sources. 0: LPCOMP output2 disabled 1: LPCOMP output2 enabled This bit cannot be modified as long as LOCK level 1 has been programmed.
[1]	rw	1'h0	BKCMP1E	BRK LPCOMP output1 enable This bit enables the LPCOMP output1 (if LPCOMP integrated) for the timer's BRK input. LPCOMP output1 is 'ORed' with the other BRK sources. 0: LPCOMP output1 disabled 1: LPCOMP output1 enabled This bit cannot be modified as long as LOCK level 1 has been programmed.
[0]	rw	1'h0	BKINE	BRK BKIN input enable This bit enables the BKIN input. BKIN input is 'Ored' with the other BRK sources. 0: BKIN input disabled 1: BKIN input enabled This bit cannot be modified as long as LOCK level 1 has been programmed.
0x64			**AF2**	Alternate function option register 2
[31:12]			RSVD	
[11]	rw	1'h0	BK2CMP2P	BRK2 LPCOMP output2 polarity This bit selects the LPCOMP output2 sensitivity (if LPCOMP integrated). It must be programmed together with the BK2P polarity bit. 0: LPCOMP output2 is active high 1: LPCOMP output2 is active low This bit cannot be modified as long as LOCK level 1 has been programmed.
[10]	rw	1'h0	BK2CMP1P	BRK2 LPCOMP output1 polarity This bit selects the LPCOMP output1 sensitivity (if LPCOMP integrated). It must be programmed together with the BK2P polarity bit. 0: LPCOMP output1 is active high 1: LPCOMP output1 is active low This bit cannot be modified as long as LOCK level 1 has been programmed.
[9]	rw	1'h0	BK2INP	BRK2 BKIN2 input polarity This bit selects the BKIN2 input sensitivity. It must be programmed together with the BK2P polarity bit. 0: BKIN2 input is active low 1: BKIN2 input is active high This bit cannot be modified as long as LOCK level 1 has been programmed.
[8:3]			RSVD	
[2]	rw	1'h0	BK2CMP2E	BRK2 LPCOMP output2 enable This bit enables the LPCOMP output2 (if LPCOMP integrated) for the timer's BRK2 input. LPCOMP output2 is 'ORed' with the other BRK2 sources. 0: LPCOMP output2 disabled 1: LPCOMP output2 enabled This bit cannot be modified as long as LOCK level 1 has been programmed.

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表 9-1: ATIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	rw	1'h0	BK2CMP1E	BRK2 LPCOMP output1 enable This bit enables the LPCOMP output1 (if LPCOMP integrated) for the timer's BRK2 input. LPCOMP output1 is 'ORed' with the other BRK2 sources. 0: LPCOMP output1 disabled 1: LPCOMP output1 enabled This bit cannot be modified as long as LOCK level 1 has been programmed.
[0]	rw	1'h0	BK2INE	BRK2 BKIN input enable This bit enables the BKIN2 input. BKIN2 input is 'Ored' with the other BRK2 sources. 0: BKIN2 input disabled 1: BKIN2 input enabled This bit cannot be modified as long as LOCK level 1 has been programmed.

9.2 BTIM

HPSYS 有 2 个 BTIM。

BTIM1 的工作时钟是 pclk_hpsys，应注意在系统动态调节频率时计数可能受到影响。

BTIM2 的工作时钟是 clk_peri_hpsys，独立于系统时钟，在系统动态调节频率时计数不受影响。

9.2.1 简介

BTIM (Basic Timer) 基于一个 32 比特递增计数器，可实现计时功能。计数时钟为系统 PCLK 或级联输入信号，并可进行 1~65536 倍的预分频。计时结果可以产生中断、DMA 请求或 PTC 触发。BTIM 包含主从模式接口，可以进行多级级联，实现多级计数或同步触发等功能。

9.2.2 主要特性

- 32 位递增自动重装载计数器
- 16 位可编程预分频器，计数器时钟频率的分频系数为 1~65536 之间的任意数值
- 支持单笔计数模式 (OPM)，计数完成后自动停止计数器
- 主从模式
  - 支持与其它定时器互连，可在作为主设备产生控制信号的同时，作为从设备被外部输入或其它主设备控制
  - 控制模式包括复位、触发、门控等
  - 支持多定时器同步启动、复位等
- 计数器溢出或初始化时产生中断/DMA

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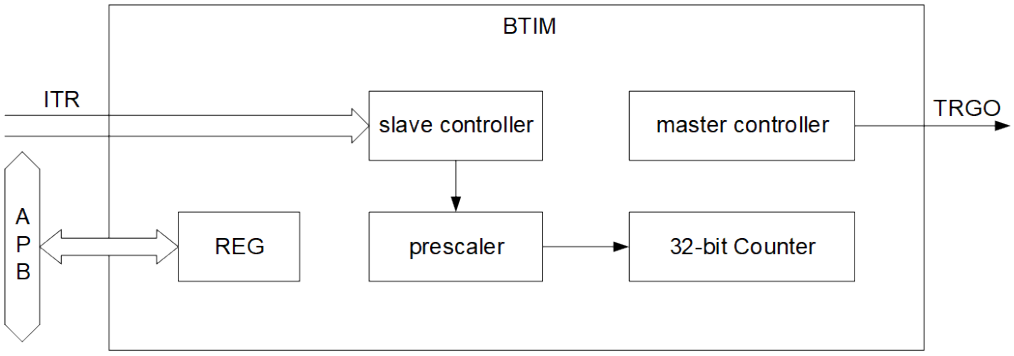


图 9-7: BTIM 结构图

9.2.3 BTIM 功能描述

9.2.3.1 计数器

BTIM 的各项功能均基于一个 32 比特的计数器。计数器基于事件计数，最基本的事件是一个 PCLK 时钟的翻转。根据不同配置，其它计数事件包括外部输入的翻转、其它定时器的输出翻转等。

计数事件经过预分频处理才会真正进入计数器。预分频的次数介于 1 到 65536 之间 (PSC+1)，即仅当发生了 (PSC+1) 次计数事件，计数器的值才真正改变一次。

计数器固定为递增计数模式，计数器从 0 计数到自动重载值 ARR，然后重新从 0 开始计数并产生计数器上溢事件。计数值可以通过 CNT 读出。

9.2.3.2 更新事件 (UEV)

更新事件用于标志一个计数单元的结束。最基本的更新事件产生于每次计数器上溢时。软件将 EGR_UG 置 1 时，也将产生更新事件。更新事件可以产生中断、DMA 请求以及 PTC 触发，是定时器最基本的一项通知功能。

通过软件将 CR1_UDIS 置 1 可禁止产生更新事件。这可避免向预装载寄存器写入新值时更新影子寄存器。在 UDIS 位写入 0 之前不会产生任何更新事件。

如果 CR1_URS（更新请求选择）已置 1，则将 EGR_UG 置 1 会生成更新事件，但不会将 UIF 标志置 1（因此，不会发送任何中断或 DMA 请求）。这样一来，如果在发生捕获事件时将计数器清零，将不会同时产生更新中断和捕获中断。

发生更新事件时，将重新装载 ARR 以及 PSC 寄存器，且将更新标志 SR_UIF 置 1（CR1_URS=0 时）。该功能可以保证修改这些计数器的基本参数不影响当前计数单元，在下一个计数周期才生效。

9.2.3.3 影子寄存器

对 ARR 以及 PSC 寄存器的修改不会直接体现在当前计数单元中，而是等到更新事件发生时才真正更新进去。在更新事件发生前，计数器真正使用的是影子寄存器中的值。这样即使在计数中动态改变这些寄存器的值，也不会影响到当前计数单元的完整性。

如果 CR1_APRE 为 0，ARR 寄存器将在配置后实时生效，不用等到更新事件发生。

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9.2.3.4 主从模式

定时器可同时处于主模式与从模式。主模式是指该定时器可以输出 TRGO 信号至芯片上其它定时器的 ITR 输入，用于控制其它定时器的计数行为。从模式是指该定时器的计数行为受其它定时器输出至该定时器的 ITR 信号控制。

多个定时器可通过主从模式实现定时器同步，以实现多级分频、同时启动、门控计数等功能。

主模式可在不同事件发生时输出 TRGO 信号，如更新、使能等，由 CR2_MMS 选择。

从模式可以通过 SMCR_SMS 选择计数器复位、触发启动、计数事件等行为，同时可以选择门控模式。从模式依赖的触发信号 TRGI 和门控信号可在 ITR 中独立选择，并可选择门控信号极性。

定时器处于复位从模式 (SMCR_SMS=001) 时，当 TRGI 发生变化时，计数器及其预分频器重新初始化。如果 CR1_URS 为 0，则会生成更新事件 UEV，ARR 被更新。

定时器处于触发从模式 (SMCR_SMS=010) 时，软件不需配置 CR1_CEN 开启计数，而是在 TRGI 上升沿自动启动计数器。定时器处于复位触发从模式 (SMCR_SMS=011) 时，在 TRGI 的上升沿复位计数器并自动重新开启。

定时器处于外部时钟从模式 (SMCR_SMS=100) 时，计数事件修改为 TRGI 的上升沿，仅当 TRGI 发生翻转时才进行计数。

定时器开启门控从模式 (SMCR_GM=1) 时，当 TRGI 满足高电平或低电平要求 (SMCR_GTP) 时才进行计数，否则计数器不变。

9.2.3.5 单脉冲模式

将 CR1_OPM 写 1 可以使能单脉冲模式。该模式下计数器启动以后一旦发生更新事件，就会自动停止计数。该模式可以用于单次计数。

9.2.3.6 定时器同步

多个定时器可通过主从模式连接在一起，实现定时器同步，以完成多级分频、同时启动、门控计数等功能。

将主模式定时器的 TRGO 设置为更新事件，连接至另一个设置为外部时钟从模式的定时器，可以实现定时器级联计数。此时主模式定时器相当于从模式定时器的预分频，计数总位宽等于两个定时器各自的位宽相加。

将主模式定时器的 TRGO 设置为计数使能，并设置从模式为触发从模式，同时连接至另一个设置为触发从模式的定时器，可以实现多个定时器同步触发启动，从而对齐多个定时器的开启时机。该场景下主模式定时器还需将 SMCR_MSM 设为 1。

9.2.3.7 通知机制

BTIM 能够产生中断、DMA 请求、PTC 触发等多种通知机制。能够触发通知的事件为更新事件。DIER 寄存器可以控制各种事件是否产生中断和 DMA 请求。各事件状态可在 SR 寄存器中查询。

9.2.4 BTIM 寄存器

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表 9-2: BTIM 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**CR1**	TIM control register 1
[31:8]			RSVD	
[7]	rw	1'h0	ARPE	Auto-reload preload enable 0: ARR register is not buffered 1: ARR register is buffered
[6:4]			RSVD	
[3]	rw	1'h0	OPM	One-pulse mode 0: Counter is not stopped at update event 1: Counter stops counting at the next update event (clearing the bit CEN)
[2]	rw	1'h0	URS	Update request source This bit is set and cleared by software to select the UEV event sources. 0: Any of the following events generate an update interrupt or DMA request if enabled. These events can be: Counter overflow Setting the UG bit Update generation through the slave mode controller 1: Only counter overflow generates an update interrupt or DMA request if enabled.
[1]	rw	1'h0	UDIS	Update disable This bit is set and cleared by software to enable/disable UEV event generation. 0: UEV enabled. The Update (UEV) event is generated by one of the following events: Counter overflow Setting the UG bit Update generation through the slave mode controller Buffered registers are then loaded with their preload values. 1: UEV disabled. The Update event is not generated, shadow registers keep their value (ARR, PSC). However the counter and the prescaler are reinitialized if the UG bit is set or if a hardware reset is received from the slave mode controller.
[0]	rw	1'h0	CEN	Counter enable 0: Counter disabled 1: Counter enabled Note: Gated mode can work only if the CEN bit has been previously set by software. However trigger mode can set the CEN bit automatically by hardware. CEN is cleared automatically in one-pulse mode, when an update event occurs.
0x04			**CR2**	TIM control register 2
[31:6]			RSVD	

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表 9-2: BTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[5:4]	rw	2'h0	MMS	Master mode selection These bits allow to select the information to be sent in master mode to slave timers for synchronization (TRGO). The combination is as follows: 00: Reset:the UG bit from the EGR register is used as trigger output (TRGO). If the reset is generated by the trigger input (slave mode controller configured in reset mode) then the signal on TRGO is delayed compared to the actual reset. 01: Enable :the Counter enable signal, CNT_EN, is used as trigger output (TRGO). It is useful to start several timers at the same time or to control a window in which a slave timer is enabled. The Counter Enable signal is generated by a logic OR between CEN control bit and the trigger input when configured in gated mode. When the Counter Enable signal is controlled by the trigger input, there is a delay on TRGO, except if the master/slave mode is selected (see the MSM bit description in SMCR register). 10: Update:The update event is selected as trigger output (TRGO). For instance a master timer can then be used as a prescaler for a slave timer. 11: Gating:The delayed gating trigger is selected as trigger output (TRGO).
[3:0]			RSVD	
0x08			**SMCR**	TIM slave mode control register
[31:24]			RSVD	
[23]	rw	1'h0	GM	Gated Mode. The counter clock is enabled when the selected trigger input (TRGI) is active (according to gating trigger polarity). The counter stops (but is not reset) as soon as the trigger becomes inactive. Both start and stop of the counter are controlled. Gated mode and slave mode can be enabled simutanuously with different trigger selection.
[22]	rw	1'h0	GTP	Gating trigger polarity invert 0: active at high level 1: active at low level
[21:20]	rw	2'h0	GTS	Gating trigger selection in gated mode This bit-field selects the trigger input to be used to enable the counter gating. 00: Internal Trigger 0 (ITR0) 01: Internal Trigger 1 (ITR1) 10: Internal Trigger 2 (ITR2) 11: Internal Trigger 3 (ITR3)
[19]			RSVD	
[18:16]	rw	3'h0	SMS	Slave mode selection When external signals are selected the active edge of the trigger signal (TRGI) is linked to the polarity selected on the external input. 000: Slave mode disabled. 001: Reset Mode - Rising edge of the selected trigger input (TRGI) reinitializes the counter and generates an update of the registers. 010: Trigger Mode - The counter starts at a rising edge of the trigger TRGI (but it is not reset). Only the start of the counter is controlled. 011: Combined reset + trigger mode - Rising edge of the selected trigger input (TRGI) reinitializes the counter, generates an update of the registers and starts the counter. 100: External Clock Mode - Rising edges of the selected trigger (TRGI) clock the counter.
[15:8]			RSVD	

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表 9-2: BTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7]	rw	1'h0	MSM	Master/Slave mode. This bit should be asserted on master timer if synchronization if needed. 0: No action 1: The effect of an event on the trigger input (TRGI) is delayed to allow a perfect synchronization between the current timer and its slaves (through TRGO). It is useful if we want to synchronize several timers on a single external event.
[6]			RSVD	
[5:4]	rw	2'h0	TS	Trigger selection This bit-field selects the trigger input to be used to synchronize the counter. 00: Internal Trigger 0 (ITR0) 01: Internal Trigger 1 (ITR1) 10: Internal Trigger 2 (ITR2) 11: Internal Trigger 3 (ITR3)
[3:0]			RSVD	
0x0C			**DIER**	TIM DMA/Interrupt enable register
[31:9]			RSVD	
[8]	rw	1'h0	UDE	Update DMA request enable 0: Update DMA request disabled. 1: Update DMA request enabled
[7:1]			RSVD	
[0]	rw	1'h0	UIE	Update interrupt enable 0: Update interrupt disabled. 1: Update interrupt enabled
0x10			**SR**	TIM status register
[31:1]			RSVD	
[0]	rw0c	1'h0	UIF	Update interrupt flag This bit is set by hardware on an update event. It is cleared by software. 0: No update occurred 1: Update interrupt pending. This bit is set by hardware when the registers are updated: At overflow and if UDIS=0 in the CR1 register. When CNT is reinitialized by software using the UG bit in EGR register, if URS=0 and UDIS=0 in the CR1 register. When CNT is reinitialized by a trigger event (refer to the synchro control register description), if URS=0 and UDIS=0 in the CR1 register.
0x14			**EGR**	Event generation register
[31:1]			RSVD	
[0]	w1s	1'h0	UG	Update generation This bit can be set by software, it is automatically cleared by hardware. 0: No action 1: Re-initialize the counter and generates an update of the registers. Note that the prescaler counter is cleared too (anyway the prescaler ratio is not affected). The counter is cleared if the center-aligned mode is selected or if DIR=0 (upcounting), else it takes the auto-reload value (ARR) if DIR=1 (downcounting).
0x24			**CNT**	Counter
[31:0]	rw	32'h0	CNT	counter value
0x28			**PSC**	Prescaler
[31:16]			RSVD	

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表 9-2: BTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[15:0]	rw	16'h0	PSC	Prescaler value The counter clock frequency is equal to fCLK / (PSC[15:0] + 1). PSC contains the value to be loaded in the active prescaler register at each update event (including when the counter is cleared through UG bit of EGR register or through trigger controller when configured in "reset mode").
0x2C			**ARR**	Auto-reload register
[31:0]	rw	32'h0	ARR	Auto-reload value ARR is the value to be loaded in the actual auto-reload register. The counter is blocked while the auto-reload value is null.

9.3 GPTIM

HPSYS 有 2 个 GPTIM。

GPTIM1 的工作时钟是 pclk_hpsys，应注意在系统动态调节频率时计数可能受到影响。

GPTIM2 的工作时钟是 clk_peri_hpsys，独立于系统时钟，在系统动态调节频率时计数不受影响。

9.3.1 简介

GPTIM (General Purpose Timer) 基于一个 16 比特计数器，可实现计时、测量输入信号的脉冲长度 (输入捕获) 或者产生输出波形 (输出比较和 PWM) 等功能。计数器本身可以进行递增、递减或者递增/递减计数，计数时钟可选系统 PCLK，IO 输入信号或级联输入信号，并可进行 1~65536 倍的预分频。GPTIM 共有 4 个通道，可以分别独立配置为输入捕获或输出模式。计数、输入捕获和输出比较的结果可以产生中断、DMA 请求或 PTC 触发。GPTIM 包含主从模式接口，可以进行多级级联，实现多级计数或同步触发等功能。

9.3.2 主要特性

- 16 位递增、递减、递增/递减自动重装载计数器，最大计数 65535
- 16 位可编程 (可以实时修改) 预分频器，计数器时钟频率的分频系数为 1~65536 之间的任意数值
- 8 位可配置重复计数
- 支持单笔计数模式 (OPM)，当重复计数完成后自动停止计数器
- 4 个独立通道，可分别配置为输入或输出模式
- 输入模式
  - 上升沿/下降沿捕获
  - PWM 脉宽和周期捕获 (需占用两个通道)
  - 可选 4 个输入端口之一或 1 个外部触发端口，支持防抖动滤波和预降频
- 输出模式
  - 强制输出高/低电平
  - 计数到比较值时输出高/低/翻转电平
  - PWM 输出，可配脉宽和周期
  - 多通道 PWM 组合输出，可产生有相互关系的多路 PWM
  - 单脉冲/重触发单脉冲模式输出
- 主从模式

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  - 支持多定时器互连，可在作为主设备产生控制信号的同时，作为从设备被外部输入或其它主设备控制
  - 控制模式包括复位、触发、门控等
  - 支持多定时器同步启动、复位等
- 编码模式输入，控制计数器递增/递减计数
- 如下事件发生时产生中断/DMA 请求/PTC 触发：
  - 更新：计数器递增溢出/递减溢出，计数器初始化 (通过软件或者内部/外部触发)
  - 触发事件 (计数器启动、停止、初始化或者由内部/外部触发计数)
  - 输入捕获
  - 输出比较

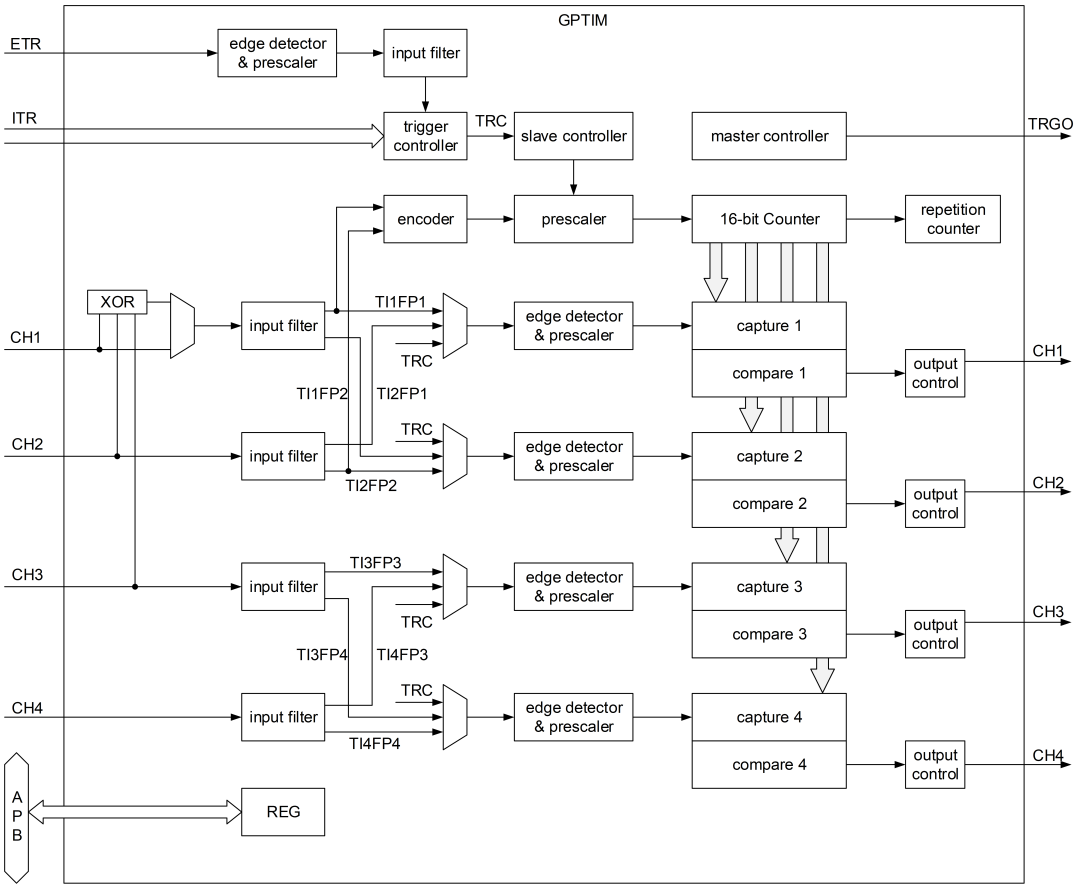


图 9-8: GPTIM 结构图

9.3.3 GPTIM 功能描述

9.3.3.1 计数器

GPTIM 的各项功能均基于一个 16 比特的计数器。计数器基于事件计数，最基本的事件是一个 PCLK 时钟的翻转。根据不同配置，其它计数事件包括外部输入的翻转、其它定时器的输出翻转、正交编码器接口解码输出等。

计数事件经过预分频处理才会真正进入计数器。预分频的次数介于 1 到 65536 之间 (PSC+1)，即仅当发生了 (PSC+1) 次计数事件，计数器的值才真正改变一次。

计数器共有三种计数模式：递增，递减以及中心对齐。在递增计数模式下 (CR1_CMS=0 且 CR1_DIR=0)，计数器

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从 0 计数到自动重载值 ARR，然后重新从 0 开始计数并产生计数器上溢事件。在递减计数模式下 (CR1_CMS=0 且 CR1_DIR=1)，计数器从 ARR 开始递减计数到 0，然后重新从 ARR 开始计数并产生计数器下溢事件。在中心对齐模式下 (CR1_CMS 不为 0)，计数器从 0 开始计数到 ARR-1，产生计数器上溢事件，然后从 ARR 开始向下计数到 1 并产生计数器下溢事件，之后从 0 开始重新计数。

计数值可以通过 CNT 读出。计数的方向可以从 CR1_DIR 读出。

9.3.3.2 更新事件 (UEV)

更新事件用于标志一个计数单元的结束。最基本的更新事件产生于每次计数器上溢或下溢时 (未开启重复计数时)。软件将 EGR_UG 置 1 时，也将产生更新事件。更新事件可以产生中断、DMA 请求以及 PTC 触发，是定时器最基本的一项通知功能。

通过软件将 CR1_UDIS 置 1 可禁止产生更新事件。这可避免向预装载寄存器写入新值时更新影子寄存器。在 UDIS 位写入 0 之前不会产生任何更新事件。

如果 CR1_URS（更新请求选择）已置 1，则将 EGR_UG 置 1 会生成更新事件，但不会将 UIF 标志置 1（因此，不会发送任何中断或 DMA 请求）。这样一来，如果在发生捕获事件时将计数器清零，将不会同时产生更新中断和捕获中断。

发生更新事件时，将重新装载 RCR，ARR 以及 PSC 寄存器，且将更新标志 SR_UIF 置 1（CR1_URS=0 时）。该功能可以保证修改这些计数器的基本参数不影响当前计数单元，在下一个计数周期才生效。

9.3.3.3 重复计数

如果配置了重复计数器 (RCR>0)，每次计数器上溢或下溢时重复计数器会递减，并仅当重复计数器为 0 时才产生更新事件。更新事件发生时，重复计数器会重新装载 RCR 的值。

重复计数器的当前值不能读出。

9.3.3.4 影子寄存器

对 RCR，ARR 以及 PSC 寄存器的修改不会直接体现在当前计数单元中，而是等到更新事件发生时才真正更新进去。在更新事件发生前，计数器真正使用的是影子寄存器中的值。这样即使在计数中动态改变这些寄存器的值，也不会影响到当前计数单元的完整性，对于 PWM 输出等应用场景很有意义。

如果 CR1_APRE 为 0，ARR 寄存器将在配置后实时生效，不用等到更新事件发生。

输出比较寄存器 CCRx 也有影子寄存器。当 CCMRx_OCxPE 为 0 时，配置的 CCRx 会立即生效，否则要等到更新事件发生时才生效。

9.3.3.5 主从模式

定时器可同时处于主模式与从模式。主模式是指该定时器可以输出 TRGO 信号至芯片上其它定时器的 ITR 输入，用于控制其它定时器的计数行为。从模式是指该定时器的计数行为受外部输入 ETR，其它定时器输出至该定时器的 ITR 信号，或定时器的通道输入 CHx 的控制。

多个定时器可通过主从模式实现定时器同步，以实现多级分频、同时启动、门控计数等功能。

主模式可在不同事件发生时输出 TRGO 信号，如更新、使能、输入捕获、输出比较等，由 CR2_MMS 选择。

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从模式可以选择计数器复位、触发启动、计数使能、计数事件等行为，由 SMCR_SMS 选择。从模式依赖的触发信号 TRGI 可灵活配置，可以在 ETR，ITR 以及通道输入中选择，并可选择信号极性，进行预分频、滤波等操作。

- 定时器处于复位从模式 (SMCR_SMS=0100) 时，当 TRGI 发生变化时，计数器及其预分频器重新初始化。如果 CR1_URS 为 0，则会生成更新事件 UEV，然后所有预装载寄存器 ARR 和 CCRx 都将更新。
- 定时器处于门控从模式 (SMCR_SMS=0101) 时，当 TRGI 满足高电平或低电平要求时才进行计数，否则计数器不变。
- 定时器处于触发从模式 (SMCR_SMS=0110) 时，软件不需配置 CR1_CEN 开启计数，而是当 TRGI 满足特定触发要求时自动启动计数器。
- 定时器处于外部时钟从模式 (SMCR_SMS=0111) 时，计数事件修改为 TRGI 的上升沿，仅当 TRGI 发生翻转时才进行计数。
- 定时器处于复位触发从模式 (SMCR_SMS=1000) 时，TRGI 满足特定触发要求时复位计数器并自动重新开启。

9.3.3.6 通道输入输出

定时器的部分通道可以独立配置为输入捕获模式 (CCMRx_CCxS!=0) 或输出模式 (CCMRx_CCxS=0)。

在输入捕获模式下，通道在对应的触发信号有效时，将计数器的值记录进 CCRx，并产生中断等通知信号。该触发信号可在 ETR，ITR 以及通道输入 CHx 中选择，并可选择信号极性，进行预分频、滤波等操作。通道产生的通知信号包括中断、DMA 请求、PTC 触发等。输入捕获模式可实现记录外部信号改变的时刻、测量 PWM 周期和占空比等功能。

在输出模式下，通道将比较计数器的值与 CCRx 的大小，在通道输出 CHx/CHxN 上产生固定电平，或产生基于本通道以及其它通道比较结果的 PWM 输出信号，并产生中断等通知信号。产生 PWM 信号的脉冲个数、频率、占空比、相位等参数均可调节。多个通道还可以联合产生特定关系的 PWM 组合。通道产生的通知信号包括中断、DMA 请求、PTC 触发等。

9.3.3.7 输入捕获模式

在输入捕获模式下，当通道相应的触发信号检测到跳变沿后，将使用 CCRx 来锁存计数器的值。发生捕获事件时，会将相应的 SR_CCxIF 标志置 1，并可发送中断、DMA 请求（如果已使能）或 PTC 触发信号。如果发生捕获事件时 SR_CCxIF 标志已处于高位，则会将重复捕获标志 SR_CCxOF 置 1。可通过软件将 SR_CCxIF 清零，方法是向 SR_CCxIF 写入 0，或读取存储在 CCRx 中的已捕获数据。向 SR_CCxOF 写入 0 后会将其清零。

以下示例说明了如何在 CH1 输入出现上升沿时将计数器的值捕获到 CCR1 中，具体操作步骤如下：

1. 选择有效输入：通道 1 要连接到 CH1 输入，因此向 CCMR1_CC1S 写入 01。
2. 根据连接到定时器的信号，对所需的输入滤波带宽进行配置。
   假设 CH1 信号边沿变化时，最多在 5 个 PCLK 周期内发生抖动，需将滤波带宽设置为大于 5 个 PCLK 周期。将 CCMR1_IC1F 设置为 0011(0x3)，则在检测到连续 8 个采样点（以 PCLK 频率采样）均为新电平后，可以确认 CH1 的跳变沿。
3. 将 CCER_CC1P 和 CCER_CC1NP 写 0，选择 CH1 上的有效转换边沿为上升沿。
4. 对输入预分频器进行编程。
   在本例中我们希望每次有效转换时都执行捕获操作，因此禁用预分频器（CCMR1_IC1PS 写 00）。
5. CCER_CC1E 置 1，使能通道 1，允许将计数器的值捕获到 CCR1 中。

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6. 如果需要，可将 DIER_CC1IE 置 1 来使能相关中断请求，或将 DIER_CC1DE 置 1 来使能 DMA 请求。

配置完成后，通道将在 CH1 输入出现上升沿时执行下列操作：

1. CCR1 寄存器记录计数器的值。
2. SR_CCxIF 标志置 1（中断标志）。如果至少发生了两次连续捕获，但 SR_CCxIF 未被清零，这样 SR_CCxOF 捕获溢出标志会被置 1。
3. 根据 CCER_CC1IE 生成中断。
4. 根据 DIER_CC1DE 生成 DMA 请求。

要处理重复捕获，建议在读出 SR_CCxOF 之前读取数据。这样可避免丢失在读取 SR_CCxOF 之后与读取数据之前可能出现的重复捕获信息。

通过软件将 EGR_CCxG 置 1 可立即产生一次捕获，并生成通道捕获中断和 DMA 请求。

9.3.3.8 PWM 输入捕获

PWM 输入捕获是输入捕获的一种扩展应用，可用于测量 PWM 输入信号的周期和占空比。为实现该功能，需要将两个通道都配置为输入捕获模式，触发信号分别映射成输入 PWM 的正边沿和负边沿，并开启计数器复位的从模式。

以下示例说明了如何用通道 1 和通道 2 测量从 CH1 输入的 PWM 的周期和占空比，具体操作步骤如下：

1. 选择通道 1 的有效输入为 CH1 输入，因此向 CCMR1_CC1S 写入 01。
2. 选择通道 1 输入信号的有效极性（用于在 CCR1 中捕获和计数器清零），将 CCER_CC1P 和 CCER_CC1NP 写 0，选择 CH1 上的有效转换边沿为上升沿。
3. 选择通道 2 的有效输入也为 CH1 输入，向 CCMR1_CC2S 写入 10(0x2)。
4. 选择通道 2 输入信号的有效极性（用于 CCR2 捕获），将 CCER_CC2P 写 1，CCER_CC1NP 写 0，选择 CH1 上的有效转换边沿为下降沿。
5. 设置从模式控制信号为 CH1，向 SMCR_TS 写入 101(0x5)，选择 TI1FP1。
6. 将从模式控制器配置为复位模式，向 SMCR_SMS 写入 0100(0x4)。
7. 使能通道 1 和通道 2，将 CCER_CC1E 和 CCER_CC2E 置 1。

配置完成后，在每个 CH1 的上升沿，计数器的值被记录在 CCR1 中，同时计数器被复位并重新开始计数；在每个 CH1 的下降沿，计数器的值被记录在 CCR2 中。将 CCR1 的值乘以 PCLK 的周期，可以算出 PWM 的周期。将 CCR2 的值乘以 PCLK 的周期，可以算出 PWM 高电平持续的时间，从而得到 PWM 的占空比。

9.3.3.9 输出比较模式

在输出比较模式下，当计数值与 CCRx 满足一定关系时，可以在对应 CHx 及 CHxN 上产生特定输出，通常用于控制输出波形，或指示已经过某一时间段。

具体而言，通道将在 CCRx 与计数器之间相匹配时执行下列操作：

1. 将为相应的 CHx 和 CHxN 输出分配一个可编程值，该值由比较模式寄存器 CCMRx_OCxM 和输出极性寄存器 CCER_CCxP/CCxNP 定义。匹配时，输出引脚既可保持其电平（CCMRx_OCxM=0000），也可设置为有效电平 (CCMRx_OCxM=0001)、无效电平 (CCMRx_OCxM=0010) 或进行翻转 (CCMRx_OCxM=0011)。
2. 将中断状态寄存器标志 SR_CCxIF 置 1。

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3. 根据 CCER_CC1IE 生成中断。
4. 根据 DIER_CC1DE 和 CR2_CCDS 生成 DMA 请求。

配置 CCMRx_OCxPE，可将 CCRx 寄存器配置为带或不带影子寄存器。当 CCMRx_OCxPE 为 0 时，软件修改 CCRx 实时生效，可通过在每次中断中修改下一次匹配的 CCRx 来实现自定义波形的输出。

9.3.3.10 基础 PWM 输出

利用输出比较模式，定时器可以产生周期、占空比、相位可控的多路 PWM 输出。PWM 输出的周期由 ARR 决定，占空比由 CCRx 决定。PWM 输出有多种模式，由每个通道的 CCMRx_OCxM 各自独立选择。最基本的单路 PWM 输出只需要占用一个通道，采用基础的 PWM 模式即可实现。复杂的 PWM 信号，或 PWM 组合则需要占用多个通道，并需仔细分配每个通道的 PWM 模式以及 CCRx。

在基础的 PWM 模式下，计数器值 CNT 与 CCRx 进行比较，并根据计数器的当前计数方向产生包含有效电平或无效电平的比较输出信号 OCxREF。有效电平的极性可通过 CCER_CCxP 配置，并根据 CCER_CCxE 和 BDTR_MOE 等寄存器使能 CHx 输出。

如在递增计数模式下，配置 CCMR1_OC1M 和 CCMR1_OC2M 为 0110(0x6)，则 PWM 输出如图9-9。其中计数值 CNT 小于 CCR1/2 时，输出高电平，否则输出低电平。

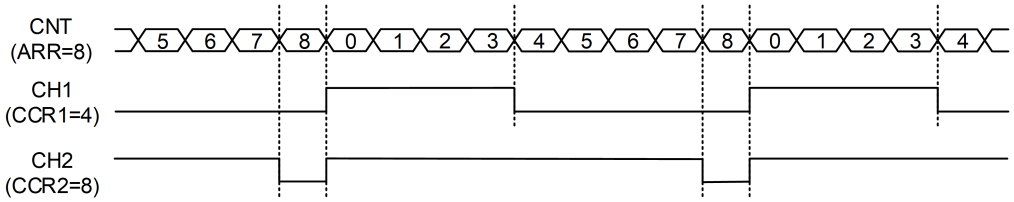


图 9-9: 递增计数模式下的 PWM 输出

如在中心对齐计数模式下，配置 CCMR1_OC1M 和 CCMR1_OC2M 为 0110(0x6)，则 PWM 输出如图9-10。其中递增阶段计数值 CNT 小于 CCR1/2 时，输出高电平，否则输出低电平；递减阶段计数值 CNT 大于 CCR1/2 时，输出低电平，否则输出高电平。

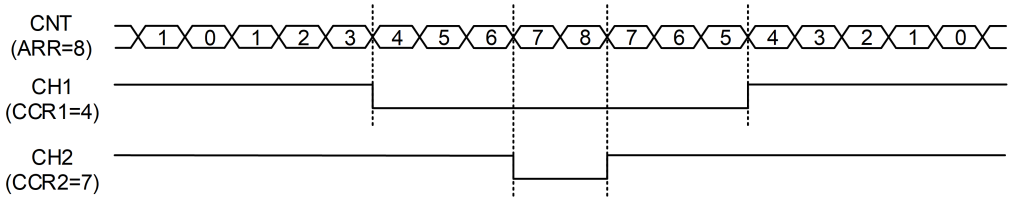


图 9-10: 中心对齐计数模式下的 PWM 输出

9.3.3.11 不对称 PWM 输出

在不对称 PWM 模式下，生成的两个 PWM 信号之间存在可编程相移。该模式仅限于计数器处于中心对齐模式时。生成的两个 PWM 信号频率相同，由 ARR 的值确定，而占空比和相移则各由一对 CCRx 寄存器确定。每一路输出 PWM 占用两个 CCRx 寄存器，分别控制递增计数和递减计数期间的行为，这样 PWM 的上升沿和下降沿时间点可以分别配置。CCR1 和 CCR2 共同控制 CH1/2 的输出，CCR3 和 CCR4 共同控制 CH3/4 的输出。

CH1/2 以及 CH3/4 可以独立选择不同的不对称 PWM 模式，配置 CCMRx_OCxM 为 1110(0xe) 或 1111(0xf)。

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如配置 CCMR1_OC1M 和 CCMR2_OC3M 为 1110(0xe)，则 PWM 输出如图9-11。其中递增阶段 (0->ARR-1) 计数值 CNT 小于 CCR1/3 时，输出高电平，否则输出低电平；递减阶段 (ARR->1) 计数值 CNT 大于 CCR2/4 时，输出低电平，否则输出高电平。

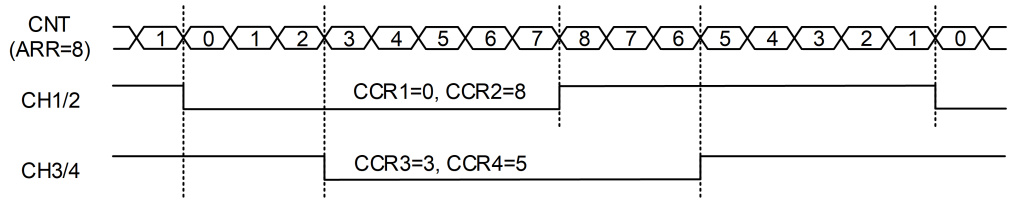


图 9-11: 不对称 PWM 输出

9.3.3.12 组合 PWM 输出

在组合 PWM 模式下，生成的两个 PWM 信号之间存在可编程延时和相移。计数器处于递增、递减或中心对齐模式均可，生成的两个 PWM 信号频率相同，由 ARR 的值确定，而占空比和相移则各由一对 CCRx 寄存器确定。每一路输出 PWM 占用两个 CCRx 寄存器，是由两路基础 PWM 输出波形的逻辑与运算或者逻辑或运算组合而成。CCR1 和 CCR2 共同控制 CH1/2 的输出，CCR3 和 CCR4 共同控制 CH3/4 的输出。

CH1/2 以及 CH3/4 可以独立选择不同的组合 PWM 模式，配置 CCMRx_OCxM 为 1100(0xc) 或 1101(0xd)。当 CH1 或 CH3 配置为组合 PWM 模式 1100(0xc) 时，CH2 或 CH4 必须配置为 0111(0x7) 或 1101(0xd) 或 1111(0xf)。当 CH1 或 CH3 配置为组合 PWM 模式 1101(0xd) 时，CH2 或 CH4 必须配置为 0110(0x6) 或 1100(0xc) 或 1110(0xe)。

如配置 CCMR1_OC1M 为 1101(0xd)，CCMR1_OC2M 为 0110(0x6)，CCMR2_OC3M 为 1100(0xc)，CCMR2_OC4M 为 0111(0x7)，则 PWM 输出如图9-12。其中计数值 CNT 小于 CCR1/4 时，OC1REF/OC4REF 为低电平，否则为高电平；计数值 CNT 小于 CCR2/3 时，OC2REF/OC3REF 为高电平，否则为低电平。CH1 输出是 OC1REF 和 OC2REF 的逻辑与运算。CH3 输出是 OC3REF 和 OC4REF 的逻辑或运算。

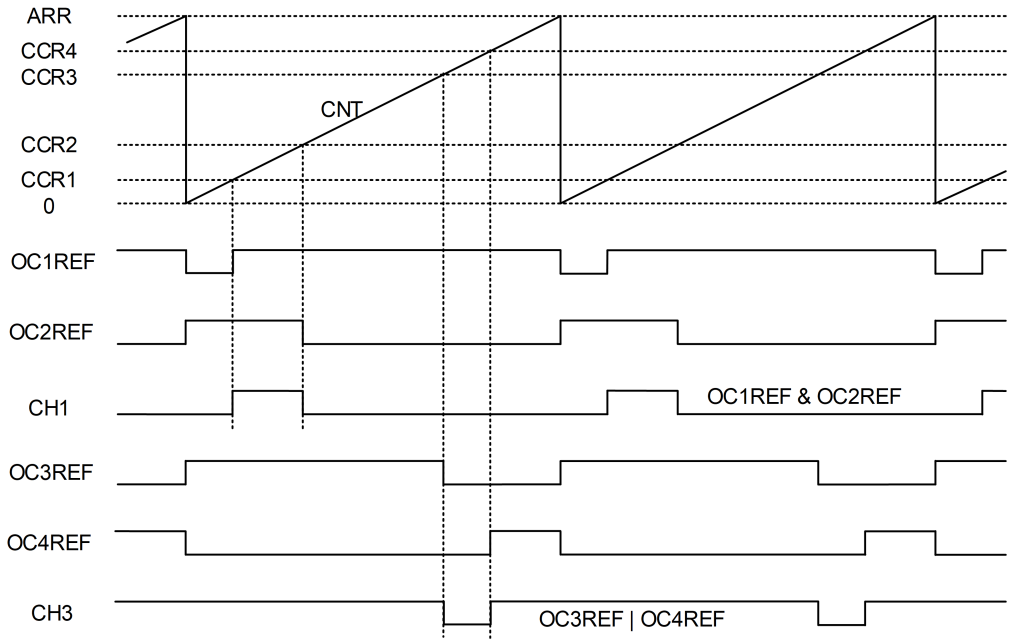


图 9-12: 组合 PWM 输出

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9.3.3.13 单脉冲模式

将 CR1_OPM 写 1 可以使能单脉冲模式。该模式下计数器启动以后一旦发生更新事件，就会自动停止计数。该模式可以用于单次计数，或在一个激励信号的触发下启动，并在一段可编程的延时后产生一个脉宽可编程的脉冲。

例如，希望实现这样的功能，在 CH2 输入引脚检测到上升沿时，经过一定时间延迟，在 CH1 上产生单个一定宽度的正脉冲。配置方法如下：

1. CCMR1_CC2S=01，以将 TI2FP2 映射到通道 2。
2. CCER_CCxP 和 CCER_CCxNP 写 0，TI2FP2 反应 CH2 上升沿的变化。
3. SMCR_TS=110(0x6)，将 TI2FP2 配置为从模式控制器的触发 TRGI。
4. SMCR_SMS=110(0x6)，将从模式控制器配置为触发模式，触发后开启计数。
5. 根据需要的时间延迟与脉冲宽度配置 ARR 与 CCR1，定义时间延迟与脉冲宽度。
6. CCMR1_OC1M=0111(0x7)，配置为正脉冲 PWM。
7. CR1_OPM=1，一次触发只产生一个脉冲。
8. EGR_UG=1，手动刷新 ARR 与 CCR1 寄存器。

从模式为触发模式时不需要手动使能 CR1_CEN，一旦检测到触发信号生效，计数器就会自动使能。

9.3.3.14 编码器接口模式

编码器接口模式下，通道 1 和通道 2 可以用于连接外部正交编码器，将外部编码器的信号转化为定时器的计数值变化，从而获知外部编码器的工作状态。

如果计数器仅在 CH1 边沿处计数，SMCR_SMS 配置为 0001；如果计数器仅在 CH2 边沿处计数，SMCR_SMS 配置为 0010(0x2)；如果计数器在 CH1 和 CH2 边沿处均计数，SMCR_SMS 配置为 0011(0x3)。CCER_CC1P/CC2P 用于选择 CH1 和 CH2 极性。如果需要，还可对输入滤波器进行编程。两个输入的信号转换序列会产生计数脉冲和方向信号，根据该信号转换序列，计数器相应递增或递减计数，同时硬件对 CR1_DIR 进行相应修改。

编码器接口模式下，计数器的计数事件是正交编码器接口的解码输出。计数器仅在 0 到 ARR 之间进行连续计数（根据计数的具体方向，从 0 递增计数到 ARR，或从 ARR 递减计数到 0）。因此，在启动前必须先配置 ARR。同样，捕获、比较、重复计数器和触发输出功能继续正常工作。在此模式下，计数器会根据正交编码器的速度和方向自动进行修改，因此，其内容始终表示编码器的位置。计数方向对应于所连传感器的旋转方向。下表汇总了可能的组合（假设 CH1 和 CH2 不同时切换）。

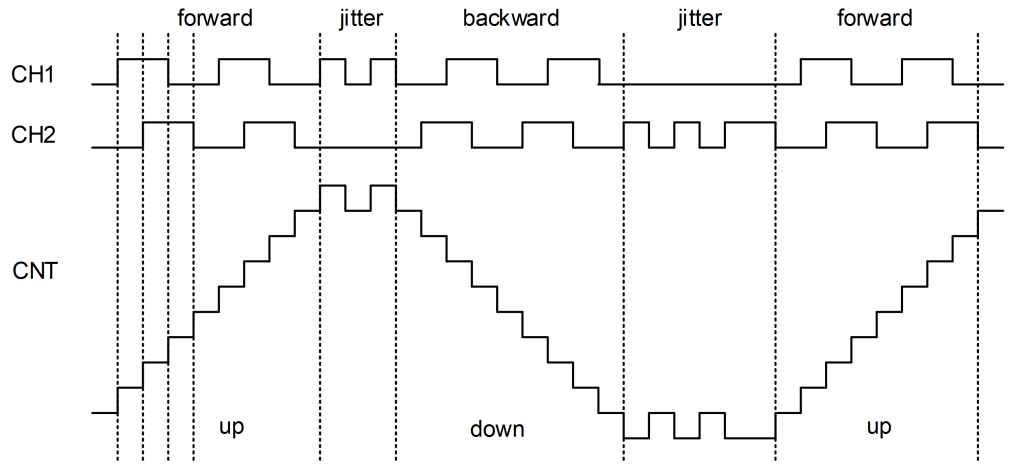
SMCR_SMS	条件	CH1 上升沿	CH1 下降沿	CH2 上升沿	CH2 下降沿
0001 或 0011	CH2=0	递增	递减	/	/
	CH2=1	递减	递增	/	/
0010 或 0011	CH1=0	/	/	递减	递增
	CH1=1	/	/	递增	递减

下图示意了计数器如何根据正交编码器的信号变化进行计数的，配置如下：

CCMR1_CC1S=01（CH1 映射到通道 1 上），CCMR2_CC2S=01（CH2 映射到通道 2 上），

CCER_CC1P/CC1NP/CC2P/CC2NP=0，SMCR_SMS=0011(0x3)，CR1_CEN=1。

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9.3.3.15 定时器同步

多个定时器可通过主从模式连接在一起，实现定时器同步，以完成多级分频、同时启动、门控计数等功能。

将主模式定时器的 TRGO 设置为更新事件 (CR2_MMS=010)，连接至另一个设置为外部时钟从模式 (SMCR_SMS = 0111) 的定时器，可以实现定时器级联计数。此时主模式定时器相当于从模式定时器的预分频，计数总位宽等于两个定时器各自的位宽相加。

将主模式定时器的 TRGO 设置为计数使能 (CR2_MMS=001)，并设置从模式为触发从模式 (SMCR_SMS=0110)，同时连接至另一个设置为触发从模式 (SMCR_SMS=0110) 的定时器，可以实现多个定时器同步触发启动，从而对齐多个定时器的开启时机。该场景下主模式定时器还需将 SMCR_MSM 设为 1。

将主模式定时器的 TRGO 设置为比较输出 (CR2_MMS=100)，连接至另一个设置为门控从模式 (SMCR_SMS=0101) 的定时器，可以实现门控 PWM 输出。主模式定时器可以对从模式定时器输出的 PWM 载波进行调制输出。

9.3.3.16 通知机制

GPTIM 能够产生中断、DMA 请求、PTC 触发等多种通知机制。能够触发通知的事件主要包括更新事件、触发事件、比较器匹配、输入捕获等。DIER 寄存器可以控制各种事件是否产生中断和 DMA 请求。各事件状态可在 SR 寄存器中查询。

9.3.4 GPTIM 寄存器

表 9-3: GPTIM 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**CR1**	TIM control register 1
[31:12]			RSVD	
[11]	rw	1'h0	UIFREMAP	UIF status bit remapping 0: No remapping. UIF status bit is not copied to CNT register bit 31 1: Remapping enabled. UIF status bit is copied to CNT register bit 31
[10:8]			RSVD	
[7]	rw	1'h0	ARPE	Auto-reload preload enable 0: ARR register is not buffered 1: ARR register is buffered

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表 9-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[6:5]	rw	2'h0	CMS	Center-aligned mode selection 00: Edge-aligned mode. The counter counts up or down depending on the direction bit (DIR). 01: Center-aligned mode 1. The counter counts up and down alternatively. Output compare interrupt flags of channels configured in output (CCxS=00 in CCMRx register) are set only when the counter is counting down. 10: Center-aligned mode 2. The counter counts up and down alternatively. Output compare interrupt flags of channels configured in output (CCxS=00 in CCMRx register) are set only when the counter is counting up. 11: Center-aligned mode 3. The counter counts up and down alternatively. Output compare interrupt flags of channels configured in output (CCxS=00 in CCMRx register) are set both when the counter is counting up or down.
[4]	rw	1'h0	DIR	Direction 0: Counter used as upcounter 1: Counter used as downcounter
[3]	rw	1'h0	OPM	One-pulse mode 0: Counter is not stopped at update event 1: Counter stops counting at the next update event (clearing the bit CEN)
[2]	rw	1'h0	URS	Update request source This bit is set and cleared by software to select the UEV event sources. 0: Any of the following events generate an update interrupt or DMA request if enabled. These events can be: Counter overflow/underflow Setting the UG bit Update generation through the slave mode controller 1: Only counter overflow/underflow generates an update interrupt or DMA request if enabled.
[1]	rw	1'h0	UDIS	Update disable This bit is set and cleared by software to enable/disable UEV event generation. 0: UEV enabled. The Update (UEV) event is generated by one of the following events: Counter overflow/underflow Setting the UG bit Update generation through the slave mode controller Buffered registers are then loaded with their preload values. 1: UEV disabled. The Update event is not generated, shadow registers keep their value (ARR, PSC, CCRx). However the counter and the prescaler are reinitialized if the UG bit is set or if a hardware reset is received from the slave mode controller.
[0]	rw	1'h0	CEN	Counter enable 0: Counter disabled 1: Counter enabled Note: External clock, gated mode and encoder mode can work only if the CEN bit has been previously set by software. However trigger mode can set the CEN bit automatically by hardware. CEN is cleared automatically in one-pulse mode, when an update event occurs.
0x04			**CR2**	TIM control register 2
[31:8]			RSVD	

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表 9-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7]	rw	1'h0	TI1S	TI1 selection 0: The CH1 pin is connected to TI1 input 1: The CH1, CH2 and CH3 pins are connected to the TI1 input (XOR combination)
[6:4]	rw	3'h0	MMS	Master mode selection These bits allow to select the information to be sent in master mode to slave timers for synchronization (TRGO). The combination is as follows: 000: Reset - the UG bit from the EGR register is used as trigger output (TRGO). If the reset is generated by the trigger input (slave mode controller configured in reset mode) then the signal on TRGO is delayed compared to the actual reset. 001: Enable - the Counter enable signal is used as trigger output (TRGO). It is useful to start several timers at the same time or to control a window in which a slave timer is enabled. The Counter Enable signal is generated by a logic OR between CEN control bit and the trigger input when configured in gated mode. When the Counter Enable signal is controlled by the trigger input, there is a delay on TRGO, except if the master/slave mode is selected. 010: Update - The update event is selected as trigger output (TRGO). For instance a master timer can then be used as a prescaler for a slave timer. 011: Compare Pulse - The trigger output send a positive pulse when the CC1IF flag is to be set (even if it was already high), as soon as a capture or a compare match occurred. (TRGO) 100: Compare - OC1REF signal is used as trigger output (TRGO) 101: Compare - OC2REF signal is used as trigger output (TRGO) 110: Compare - OC3REF signal is used as trigger output (TRGO) 111: Compare - OC4REF signal is used as trigger output (TRGO)
[3]	rw	1'h0	CCDS	Capture/compare DMA selection 0: CCx DMA request sent when CCx event occurs 1: CCx DMA requests sent when update event occurs
[2:0]			RSVD	
0x08			**SMCR**	TIM slave mode control register
[31:20]			RSVD	

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表 9-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[19:16]	rw	4'h0	SMS	Slave mode selection When external signals are selected the active edge of the trigger signal (TRGI) is linked to the polarity selected on the external input. 0000: Slave mode disabled. 0001: Encoder mode 1 - Counter counts up/down on TI1FP1 edge depending on TI2FP2 level. 0010: Encoder mode 2 - Counter counts up/down on TI2FP2 edge depending on TI1FP1 level. 0011: Encoder mode 3 - Counter counts up/down on both TI1FP1 and TI2FP2 edges depending on the level of the other input. 0100: Reset Mode - Rising edge of the selected trigger input (TRGI) reinitializes the counter and generates an update of the registers. 0101: Gated Mode - The counter clock is enabled when the trigger input (TRGI) is high. The counter stops (but is not reset) as soon as the trigger becomes low. Both start and stop of the counter are controlled. 0110: Trigger Mode - The counter starts at a rising edge of the trigger TRGI (but it is not reset). Only the start of the counter is controlled. 0111: External Clock Mode 1 - Rising edges of the selected trigger (TRGI) clock the counter. 1000: Combined reset + trigger mode - Rising edge of the selected trigger input (TRGI) reinitializes the counter, generates an update of the registers and starts the counter.
[15]	rw	1'h0	ETP	External trigger polarity 0: ETR is non-inverted, active at high level or rising edge 1: ETR is inverted, active at low level or falling edge
[14]	rw	1'h0	ECE	External clock enable This bit enables External clock mode 2. 0: External clock mode 2 disabled 1: External clock mode 2 enabled. The counter is clocked by any active edge on the ETRF signal.
[13:12]	rw	2'h0	ETPS	External trigger prescaler External trigger signal ETRP frequency must be at most 1/4 of CK_INT frequency. A prescaler can be enabled to reduce ETRP frequency. It is useful when inputting fast external clocks. 00: Prescaler OFF 01: ETRP frequency divided by 2 10: ETRP frequency divided by 4 11: ETRP frequency divided by 8

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表 9-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11:8]	rw	4'h0	ETF	External trigger filter This bit-field then defines the frequency used to sample ETRP signal and the length of the digital filter applied to ETRP. The digital filter is made of an event counter in which N consecutive events are needed to validate a transition on the output: 0000: No filter 0001: fSAMPLING=fCLK, N=2 0010: fSAMPLING=fCLK, N=4 0011: fSAMPLING=fCLK, N=8 0100: fSAMPLING=fCLK/2, N=6 0101: fSAMPLING=fCLK/2, N=8 0110: fSAMPLING=fCLK/4, N=6 0111: fSAMPLING=fCLK/4, N=8 1000: fSAMPLING=fCLK/8, N=6 1001: fSAMPLING=fCLK/8, N=8 1010: fSAMPLING=fCLK/16, N=5 1011: fSAMPLING=fCLK/16, N=6 1100: fSAMPLING=fCLK/16, N=8 1101: fSAMPLING=fCLK/32, N=5 1110: fSAMPLING=fCLK/32, N=6 1111: fSAMPLING=fCLK/32, N=8
[7]	rw	1'h0	MSM	Master/Slave mode 0: No action 1: The effect of an event on the trigger input (TRGI) is delayed to allow a perfect synchronization between the current timer and its slaves (through TRGO). It is useful if we want to synchronize several timers on a single external event.
[6:4]	rw	3'h0	TS	Trigger selection This bit-field selects the trigger input to be used to synchronize the counter. 000: Internal Trigger 0 (ITR0) 001: Internal Trigger 1 (ITR1) 010: Internal Trigger 2 (ITR2) 011: Internal Trigger 3 (ITR3) 100: TI1 Edge Detector (TI1F_ED) 101: Filtered Timer Input 1 (TI1FP1) 110: Filtered Timer Input 2 (TI2FP2) 111: External Trigger input (ETRF)
[3:0]			RSVD	
0x0C			**DIER**	TIM DMA/Interrupt enable register
[31:15]			RSVD	
[14]	rw	1'h0	TDE	Trigger DMA request enable 0: Trigger DMA request disabled. 1: Trigger DMA request enabled.
[13]			RSVD	
[12]	rw	1'h0	CC4DE	Capture/Compare 4 DMA request enable 0: CC4 DMA request disabled. 1: CC4 DMA request enabled
[11]	rw	1'h0	CC3DE	Capture/Compare 3 DMA request enable 0: CC3 DMA request disabled. 1: CC3 DMA request enabled.

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表 9-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[10]	rw	1'h0	CC2DE	Capture/Compare 2 DMA request enable 0: CC2 DMA request disabled. 1: CC2 DMA request enabled.
[9]	rw	1'h0	CC1DE	Capture/Compare 1 DMA request enable 0: CC1 DMA request disabled. 1: CC1 DMA request enabled.
[8]	rw	1'h0	UDE	Update DMA request enable 0: Update DMA request disabled. 1: Update DMA request enabled
[7]			RSVD	
[6]	rw	1'h0	TIE	Trigger interrupt enable 0: Trigger interrupt disabled. 1: Trigger interrupt enabled
[5]			RSVD	
[4]	rw	1'h0	CC4IE	Capture/Compare 4 interrupt enable 0: CC4 interrupt disabled. 1: CC4 interrupt enabled
[3]	rw	1'h0	CC3IE	Capture/Compare 3 interrupt enable 0: CC3 interrupt disabled. 1: CC3 interrupt enabled
[2]	rw	1'h0	CC2IE	Capture/Compare 2 interrupt enable 0: CC2 interrupt disabled. 1: CC2 interrupt enabled.
[1]	rw	1'h0	CC1IE	Capture/Compare 1 interrupt enable 0: CC1 interrupt disabled. 1: CC1 interrupt enabled
[0]	rw	1'h0	UIE	Update interrupt enable 0: Update interrupt disabled. 1: Update interrupt enabled
0x10			**SR**	TIM status register
[31:13]			RSVD	
[12]	rw0c	1'h0	CC4OF	Capture/Compare 4 overcapture flag
[11]	rw0c	1'h0	CC3OF	Capture/Compare 3 overcapture flag
[10]	rw0c	1'h0	CC2OF	Capture/Compare 2 overcapture flag
[9]	rw0c	1'h0	CC1OF	Capture/Compare 1 overcapture flag This flag is set by hardware only when the corresponding channel is configured in input capture mode. It is cleared by software by writing it to '0'. 0: No overcapture has been detected. 1: The counter value has been captured in CCR1 register while CC1IF flag was already set
[8:7]			RSVD	
[6]	rw0c	1'h0	TIF	Trigger interrupt flag This flag is set by hardware on trigger event (active edge detected on TRGI input when the slave mode controller is enabled in all modes but gated mode). It is set when the counter starts or stops when gated mode is selected. It is cleared by software. 0: No trigger event occurred. 1: Trigger interrupt pending.
[5]			RSVD	

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表 9-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw0c	1'h0	CC4IF	Capture/Compare 4 interrupt flag
[3]	rw0c	1'h0	CC3IF	Capture/Compare 3 interrupt flag
[2]	rw0c	1'h0	CC2IF	Capture/Compare 2 interrupt flag
[1]	rw0c	1'h0	CC1IF	Capture/Compare 1 interrupt flag If channel CC1 is configured as output: This flag is set by hardware when the counter matches the compare value. It is cleared by software. 0: No match. 1: The content of the counter CNT has matched the content of the CCR1 register. If channel CC1 is configured as input: This bit is set by hardware on a capture. It is cleared by software or by reading the CCR1 register. 0: No input capture occurred. 1: The counter value has been captured in CCR1 register (An edge has been detected on IC1 which matches the selected polarity).
[0]	rw0c	1'h0	UIF	Update interrupt flag This bit is set by hardware on an update event. It is cleared by software. 0: No update occurred 1: Update interrupt pending. This bit is set by hardware when the registers are updated: At overflow or underflow and if UDIS=0 in the CR1 register. When CNT is reinitialized by software using the UG bit in EGR register, if URS=0 and UDIS=0 in the CR1 register. When CNT is reinitialized by a trigger event, if URS=0 and UDIS=0 in the CR1 register.
0x14			**EGR**	Event generation register
[31:7]			RSVD	
[6]	w	1'h0	TG	Trigger generation This bit is set by software in order to generate an event, it is automatically cleared by hardware. 0: No action 1: The TIF flag is set in SR register. Related interrupt or DMA transfer can occur if enabled.
[5]			RSVD	
[4]	w	1'h0	CC4G	Capture/compare 4 generation
[3]	w	1'h0	CC3G	Capture/compare 3 generation
[2]	w	1'h0	CC2G	Capture/compare 2 generation
[1]	w	1'h0	CC1G	Capture/compare 1 generation This bit is set by software in order to generate an event, it is automatically cleared by hardware. 0: No action 1: A capture/compare event is generated on channel 1: If channel CC1 is configured as output: CC1IF flag is set, Corresponding interrupt or DMA request is sent if enabled. If channel CC1 is configured as input: The current value of the counter is captured in CCR1 register. The CC1IF flag is set, the corresponding interrupt or DMA request is sent if enabled. The CC1OF flag is set if the CC1IF flag was already high.

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表 9-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[0]	w	1'h0	UG	Update generation This bit can be set by software, it is automatically cleared by hardware. 0: No action 1: Re-initialize the counter and generates an update of the registers. Note that the prescaler counter is cleared too (anyway the prescaler ratio is not affected). The counter is cleared if the center-aligned mode is selected or if DIR=0 (upcounting), else it takes the auto-reload value (ARR) if DIR=1 (downcounting).
0x18			**CCMR1**	TIM capture/compare mode register 1
[31:28]	rw	4'h0	OC2M	Output compare 2 mode
[27]	rw	1'h0	OC2PE	Output compare 2 preload enable
[26:25]			RSVD	
[24]	rw	1'h0	OC2CE	Output compare 2 clear enable

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表 9-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[23:20]	rw	4'h0	OC1M	Output compare 1 mode These bits define the behavior of the output reference signal OC1REF from which OC1 and OC1N are derived. OC1REF is active high whereas OC1 and OC1N active level depends on CC1P and CC1NP bits. 0000: Frozen - The comparison between the output compare register CCR1 and the counter CNT has no effect on the outputs.(this mode is used to generate a timing base). 0001: Set channel 1 to active level on match. OC1REF signal is forced high when the counter CNT matches the capture/compare register 1 (CCR1). 0010: Set channel 1 to inactive level on match. OC1REF signal is forced low when the counter CNT matches the capture/compare register 1 (CCR1). 0011: Toggle - OC1REF toggles when CNT=CCR1. 0100: Force inactive level - OC1REF is forced low. 0101: Force active level - OC1REF is forced high. 0110: PWM mode 1 - In upcounting, channel 1 is active as long as CNT<CCR1 else inactive. In downcounting, channel 1 is inactive (OC1REF='0) as long as CNT>CCR1 else active (OC1REF=1). 0111: PWM mode 2 - In upcounting, channel 1 is inactive as long as CNT<CCR1 else active. In downcounting, channel 1 is active as long as CNT>CCR1 else inactive. 1000: Retriggerable OPM mode 1 - In up-counting mode, the channel is active until a trigger event is detected (on TRGI signal). Then, a comparison is performed as in PWM mode 1 and the channels becomes inactive again at the next update. In down-counting mode, the channel is inactive until a trigger event is detected (on TRGI signal). Then, a comparison is performed as in PWM mode 1 and the channels becomes inactive again at the next update. 1001: Retriggerable OPM mode 2 - In up-counting mode, the channel is inactive until a trigger event is detected (on TRGI signal). Then, a comparison is performed as in PWM mode 2 and the channels becomes inactive again at the next update. In down-counting mode, the channel is active until a trigger event is detected (on TRGI signal). Then, a comparison is performed as in PWM mode 1 and the channels becomes active again at the next update. 1010: Reserved, 1011: Reserved, 1100: Combined PWM mode 1 - OC1REF has the same behavior as in PWM mode 1. OC1REFC is the logical OR between OC1REF and OC2REF. 1101: Combined PWM mode 2 - OC1REF has the same behavior as in PWM mode 2. OC1REFC is the logical AND between OC1REF and OC2REF. 1110: Asymmetric PWM mode 1 - OC1REF has the same behavior as in PWM mode 1. OC1REFC outputs OC1REF when the counter is counting up, OC2REF when it is counting down. 1111: Asymmetric PWM mode 2 - OC1REF has the same behavior as in PWM mode 2. OC1REFC outputs OC1REF when the counter is counting up, OC2REF when it is counting down.
[19]	rw	1'h0	OC1PE	Output compare 1 preload enable 0: Preload register on CCR1 disabled. CCR1 can be written at anytime, the new value is taken in account immediately. 1: Preload register on CCR1 enabled. Read/Write operations access the preload register. CCR1 preload value is loaded in the active register at each update event.

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表 9-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[18:17]			RSVD	
[16]	rw	1'h0	OC1CE	Output compare 1 clear enable 0: OC1Ref is not affected by the ETRF input 1: OC1Ref is cleared as soon as a High level is detected on ETRF input
[15:12]	rw	4'h0	IC2F	Input capture 2 filter
[11:10]	rw	2'h0	IC2PSC	Input capture 2 prescaler
[9:8]	rw	2'h0	CC2S	Capture/Compare 2 selection This bit-field defines the direction of the channel (input/output) as well as the used input. 00: CC2 channel is configured as output 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is working only if an internal trigger input is selected through the TS bit (SMCR register)
[7:4]	rw	4'h0	IC1F	Input capture 1 filter This bit-field defines the frequency used to sample TI1 input and the length of the digital filter applied to TI1. The digital filter is made of an event counter in which N consecutive events are needed to validate a transition on the output: 0000: No filter, sampling is done at fCLK 0001: fSAMPLING=fCLK, N=2 0010: fSAMPLING=fCLK, N=4 0011: fSAMPLING=fCLK, N=8 0100: fSAMPLING=fCLK/2, N=6 0101: fSAMPLING=fCLK/2, N=8 0110: fSAMPLING=fCLK/4, N=6 0111: fSAMPLING=fCLK/4, N=8 1000: fSAMPLING=fCLK/8, N=6 1001: fSAMPLING=fCLK/8, N=8 1010: fSAMPLING=fCLK/16, N=5 1011: fSAMPLING=fCLK/16, N=6 1100: fSAMPLING=fCLK/16, N=8 1101: fSAMPLING=fCLK/32, N=5 1110: fSAMPLING=fCLK/32, N=6 1111: fSAMPLING=fCLK/32, N=8
[3:2]	rw	2'h0	IC1PSC	Input capture 1 prescaler This bit-field defines the ratio of the prescaler acting on CC1 input (IC1). The prescaler is reset as soon as CC1E=0. 00: no prescaler, capture is done each time an edge is detected on the capture input 01: capture is done once every 2 events 10: capture is done once every 4 events 11: capture is done once every 8 events

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表 9-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1:0]	rw	2'h0	CC1S	Capture/Compare 1 selection This bit-field defines the direction of the channel (input/output) as well as the used input. 00: CC1 channel is configured as output 01: CC1 channel is configured as input, IC1 is mapped on TI1 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channel is configured as input, IC1 is mapped on TRC. This mode is working only if an internal trigger input is selected through TS bit (SMCR register)
0x1C			**CCMR2**	TIM capture/compare mode register 2
[31:28]	rw	4'h0	OC4M	Output compare 4 mode
[27]	rw	1'h0	OC4PE	Output compare 4 preload enable
[26:25]			RSVD	
[24]	rw	1'h0	OC4CE	Output compare 4 clear enable
[23:20]	rw	4'h0	OC3M	Output compare 3 mode
[19]	rw	1'h0	OC3PE	Output compare 3 preload enable
[18:17]			RSVD	
[16]	rw	1'h0	OC3CE	Output compare 3 clear enable
[15:12]	rw	4'h0	IC4F	Input capture 4 filter
[11:10]	rw	2'h0	IC4PSC	Input capture 4 prescaler
[9:8]	rw	2'h0	CC4S	Capture/Compare 4 selection This bit-field defines the direction of the channel (input/output) as well as the used input. 00: CC4 channel is configured as output 01: CC4 channel is configured as input, IC4 is mapped on TI4 10: CC4 channel is configured as input, IC4 is mapped on TI3 11: CC4 channel is configured as input, IC4 is mapped on TRC. This mode is working only if an internal trigger input is selected through TS bit (SMCR register)
[7:4]	rw	4'h0	IC3F	Input capture 3 filter
[3:2]	rw	2'h0	IC3PSC	Input capture 3 prescaler
[1:0]	rw	2'h0	CC3S	Capture/Compare 3 selection This bit-field defines the direction of the channel (input/output) as well as the used input. 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped on TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped on TRC. This mode is working only if an internal trigger input is selected through TS bit (SMCR register)
0x20			**CCER**	Capture/Compare enable register
[31:16]			RSVD	
[15]	rw	1'h0	CC4NP	Capture/Compare 4 output Polarity.
[14]			RSVD	
[13]	rw	1'h0	CC4P	Capture/Compare 4 output Polarity.
[12]	rw	1'h0	CC4E	Capture/Compare 4 output enable.
[11]	rw	1'h0	CC3NP	Capture/Compare 3 output Polarity.
[10]			RSVD	
[9]	rw	1'h0	CC3P	Capture/Compare 3 output Polarity.

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表 9-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[8]	rw	1'h0	CC3E	Capture/Compare 3 output enable.
[7]	rw	1'h0	CC2NP	Capture/Compare 2 output Polarity.
[6]			RSVD	
[5]	rw	1'h0	CC2P	Capture/Compare 2 output Polarity.
[4]	rw	1'h0	CC2E	Capture/Compare 2 output enable.
[3]	rw	1'h0	CC1NP	Capture/Compare 1 output Polarity. CC1 channel configured as output: CC1NP must be kept cleared in this case. CC1 channel configured as input: This bit is used in conjunction with CC1P to define TI1FP1/TI2FP1 polarity. refer to CC1P description.
[2]			RSVD	
[1]	rw	1'h0	CC1P	Capture/Compare 1 output Polarity. CC1 channel configured as output: 0: OC1 active high 1: OC1 active low CC1 channel configured as input: CC1NP/CC1P bits select TI1FP1 and TI2FP1 polarity for trigger or capture operations. 00: noninverted/rising edge Circuit is sensitive to TIxFP1 rising edge (capture, trigger in reset, external clock or trigger mode), TIxFP1 is not inverted (trigger in gated mode, encoder mode). 01: inverted/falling edge Circuit is sensitive to TIxFP1 falling edge (capture, trigger in reset, external clock or trigger mode), TIxFP1 is inverted (trigger in gated mode, encoder mode). 10: reserved, do not use this configuration. 11: noninverted/both edges Circuit is sensitive to both TIxFP1 rising and falling edges (capture, trigger in reset, external clock or trigger mode), TIxFP1 is not inverted (trigger in gated mode). This configuration must not be used for encoder mode.
[0]	rw	1'h0	CC1E	Capture/Compare 1 output enable. CC1 channel configured as output: 0: Off - OC1 is not active 1: On - OC1 signal is output on the corresponding output pin CC1 channel configured as input: This bit determines if a capture of the counter value can actually be done into the input capture/compare register 1 (CCR1) or not. 0: Capture disabled 1: Capture enabled
0x24			**CNT**	Counter
[31]	r	1'h0	UIFCPY	Value depends on IUFREMAP in CR1. If UIFREMAP = 1 UIFCPY: UIF Copy This bit is a read-only copy of the UIF bit of the ISR register
[30:16]			RSVD	
[15:0]	rw	16'h0	CNT	counter value
0x28			**PSC**	Prescaler
[31:16]			RSVD	

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表 9-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[15:0]	rw	16'h0	PSC	Prescaler value The counter clock frequency is equal to fCLK / (PSC[15:0] + 1). PSC contains the value to be loaded in the active prescaler register at each update event (including when the counter is cleared through UG bit of EGR register or through trigger controller when configured in 'reset mode').
0x2C			**ARR**	Auto-reload register
[31:16]			RSVD	
[15:0]	rw	16'h0	ARR	Auto-reload value ARR is the value to be loaded in the actual auto-reload register.
0x30			**RCR**	Repetition counter register
[31:8]			RSVD	
[7:0]	rw	8'h0	REP	Repetition counter value These bits allow the user to set-up the update rate of the compare registers (i.e. periodic transfers from preload to active registers) when preload registers are enable, as well as the update interrupt generation rate, if this interrupt is enable. Each time the REP_CNT related downcounter reaches zero, an update event is generated and it restarts counting from REP value. As REP_CNT is reloaded with REP value only at the repetition update event, any write to the RCR register is not taken in account until the next repetition update event. It means in PWM mode (REP+1) corresponds to the number of PWM periods in edge-aligned mode.
0x34			**CCR1**	Capture/Compare register 1
[31:16]			RSVD	
[15:0]	rw	16'h0	CCR1	Capture/Compare 1 value If channel CC1 is configured as output: CCR1 is the value to be loaded in the actual capture/compare 1 register (preload value).It is loaded permanently if the preload feature is not selected in the CCMR1 register (bit OC1PE). Else the preload value is copied in the active capture/compare 1 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signaled on OC1 output. If channel CC1is configured as input: CCR1 is the counter value transferred by the last input capture 1 event (IC1). The CCR1 register is read-only and cannot be programmed.
0x38			**CCR2**	Capture/Compare register 2
[31:16]			RSVD	
[15:0]	rw	16'h0	CCR2	Capture/Compare 2 value If channel CC2 is configured as output: CCR2 is the value to be loaded in the actual capture/compare 2 register (preload value).It is loaded permanently if the preload feature is not selected in the CCMR1 register (bit OC2PE). Else the preload value is copied in the active capture/compare 2 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signalled on OC2 output. If channel CC2 is configured as input: CCR2 is the counter value transferred by the last input capture 2 event (IC2). The CCR2 register is read-only and cannot be programmed.
0x3C			**CCR3**	Capture/Compare register 3
[31:16]			RSVD	

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表 9-3: GPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[15:0]	rw	16'h0	CCR3	Capture/Compare value If channel CC3 is configured as output: CCR3 is the value to be loaded in the actual capture/compare 3 register (preload value).It is loaded permanently if the preload feature is not selected in the CCMR2 register (bit OC3PE). Else the preload value is copied in the active capture/compare 3 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signalled on OC3 output. If channel CC3is configured as input: CCR3 is the counter value transferred by the last input capture 3 event (IC3). The CCR3 register is read-only and cannot be programmed.
0x40			**CCR4**	Capture/Compare register 4
[31:16]			RSVD	
[15:0]	rw	16'h0	CCR4	Capture/Compare value 1. if CC4 channel is configured as output: CCR4 is the value to be loaded in the actual capture/compare 4 register (preload value).It is loaded permanently if the preload feature is not selected in the CCMR2 register (bit OC4PE). Else the preload value is copied in the active capture/compare 4 register when an update event occurs. The active capture/compare register contains the value to be compared to the counter CNT and signalled on OC4 output. 2. if CC4 channel is configured as input: CCR4 is the counter value transferred by the last input capture 4 event (IC4). The CCR4 register is read-only and cannot be programmed.

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9.3.5 定时器级联

表 9-4: 定时器级联

下级定时器	级联端口	上级定时器
ATIM1	ITR0	BTIM2
	ITR1	GPTIM2
	ITR2	GPTIM1
	ITR3	BTIM1
GPTIM1	ITR0	GPTIM2
	ITR1	BTIM2
	ITR2	ATIM1
	ITR3	BTIM1
GPTIM2	ITR0	GPTIM1
	ITR1	ATIM1
	ITR2	BTIM1
	ITR3	BTIM2
BTIM1	ITR0	BTIM2
	ITR1	GPTIM1
	ITR2	ATIM1
	ITR3	GPTIM2
BTIM2	ITR0	GPTIM1
	ITR1	BTIM1
	ITR2	GPTIM2
	ITR3	ATIM1

9.4 PWM

PWM (Pulse Width Modulation) 可基于 32 比特递增计数器产生输出波形。计数时钟是 PWM 的总线时钟，并可进行 1~65536 倍的预分频。PWM 共有 5 个独立通道，其中 4 个通道可以输出独立周期和占空比的 PWM 或基于 FIFO 数据的自定义方波，另 1 个通道可以输出占空比渐变的呼吸灯 PWM。计数和输出比较的结果可以产生中断和 PTC 触发。

9.4.1 主要特性

- 4 路独立的 32 位递增自动重装载计数器，和 1 路 16 位递增自动重装载计数器
- 16 位可编程预分频器，计数器时钟频率的分频系数为 1~65536 之间的任意数值
- 16 位可配置重复计数
- 支持单笔计数模式 (OPM)，当重复计数完成后自动停止计数器
- 4 个独立的通用通道
  - 强制输出高/低电平
  - 计数到比较值时输出高/低/翻转电平
  - PWM 输出，可配脉宽和周期
  - 基于 FIFO 数据的自定义方波输出

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  - 单脉冲/重触发单脉冲模式输出
- 1 个专用通道，输出可配置峰谷时长的正弦函数呼吸灯 PWM
- 从模式
  - 支持多定时器互连，可作为从设备被其它主设备控制
  - 控制模式包括复位、触发、门控等
  - 支持多定时器同步启动、复位等
- 如下事件发生时产生中断/DMA 请求/PTC 触发：
  - 更新：计数器递增溢出/递减溢出，计数器初始化 (通过软件或者内部/外部触发)
  - 输出比较
  - FIFO 下溢出

9.4.2 结构图

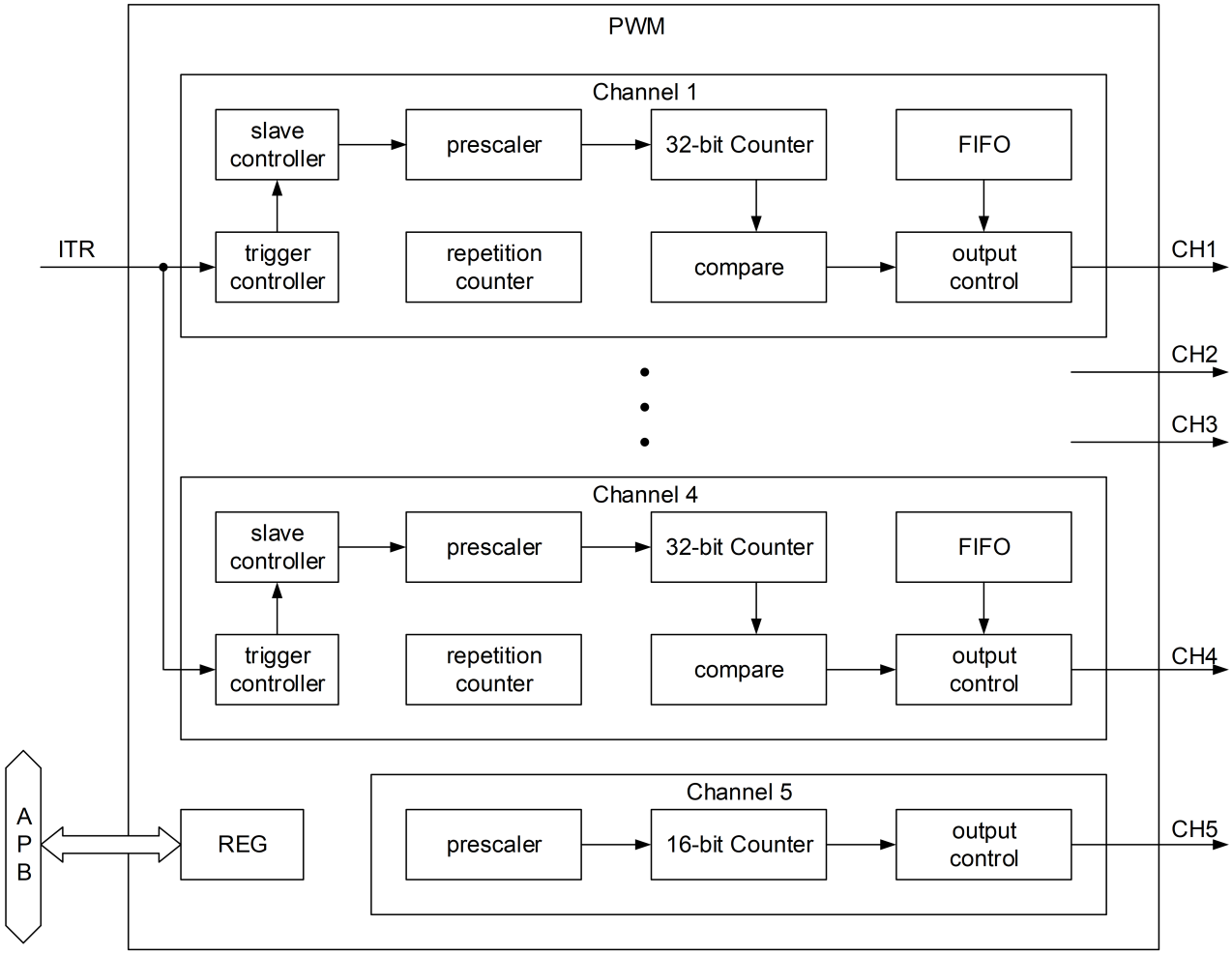


图 9-13: GPDMA 结构图

9.4.3 计数器

PWM 每个通道有独立的计数器，其中通道 1~4 基于 32 比特的计数器，而通道 5 基于 16 比特计数器。

计数器基于总线时钟计数。总线时钟经过预分频处理才会真正进入计数器。预分频的次数介于 1 到 65536 之间

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(PSCx+1)，即仅当发生了 (PSCx+1) 次总线时钟翻转，计数器的值才真正改变一次。每个通道的预分频可以独立设置。

计数器固定为递增计数模式，计数器从 0 计数到自动重载值 ARR，然后重新从 0 开始计数并产生计数器上溢事件。计数值可以通过CNTx 读出。

9.4.4 更新事件 (UEV)

更新事件用于标志一个计数单元的结束。最基本的更新事件产生于每次计数器上溢时 (未开启重复计数时)。软件将EGR_UGx 置 1 时，也将产生更新事件。更新事件可以产生中断、DMA 请求以及 PTC 触发，是定时器最基本的一项通知功能。

通过软件将CRx_UDIS置 1 可禁止产生更新事件。这可避免向预装载寄存器写入新值时更新影子寄存器。在 UDIS 位写入 0 之前不会产生任何更新事件。

如果CRx_URS（更新请求选择）已置 1，则将EGR_UGx 置 1 会生成更新事件，但不会将 UIF 标志置 1（因此，不会发送任何中断或 DMA 请求）。

发生更新事件时，将重新装载 RCR，ARR 以及 PSC 寄存器，且将更新标志SR_UIF置 1（CRx_URS=0 时）。该功能可以保证修改这些计数器的基本参数不影响当前计数单元，在下一个计数周期才生效。

9.4.5 重复计数

在通道 1~4 中，如果配置了重复计数器 (RCRx>0)，每次计数器上溢时重复计数器会递减，并仅当重复计数器为 0 时才产生更新事件。更新事件发生时，重复计数器会重新装载RCRx 的值。

重复计数器的当前值不能读出。

利用重复计数器可以在产生更新事件之前，将当前设置的 PWM 脉冲重复若干个周期。配合单脉冲模式使用，可以产生指定次数的 PWM 脉冲。

9.4.6 影子寄存器

对 RCR，ARR 以及 PSC 寄存器的修改不会直接体现在当前计数单元中，而是等到更新事件发生时才真正更新进去。在更新事件发生前，计数器真正使用的是影子寄存器中的值。这样即使在计数中动态改变这些寄存器的值，也不会影响到当前计数单元的完整性，对于动态改变 PWM 参数很有意义。

如果CRx_APRE为 0，ARR 寄存器将在配置后实时生效，不用等到更新事件发生。

输出比较寄存器 CCRx 也有影子寄存器。当CRx_OCPE为 0 时，配置的 CCRx 会立即生效，否则要等到更新事件发生时才生效。

9.4.7 从模式

从模式可以选择计数器复位、触发启动、计数使能等行为，由CRx_SMS选择。从模式依赖的触发信号 TRGI 可以在 ITR 输入中通过CRx_TS选择，并可选择信号极性。

- 定时器处于**复位从模式** (CRx_SMS=0100) 时，当 TRGI 发生变化时，计数器及其预分频器重新初始化。如果CRx_URS为 0，则会生成更新事件 UEV，然后预装载寄存器 ARRx 和 CCRx 都将更新。

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- 定时器处于**门控从模式** (CRx_SMS=0101) 时，当 TRGI 满足高电平或低电平要求时才进行计数，否则计数器不变。
- 定时器处于**触发从模式** (CRx_SMS=0110) 时，软件不需配置CRx_CEN开启计数，而是当 TRGI 满足特定触发要求时自动启动计数器。
- 定时器处于**复位触发从模式** (CRx_SMS=1000) 时，TRGI 满足特定触发要求时复位计数器并自动重新开启。

9.4.8 通道输出

通道 1~4 将比较各自计数器的值与 CCRx 的大小，在各自的通道输出 CHx 上产生固定电平，或产生基于本通道比较结果的 PWM 输出信号，并产生中断等通知信号。每个通道产生 PWM 信号的脉冲个数、频率、占空比等参数均可调节。通道产生的通知信号包括中断和 PTC 触发。

9.4.9 输出比较模式

在输出比较模式下，当计数值与 CCRx 满足一定关系时，可以在对应 CHx 上产生特定输出。

具体而言，通道将在 CCRx 与计数器之间相匹配时执行下列操作：

1. 将为相应的 CHx 输出分配一个可编程值，该值由比较模式寄存器CRx_OCM和输出极性寄存器CRx_CCP定义。匹配时，输出引脚既可保持其电平（CRx_OCM=0000），也可设置为有效电平 (CRx_OCM=0001)、无效电平 (CRx_OCM=0010) 或进行翻转 (CRx_OCM=0011)。
2. 将中断状态寄存器标志SR_CCIFx 置 1。
3. 根据IER_CCIEx生成中断。

通过CRx_OCPE寄存器，可将 CCRx 配置为带或不带影子寄存器。当CRx_OCPE为 0 时，软件修改 CCRx 实时生效，可通过在每次中断中修改下一次匹配的 CCRx 来实现自定义波形的输出。

9.4.10 基于比较值的 PWM 输出

利用输出比较模式，通道 1~4 可以产生周期和占空比独立可控的 PWM 输出。PWM 输出的周期由 ARRx 决定，占空比由 CCRx 决定。

每个通道的计数器值CNTx 与 CCRx 进行比较，产生包含有效电平或无效电平的比较输出信号。有效电平的极性可通过CRx_CCP配置，并根据CRx_CCE寄存器使能 CHx 输出。

如配置CR1_OCM和CR2_OCM为 0110(0x6)，则 PWM 输出如图9-14所示。其中计数值CNTx 小于 CCRx 时，输出高电平，否则输出低电平。

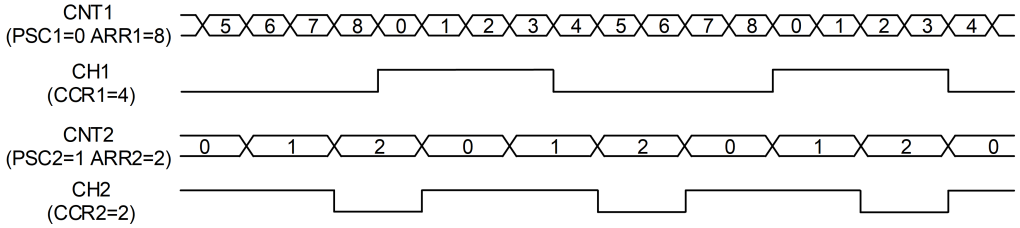


图 9-14: **PWM 输出示例**

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9.4.11 基于 FIFO 的自定义方波输出

通道 1~4 支持基于 FIFO 的自定义方波输出，通过将CRx_OCM设置为 1000(0x8) 使能。每个通道拥有深度为 8 字节的 FIFO，可根据 FIFO 中的数据按比特顺序输出自定义的方波，其中数据的每个比特 1 代表有效电平，比特 0 代表无效电平，每个比特的电平持续时间是经过预分频的一个计数周期。FIFO 的数据通过 FIFOx 寄存器输入，写入之前应先将EGR_APLOADx 置 1 以清空 FIFO，然后以字节为单元依次写入数据。FIFO 内的数据按照字节先写入先输出的原则产生方波，每个字节内的比特顺序由CRx_APMSB定义，为 1 时先从最高位 (MSB) 比特输出。当计数器未使能，或 FIFO 内的数据未准备好时，输出电平由CRx_APIDLE配置，为 1 输出有效电平，为 0 输出无效电平。有效电平的极性通过CRx_CCP配置。

自定义方波时，可选择非 DMA 或 DMA 两种模式。CRx_APDMA为 0 时处于非 DMA 模式，FIFO 数据直接通过 CPU 写入，一段自定义方波最长可持续 64 个计数周期，并可重复指定次数或无限重复，重复时 FIFO 内数据被重新使用。

非 DMA 模式下，一段自定义方波的长度应不大于 64 个计数周期，计数周期数等于ARRx+1。CRx_OPM为 1 时，这段自定义方波的重复次数等于RCRx+1，CRx_OPM为 0 时则会无限重复。

非 DMA 模式下 CPU 启动自定义方波输出的流程为：

1. 设置预分频 PSCx，通过 ARRx 设置自定义方波周期数，通过 RCRx 设置总段数；
2. EGR_UGx 置 1 刷新影子寄存器，EGR_APLOADx 置 1 清空 FIFO；
3. CRx_APDMA设为 0，CRx_OCM设为 0x8，设置输出比特顺序CRx_APMSB，默认输出电平CRx_APIDLE，有效电平极性CRx_CCP，单脉冲模式CRx_OPM，将CRx_CCE置 1 使能通道输出；
4. CPU 以字节为单元向 FIFOx 写入所有数据；
5. 将CRx_CEN置 1，使能计数器。

下图是非 DMA 模式下自定义方波示例。向 FIFOx 依次写入 0xec 与 0x8a，并启动计数器以后，不同配置下的输出自定义方波波形如图所示。

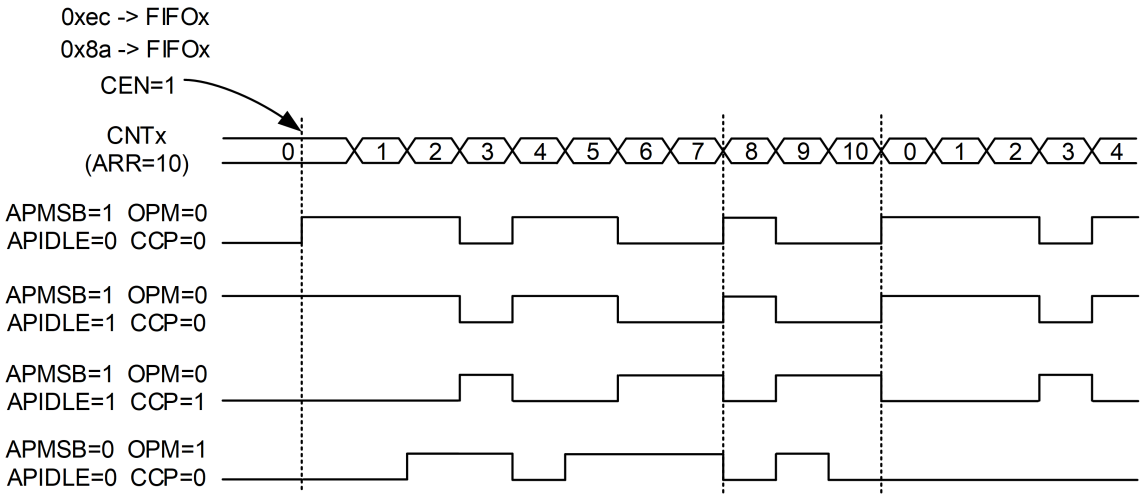


图 9-15: 非 DMA 模式自定义方波示例

DMA 模式下，一段自定义方波的长度可扩展到 2^{32} 个计数周期，计数周期数等于ARRx+1。CRx_OPM为 1 时，输出自定义方波的总段数等于RCRx+1，但每一段自定义方波的输出样式都由 DMA 搬运的数据决定，可以发生变化。CRx_OPM为 0 时则会无限输出自定义方波，输出样式由 DMA 搬运的数据决定。

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DMA 以字节为单元搬运数据，当一段自定义方波的计数周期数不是 8 的整数倍时，数据最后一个字节内多余的比特会被丢弃，新一段自定义方波的数据从下一个字节开始。

在自定义方波输出过程中，如果因为总线繁忙等原因造成 DMA 搬运不及时，FIFO 数据产生了下溢出，自定义方波会输出由CRx_APIDLE决定的电平，SR_UFIFx 标志会拉高，并可产生中断。

DMA 模式下 CPU 启动自定义方波输出的流程为：

1. 配置 DMA 模块为外设传输模式，请求源选择 PWM 对应通道，目标地址为 FIFOx，传输单元为字节，总数据量等于每一段自定义方波的字节数乘以总段数。
2. 设置预分频 PSCx，通过 ARRx 设置自定义方波周期数，通过 RCRx 设置总段数；
3. EGR_UGx 置 1 刷新影子寄存器；
4. CRx_APDMA设为 1，CRx_OCM设为 0x8，设置输出比特顺序CRx_APMSB，默认输出电平CRx_APIDLE，有效电平极性CRx_CCP，单脉冲模式CRx_OPM，将CRx_CCE置 1 使能通道输出；
5. EGR_APLOADx 置 1 启动 DMA 搬运；
6. 查询EGR_APLOADx，直到EGR_APLOADx 为 1，表示 DMA 已经完成第 1 个字节搬运；
7. 将CRx_CEN置 1，使能计数器。

下图是 DMA 模式下自定义方波示例。每一段自定义方波长度为 28 个计数周期，需占用 4 个字节的内存空间。DMA 持续向 FIFOx 搬运数据以支持自定义方波持续产生输出。

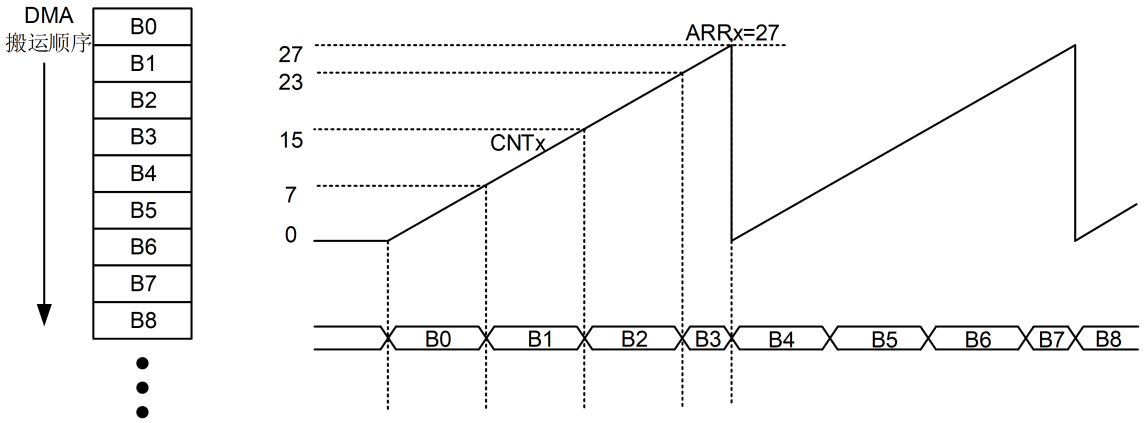


图 9-16: DMA 模式自定义方波示例

9.4.12 单脉冲模式

将CRx_OPM写 1 可以使能单脉冲模式。该模式下计数器启动以后一旦发生更新事件，就会自动停止计数。该模式可以用于产生单个脉宽的输出。RCRx 寄存器可以设定发生更新事件之前的重复次数，因此单脉冲模式也可用于产生指定次数个脉冲输出。

在自定义方波输出时，单脉冲模式可以用于产生指定次数的自定义方波。

9.4.13 呼吸灯 PWM 输出

通道 5 专用于产生呼吸灯 PWM 输出。呼吸灯样式为正弦函数，支持调节呼吸频率，变化快慢，最高亮度等参数。

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通道 5 具有独立的 16 比特计数器，由总线时钟经过预分频产生计数，分频比为PSC5+1。通过调节 PSC5 可以调节呼吸灯的计数周期。

单次由暗到明或由明到暗的变化包含 32 个阶梯，每个阶梯的持续时间是 (RCR5+1) 个计数周期。调节 RCR5 可以配置呼吸灯的变化快慢。

ARR5 用于调整 PWM 占空比，从而改变呼吸灯的最高亮度。当 ARR5 为 0x80 时 PWM 占空比最大，亮度最高，增大 ARR5 会相应降低亮度。

最高亮度和最低亮度的持续时间可通过INTV5_PEAK和INTV5_IDLE调节，从而改变呼吸频率。

9.4.14 通知机制

PWM 能够产生中断和 PTC 触发。能够触发通知的事件主要包括更新事件、比较器匹配、FIFO 下溢出等。IER 寄存器可以控制各种事件是否产生中断。各事件状态可在 SR 寄存器中查询。

9.4.15 PWM 寄存器

PWM 的基地址是 0x500B3000。

表 9-5: PWM 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**IER**	Interrupt enable register
[31:20]			RSVD	
[19]	rw	1'h0	UFIE4	Channel 4 FIFO underflow interrupt enable 0: FIFO underflow interrupt disabled. 1: FIFO underflow interrupt enabled
[18]	rw	1'h0	UFIE3	Channel 3 FIFO underflow interrupt enable 0: FIFO underflow interrupt disabled. 1: FIFO underflow interrupt enabled
[17]	rw	1'h0	UFIE2	Channel 2 FIFO underflow interrupt enable 0: FIFO underflow interrupt disabled. 1: FIFO underflow interrupt enabled
[16]	rw	1'h0	UFIE1	Channel 1 FIFO underflow interrupt enable 0: FIFO underflow interrupt disabled. 1: FIFO underflow interrupt enabled
[15:12]			RSVD	
[11]	rw	1'h0	CCIE4	Channel 4 compare interrupt enable 0: CC4 interrupt disabled. 1: CC4 interrupt enabled
[10]	rw	1'h0	CCIE3	Channel 3 compare interrupt enable 0: CC3 interrupt disabled. 1: CC3 interrupt enabled
[9]	rw	1'h0	CCIE2	Channel 2 compare interrupt enable 0: CC2 interrupt disabled. 1: CC2 interrupt enabled
[8]	rw	1'h0	CCIE1	Channel 1 compare interrupt enable 0: CC1 interrupt disabled. 1: CC1 interrupt enabled
[7:5]			RSVD	

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表 9-5: PWM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4]	rw	1'h0	UIE5	Channel 5 update interrupt enable 0: Update interrupt disabled. 1: Update interrupt enabled
[3]	rw	1'h0	UIE4	Channel 4 update interrupt enable 0: Update interrupt disabled. 0: Update interrupt enabled
[2]	rw	1'h0	UIE3	Channel 3 update interrupt enable 0: Update interrupt disabled. 0: Update interrupt enabled
[1]	rw	1'h0	UIE2	Channel 2 update interrupt enable 0: Update interrupt disabled. 1: Update interrupt enabled
[0]	rw	1'h0	UIE1	Channel 1 update interrupt enable 0: Update interrupt disabled. 1: Update interrupt enabled
0x04			**SR**	Interrupt status register
[31:20]			RSVD	
[19]	rw0c	1'h0	UFIF4	Channel 4 FIFO underflow interrupt flag
[18]	rw0c	1'h0	UFIF3	Channel 3 FIFO underflow interrupt flag
[17]	rw0c	1'h0	UFIF2	Channel 2 FIFO underflow interrupt flag
[16]	rw0c	1'h0	UFIF1	Channel 1 FIFO underflow interrupt flag 0: No FIFO underflow. 1: FIFO underflow occur
[15:12]			RSVD	
[11]	rw0c	1'h0	CCIF4	Channel 4 compare interrupt flag
[10]	rw0c	1'h0	CCIF3	Channel 3 compare interrupt flag
[9]	rw0c	1'h0	CCIF2	Channel 2 compare interrupt flag
[8]	rw0c	1'h0	CCIF1	Channel 1 compare interrupt flag This flag is set by hardware when the counter matches the compare value. It is cleared by software. 0: No match. 1: The content of the counter CNTx has matched the content of the CCRx register.
[7:5]			RSVD	
[4]	rw0c	1'h0	UIF5	Channel 5 update interrupt flag
[3]	rw0c	1'h0	UIF4	Channel 4 update interrupt flag
[2]	rw0c	1'h0	UIF3	Channel 3 update interrupt flag
[1]	rw0c	1'h0	UIF2	Channel 2 update interrupt flag
[0]	rw0c	1'h0	UIF1	Channel 1 update interrupt flag This bit is set by hardware on an update event. It is cleared by software. 0: No update occurred 1: Update interrupt pending. This bit is set by hardware when the registers are updated: - At overflow regarding the repetition counter value (update if repetition counter = 0) and if UDIS=0 in the CRx register. - When CNT is reinitialized by software using the UG bit in EGR register, if URS=0 and UDIS=0 in the CRx register. - When CNT is reinitialized by a trigger event, if URS=0 and UDIS=0 in the CRx register.
0x08			**EGR**	Event generation register

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表 9-5: PWM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:20]			RSVD	
[19]	rw	1'h0	APLOAD4	Channel 4 load data for arbitary pulse
[18]	rw	1'h0	APLOAD3	Channel 3 load data for arbitary pulse
[17]	rw	1'h0	APLOAD2	Channel 2 load data for arbitary pulse
[16]	rw	1'h0	APLOAD1	Channel 1 load data for arbitary pulse This bit can be set by software. It is automatically cleared by hardware if first FIFO byte is ready. write 0: No action write 1: reset fifo, and start data load if DMA enabled. In arbitary pulse mode, data must be pre-loaded before counter starts. By setting APLOAD, data fifo will be reset, then data should be filled by DMA or CPU. read 0: first FIFO byte ready read 1: first FIFO byte not ready yet
[15:12]			RSVD	
[11]	w	1'h0	TG4	Channel 4 trigger generation
[10]	w	1'h0	TG3	Channel 3 trigger generation
[9]	w	1'h0	TG2	Channel 2 trigger generation
[8]	w	1'h0	TG1	Channel 1 trigger generation This bit is set by software in order to generate an event, it is automatically cleared by hardware. 0: No action 1: trigger counter in slave reset/trigger mode.
[7:5]			RSVD	
[4]	w	1'h0	UG5	Channel 5 update generation
[3]	w	1'h0	UG4	Channel 4 update generation
[2]	w	1'h0	UG3	Channel 3 update generation
[1]	w	1'h0	UG2	Channel 2 update generation
[0]	w	1'h0	UG1	Channel 1 update generation This bit can be set by software, it is automatically cleared by hardware. 0: No action 1: Re-initialize the counter and generates an update of the registers. Note that the prescaler counter is cleared too (anyway the prescaler ratio is not affected). The counter is cleared.
0x0C			**CR1**	control register for channel 1
[31:23]			RSVD	
[22:20]	rw	3'h0	TS	Trigger selection This bit-field selects the trigger input to be used to synchronize the counter. 000: Internal Trigger 0 (ITR0) 001: Internal Trigger 1 (ITR1) 010: Internal Trigger 2 (ITR2) 011: Internal Trigger 3 (ITR3) Note: These bits must be changed only when they are not used (e.g. when SMS=000) to avoid wrong edge detections at the transition.

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表 9-5: PWM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[19:16]	rw	4'h0	SMS	Slave mode selection When external signals are selected the active edge of the trigger signal (TRGI) is linked to the polarity selected on the external input. 0000: Slave mode disabled - if CEN = '1 then the prescaler is clocked directly by the internal clock. 0100: Reset Mode - Rising edge of the selected trigger input (TRGI) reinitializes the counter and generates an update of the registers. 0101: Gated Mode - The counter clock is enabled when the trigger input (TRGI) is high. The counter stops (but is not reset) as soon as the trigger becomes low. Both start and stop of the counter are controlled. 0110: Trigger Mode - The counter starts at a rising edge of the trigger TRGI (but it is not reset). Only the start of the counter is controlled. 1000: Combined reset + trigger mode - Rising edge of the selected trigger input (TRGI) reinitializes the counter, generates an update of the registers and starts the counter.
[15]			RSVD	
[14]	rw	1'h0	APMSB	Most significant bit first in arbitary pulse mode 0: output from LSB of each byte in FIFO 1: output from MSB of each byte in FIFO
[13]	rw	1'h0	APDMA	Enable DMA in arbitary pulse mode 0: DMA not enabled, data should be filled by CPU 1: DMA enabled. Data will be filled by DMA after APLOAD set.
[12]	rw	1'h0	APIDLE	Default output level in arbitary pulse mode when counter not enabled 0: default output is low 1: default output is high
[11:8]	rw	4'h0	OCM	Output compare mode These bits define the behavior of the output reference signal. 0000: Frozen - The comparison between the output compare register CCRx and the counter CNTx has no effect on the outputs.(this mode is used to generate a timing base). 0001: Set to active level on match. Output signal is forced active when the counter CNTx matches CCRx. 0010: Set to inactive level on match. OC1REF signal is forced inactive when the counter CNTx matches CCRx. 0011: Toggle - output toggles when CNTx=CCRx. 0100: Force to inactive level. 0101: Force to active level. 0110: PWM mode 1 - Output is active as long as CNTx<CCRx else inactive. 0111: PWM mode 2 - Output is inactive as long as CNTx<CCRx else active. 1000: Arbitary pulse mode. Output is generated according to FIFO data filled by DMA or CPU. others: Reserved
[7]	rw	1'h0	ARPE	Auto-reload preload enable 0: ARRx register is not buffered 1: ARRx register is buffered

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表 9-5: PWM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[6]	rw	1'h0	OCPE	Output compare preload enable 0: Preload register on CCRx disabled. CCRx can be written at anytime, the new value is taken in account immediately. 1: Preload register on CCRx enabled. Read/Write operations access the preload register. CCRx preload value is loaded in the active register at each update event.
[5]	rw	1'h0	CCP	Compare output Polarity. 0: output active high 1: output active low
[4]	rw	1'h0	CCE	Compare output enable 0: Off - output is not active. No push-pull output. 1: On - output active.
[3]	rw	1'h0	OPM	One-pulse mode 0: Counter is not stopped at update event 1: Counter stops counting at the next update event (clearing the bit CEN)
[2]	rw	1'h0	URS	Update request source This bit is set and cleared by software to select the UEV event sources. 0: Any of the following events generate an update interrupt if enabled. These events can be: – Counter overflow – Setting the UG bit – Update generation through the slave mode controller 1: Only counter overflow generates an update interrupt if enabled.
[1]	rw	1'h0	UDIS	Update disable This bit is set and cleared by software to enable/disable UEV event generation. 0: UEV enabled. The Update (UEV) event is generated by one of the following events: – Counter overflow/underflow – Setting the UG bit – Update generation through the slave mode controller Buffered registers are then loaded with their preload values. 1: UEV disabled. The Update event is not generated, shadow registers keep their value (ARRx, PSCx, CCRx). However the counter and the prescaler are reinitialized if the UG bit is set or if a hardware reset is received from the slave mode controller.
[0]	rw	1'h0	CEN	Counter enable 0: Counter disabled 1: Counter enabled Note: Gated mode can work only if the CEN bit has been previously set by software. However trigger mode can set the CEN bit automatically by hardware. CEN is cleared automatically in one-pulse mode, when an update event occurs.
0x14			**CNT1**	Counter for channel 1
[31:0]	rw	32'h0	CNT	current counter value
0x18			**PSC1**	Prescaler for channel 1
[31:16]			RSVD	
[15:0]	rw	16'h0	PSC	Prescaler value The counter clock frequency is fpclk/(PSC+1). PSC contains the value to be loaded in the active prescaler register at each update event (including when the counter is cleared through UG bit of EGR register or through trigger controller when configured in "reset mode").

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表 9-5: PWM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x1C			**ARR1**	Auto-reload register for channel 1
[31:0]	rw	32'h0	ARR	Auto-reload value ARR is the value to be loaded in the actual auto-reload register. In arbitary mode, ARR defines the total output bit of one PWM period.
0x20			**RCR1**	Repetition counter register for channel 1
[31:16]			RSVD	
[15:0]	rw	16'h0	REP	Repetition counter value These bits allow the user to set-up the update rate of the compare registers (i.e. periodic transfers from preload to active registers) when preload registers are enable, as well as the update interrupt generation rate, if this interrupt is enable. Each time the REP_CNT related downcounter reaches zero, an update event is generated and it restarts counting from REP value. As REP_CNT is reloaded with REP value only at the repetition update event, any write to the RCRx register is not taken in account until the next repetition update event. It means in PWM mode (REP+1) corresponds to the number of PWM periods.
0x24			**CCR1**	Compare register for channel 1
[31:0]	rw	32'h0	CCR	Compare value CCR is the value to be loaded in the actual compare register (preload value).It is loaded permanently if the preload feature is not selected in the CR register (bit OCPE). Else the preload value is copied in the active compare register when an update event occurs. The active compare register contains the value to be compared to the counter and signaled on output.
0x28			**FIFO1**	FIFO for channel 1
[31:8]			RSVD	
[7:0]	w	8'h0	DATA	Entry of data FIFO in arbitary pulse mode. DMA or CPU will write data to this register to fill data FIFO.
0x2C			**CR2**	control register for channel 2
[31:23]			RSVD	
[22:20]	rw	3'h0	TS	Trigger selection This bit-field selects the trigger input to be used to synchronize the counter. 000: Internal Trigger 0 (ITR0) 001: Internal Trigger 1 (ITR1) 010: Internal Trigger 2 (ITR2) 011: Internal Trigger 3 (ITR3) Note: These bits must be changed only when they are not used (e.g. when SMS=000) to avoid wrong edge detections at the transition.

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表 9-5: PWM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[19:16]	rw	4'h0	SMS	Slave mode selection When external signals are selected the active edge of the trigger signal (TRGI) is linked to the polarity selected on the external input. 0000: Slave mode disabled - if CEN = '1 then the prescaler is clocked directly by the internal clock. 0100: Reset Mode - Rising edge of the selected trigger input (TRGI) reinitializes the counter and generates an update of the registers. 0101: Gated Mode - The counter clock is enabled when the trigger input (TRGI) is high. The counter stops (but is not reset) as soon as the trigger becomes low. Both start and stop of the counter are controlled. 0110: Trigger Mode - The counter starts at a rising edge of the trigger TRGI (but it is not reset). Only the start of the counter is controlled. 1000: Combined reset + trigger mode - Rising edge of the selected trigger input (TRGI) reinitializes the counter, generates an update of the registers and starts the counter.
[15]			RSVD	
[14]	rw	1'h0	APMSB	Most significant bit first in arbitary pulse mode 0: output from LSB of each byte in FIFO 1: output from MSB of each byte in FIFO
[13]	rw	1'h0	APDMA	Enable DMA in arbitary pulse mode 0: DMA not enabled, data should be filled by CPU 1: DMA enabled. Data will be filled by DMA after APLOAD set.
[12]	rw	1'h0	APIDLE	Default output level in arbitary pulse mode when counter not enabled 0: default output is low 1: default output is high
[11:8]	rw	4'h0	OCM	Output compare mode These bits define the behavior of the output reference signal. 0000: Frozen - The comparison between the output compare register CCRx and the counter CNTx has no effect on the outputs.(this mode is used to generate a timing base). 0001: Set to active level on match. Output signal is forced active when the counter CNTx matches CCRx. 0010: Set to inactive level on match. OC1REF signal is forced inactive when the counter CNTx matches CCRx. 0011: Toggle - output toggles when CNTx=CCRx. 0100: Force to inactive level. 0101: Force to active level. 0110: PWM mode 1 - Output is active as long as CNTx<CCRx else inactive. 0111: PWM mode 2 - Output is inactive as long as CNTx<CCRx else active. 1000: Arbitary pulse mode. Output is generated according to FIFO data filled by DMA or CPU. others: Reserved
[7]	rw	1'h0	ARPE	Auto-reload preload enable 0: ARRx register is not buffered 1: ARRx register is buffered

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表 9-5: PWM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[6]	rw	1'h0	OCPE	Output compare preload enable 0: Preload register on CCRx disabled. CCRx can be written at anytime, the new value is taken in account immediately. 1: Preload register on CCRx enabled. Read/Write operations access the preload register. CCRx preload value is loaded in the active register at each update event.
[5]	rw	1'h0	CCP	Compare output Polarity. 0: output active high 1: output active low
[4]	rw	1'h0	CCE	Compare output enable 0: Off - output is not active. No push-pull output. 1: On - output active.
[3]	rw	1'h0	OPM	One-pulse mode 0: Counter is not stopped at update event 1: Counter stops counting at the next update event (clearing the bit CEN)
[2]	rw	1'h0	URS	Update request source This bit is set and cleared by software to select the UEV event sources. 0: Any of the following events generate an update interrupt if enabled. These events can be: – Counter overflow – Setting the UG bit – Update generation through the slave mode controller 1: Only counter overflow generates an update interrupt if enabled.
[1]	rw	1'h0	UDIS	Update disable This bit is set and cleared by software to enable/disable UEV event generation. 0: UEV enabled. The Update (UEV) event is generated by one of the following events: – Counter overflow/underflow – Setting the UG bit – Update generation through the slave mode controller Buffered registers are then loaded with their preload values. 1: UEV disabled. The Update event is not generated, shadow registers keep their value (ARRx, PSCx, CCRx). However the counter and the prescaler are reinitialized if the UG bit is set or if a hardware reset is received from the slave mode controller.
[0]	rw	1'h0	CEN	Counter enable 0: Counter disabled 1: Counter enabled Note: Gated mode can work only if the CEN bit has been previously set by software. However trigger mode can set the CEN bit automatically by hardware. CEN is cleared automatically in one-pulse mode, when an update event occurs.
0x34			**CNT2**	Counter for channel 2
[31:0]	rw	32'h0	CNT	current counter value
0x38			**PSC2**	Prescaler for channel 2
[31:16]			RSVD	
[15:0]	rw	16'h0	PSC	Prescaler value The counter clock frequency is fpclk/(PSC+1). PSC contains the value to be loaded in the active prescaler register at each update event (including when the counter is cleared through UG bit of EGR register or through trigger controller when configured in "reset mode").

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表 9-5: PWM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x3C			**ARR2**	Auto-reload register for channel 2
[31:0]	rw	32'h0	ARR	Auto-reload value ARR is the value to be loaded in the actual auto-reload register. In arbitary mode, ARR defines the total output bit of one PWM period.
0x40			**RCR2**	Repetition counter register for channel 2
[31:16]			RSVD	
[15:0]	rw	16'h0	REP	Repetition counter value These bits allow the user to set-up the update rate of the compare registers (i.e. periodic transfers from preload to active registers) when preload registers are enable, as well as the update interrupt generation rate, if this interrupt is enable. Each time the REP_CNT related downcounter reaches zero, an update event is generated and it restarts counting from REP value. As REP_CNT is reloaded with REP value only at the repetition update event, any write to the RCRx register is not taken in account until the next repetition update event. It means in PWM mode (REP+1) corresponds to the number of PWM periods.
0x44			**CCR2**	Compare register for channel 2
[31:0]	rw	32'h0	CCR	Compare value CCR is the value to be loaded in the actual compare register (preload value).It is loaded permanently if the preload feature is not selected in the CR register (bit OCPE). Else the preload value is copied in the active compare register when an update event occurs. The active compare register contains the value to be compared to the counter and signaled on output.
0x48			**FIFO2**	FIFO for channel 2
[31:8]			RSVD	
[7:0]	w	8'h0	DATA	Entry of data FIFO in arbitary pulse mode. DMA or CPU will write data to this register to fill data FIFO.
0x4C			**CR3**	control register for channel 3
[31:23]			RSVD	
[22:20]	rw	3'h0	TS	Trigger selection This bit-field selects the trigger input to be used to synchronize the counter. 000: Internal Trigger 0 (ITR0) 001: Internal Trigger 1 (ITR1) 010: Internal Trigger 2 (ITR2) 011: Internal Trigger 3 (ITR3) Note: These bits must be changed only when they are not used (e.g. when SMS=000) to avoid wrong edge detections at the transition.

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表 9-5: PWM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[19:16]	rw	4'h0	SMS	Slave mode selection When external signals are selected the active edge of the trigger signal (TRGI) is linked to the polarity selected on the external input. 0000: Slave mode disabled - if CEN = '1 then the prescaler is clocked directly by the internal clock. 0100: Reset Mode - Rising edge of the selected trigger input (TRGI) reinitializes the counter and generates an update of the registers. 0101: Gated Mode - The counter clock is enabled when the trigger input (TRGI) is high. The counter stops (but is not reset) as soon as the trigger becomes low. Both start and stop of the counter are controlled. 0110: Trigger Mode - The counter starts at a rising edge of the trigger TRGI (but it is not reset). Only the start of the counter is controlled. 1000: Combined reset + trigger mode - Rising edge of the selected trigger input (TRGI) reinitializes the counter, generates an update of the registers and starts the counter.
[15]			RSVD	
[14]	rw	1'h0	APMSB	Most significant bit first in arbitary pulse mode 0: output from LSB of each byte in FIFO 1: output from MSB of each byte in FIFO
[13]	rw	1'h0	APDMA	Enable DMA in arbitary pulse mode 0: DMA not enabled, data should be filled by CPU 1: DMA enabled. Data will be filled by DMA after APLOAD set.
[12]	rw	1'h0	APIDLE	Default output level in arbitary pulse mode when counter not enabled 0: default output is low 1: default output is high
[11:8]	rw	4'h0	OCM	Output compare mode These bits define the behavior of the output reference signal. 0000: Frozen - The comparison between the output compare register CCRx and the counter CNTx has no effect on the outputs.(this mode is used to generate a timing base). 0001: Set to active level on match. Output signal is forced active when the counter CNTx matches CCRx. 0010: Set to inactive level on match. OC1REF signal is forced inactive when the counter CNTx matches CCRx. 0011: Toggle - output toggles when CNTx=CCRx. 0100: Force to inactive level. 0101: Force to active level. 0110: PWM mode 1 - Output is active as long as CNTx<CCRx else inactive. 0111: PWM mode 2 - Output is inactive as long as CNTx<CCRx else active. 1000: Arbitary pulse mode. Output is generated according to FIFO data filled by DMA or CPU. others: Reserved
[7]	rw	1'h0	ARPE	Auto-reload preload enable 0: ARRx register is not buffered 1: ARRx register is buffered

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表 9-5: PWM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[6]	rw	1'h0	OCPE	Output compare preload enable 0: Preload register on CCRx disabled. CCRx can be written at anytime, the new value is taken in account immediately. 1: Preload register on CCRx enabled. Read/Write operations access the preload register. CCRx preload value is loaded in the active register at each update event.
[5]	rw	1'h0	CCP	Compare output Polarity. 0: output active high 1: output active low
[4]	rw	1'h0	CCE	Compare output enable 0: Off - output is not active. No push-pull output. 1: On - output active.
[3]	rw	1'h0	OPM	One-pulse mode 0: Counter is not stopped at update event 1: Counter stops counting at the next update event (clearing the bit CEN)
[2]	rw	1'h0	URS	Update request source This bit is set and cleared by software to select the UEV event sources. 0: Any of the following events generate an update interrupt if enabled. These events can be: – Counter overflow – Setting the UG bit – Update generation through the slave mode controller 1: Only counter overflow generates an update interrupt if enabled.
[1]	rw	1'h0	UDIS	Update disable This bit is set and cleared by software to enable/disable UEV event generation. 0: UEV enabled. The Update (UEV) event is generated by one of the following events: – Counter overflow/underflow – Setting the UG bit – Update generation through the slave mode controller Buffered registers are then loaded with their preload values. 1: UEV disabled. The Update event is not generated, shadow registers keep their value (ARRx, PSCx, CCRx). However the counter and the prescaler are reinitialized if the UG bit is set or if a hardware reset is received from the slave mode controller.
[0]	rw	1'h0	CEN	Counter enable 0: Counter disabled 1: Counter enabled Note: Gated mode can work only if the CEN bit has been previously set by software. However trigger mode can set the CEN bit automatically by hardware. CEN is cleared automatically in one-pulse mode, when an update event occurs.
0x54			**CNT3**	Counter for channel 3
[31:0]	rw	32'h0	CNT	current counter value
0x58			**PSC3**	Prescaler for channel 3
[31:16]			RSVD	
[15:0]	rw	16'h0	PSC	Prescaler value The counter clock frequency is fpclk/(PSC+1). PSC contains the value to be loaded in the active prescaler register at each update event (including when the counter is cleared through UG bit of EGR register or through trigger controller when configured in "reset mode").

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表 9-5: PWM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x5C			**ARR3**	Auto-reload register for channel 3
[31:0]	rw	32'h0	ARR	Auto-reload value ARR is the value to be loaded in the actual auto-reload register. In arbitary mode, ARR defines the total output bit of one PWM period.
0x60			**RCR3**	Repetition counter register for channel 3
[31:16]			RSVD	
[15:0]	rw	16'h0	REP	Repetition counter value These bits allow the user to set-up the update rate of the compare registers (i.e. periodic transfers from preload to active registers) when preload registers are enable, as well as the update interrupt generation rate, if this interrupt is enable. Each time the REP_CNT related downcounter reaches zero, an update event is generated and it restarts counting from REP value. As REP_CNT is reloaded with REP value only at the repetition update event, any write to the RCRx register is not taken in account until the next repetition update event. It means in PWM mode (REP+1) corresponds to the number of PWM periods.
0x64			**CCR3**	Compare register for channel 3
[31:0]	rw	32'h0	CCR	Compare value CCR is the value to be loaded in the actual compare register (preload value).It is loaded permanently if the preload feature is not selected in the CR register (bit OCPE). Else the preload value is copied in the active compare register when an update event occurs. The active compare register contains the value to be compared to the counter and signaled on output.
0x68			**FIFO3**	FIFO for channel 3
[31:8]			RSVD	
[7:0]	w	8'h0	DATA	Entry of data FIFO in arbitary pulse mode. DMA or CPU will write data to this register to fill data FIFO.
0x6C			**CR4**	control register for channel 4
[31:23]			RSVD	
[22:20]	rw	3'h0	TS	Trigger selection This bit-field selects the trigger input to be used to synchronize the counter. 000: Internal Trigger 0 (ITR0) 001: Internal Trigger 1 (ITR1) 010: Internal Trigger 2 (ITR2) 011: Internal Trigger 3 (ITR3) Note: These bits must be changed only when they are not used (e.g. when SMS=000) to avoid wrong edge detections at the transition.

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表 9-5: PWM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[19:16]	rw	4'h0	SMS	Slave mode selection When external signals are selected the active edge of the trigger signal (TRGI) is linked to the polarity selected on the external input. 0000: Slave mode disabled - if CEN = '1 then the prescaler is clocked directly by the internal clock. 0100: Reset Mode - Rising edge of the selected trigger input (TRGI) reinitializes the counter and generates an update of the registers. 0101: Gated Mode - The counter clock is enabled when the trigger input (TRGI) is high. The counter stops (but is not reset) as soon as the trigger becomes low. Both start and stop of the counter are controlled. 0110: Trigger Mode - The counter starts at a rising edge of the trigger TRGI (but it is not reset). Only the start of the counter is controlled. 1000: Combined reset + trigger mode - Rising edge of the selected trigger input (TRGI) reinitializes the counter, generates an update of the registers and starts the counter.
[15]			RSVD	
[14]	rw	1'h0	APMSB	Most significant bit first in arbitary pulse mode 0: output from LSB of each byte in FIFO 1: output from MSB of each byte in FIFO
[13]	rw	1'h0	APDMA	Enable DMA in arbitary pulse mode 0: DMA not enabled, data should be filled by CPU 1: DMA enabled. Data will be filled by DMA after APLOAD set.
[12]	rw	1'h0	APIDLE	Default output level in arbitary pulse mode when counter not enabled 0: default output is low 1: default output is high
[11:8]	rw	4'h0	OCM	Output compare mode These bits define the behavior of the output reference signal. 0000: Frozen - The comparison between the output compare register CCRx and the counter CNTx has no effect on the outputs.(this mode is used to generate a timing base). 0001: Set to active level on match. Output signal is forced active when the counter CNTx matches CCRx. 0010: Set to inactive level on match. OC1REF signal is forced inactive when the counter CNTx matches CCRx. 0011: Toggle - output toggles when CNTx=CCRx. 0100: Force to inactive level. 0101: Force to active level. 0110: PWM mode 1 - Output is active as long as CNTx<CCRx else inactive. 0111: PWM mode 2 - Output is inactive as long as CNTx<CCRx else active. 1000: Arbitary pulse mode. Output is generated according to FIFO data filled by DMA or CPU. others: Reserved
[7]	rw	1'h0	ARPE	Auto-reload preload enable 0: ARRx register is not buffered 1: ARRx register is buffered

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表 9-5: PWM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[6]	rw	1'h0	OCPE	Output compare preload enable 0: Preload register on CCRx disabled. CCRx can be written at anytime, the new value is taken in account immediately. 1: Preload register on CCRx enabled. Read/Write operations access the preload register. CCRx preload value is loaded in the active register at each update event.
[5]	rw	1'h0	CCP	Compare output Polarity. 0: output active high 1: output active low
[4]	rw	1'h0	CCE	Compare output enable 0: Off - output is not active. No push-pull output. 1: On - output active.
[3]	rw	1'h0	OPM	One-pulse mode 0: Counter is not stopped at update event 1: Counter stops counting at the next update event (clearing the bit CEN)
[2]	rw	1'h0	URS	Update request source This bit is set and cleared by software to select the UEV event sources. 0: Any of the following events generate an update interrupt if enabled. These events can be: – Counter overflow – Setting the UG bit – Update generation through the slave mode controller 1: Only counter overflow generates an update interrupt if enabled.
[1]	rw	1'h0	UDIS	Update disable This bit is set and cleared by software to enable/disable UEV event generation. 0: UEV enabled. The Update (UEV) event is generated by one of the following events: – Counter overflow/underflow – Setting the UG bit – Update generation through the slave mode controller Buffered registers are then loaded with their preload values. 1: UEV disabled. The Update event is not generated, shadow registers keep their value (ARRx, PSCx, CCRx). However the counter and the prescaler are reinitialized if the UG bit is set or if a hardware reset is received from the slave mode controller.
[0]	rw	1'h0	CEN	Counter enable 0: Counter disabled 1: Counter enabled Note: Gated mode can work only if the CEN bit has been previously set by software. However trigger mode can set the CEN bit automatically by hardware. CEN is cleared automatically in one-pulse mode, when an update event occurs.
0x74			**CNT4**	Counter for channel 4
[31:0]	rw	32'h0	CNT	current counter value
0x78			**PSC4**	Prescaler for channel 4
[31:16]			RSVD	
[15:0]	rw	16'h0	PSC	Prescaler value The counter clock frequency is fpclk/(PSC+1). PSC contains the value to be loaded in the active prescaler register at each update event (including when the counter is cleared through UG bit of EGR register or through trigger controller when configured in "reset mode").

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表 9-5: PWM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x7C			**ARR4**	Auto-reload register for channel 4
[31:0]	rw	32'h0	ARR	Auto-reload value ARR is the value to be loaded in the actual auto-reload register. In arbitary mode, ARR defines the total output bit of one PWM period.
0x80			**RCR4**	Repetition counter register for channel 4
[31:16]			RSVD	
[15:0]	rw	16'h0	REP	Repetition counter value These bits allow the user to set-up the update rate of the compare registers (i.e. periodic transfers from preload to active registers) when preload registers are enable, as well as the update interrupt generation rate, if this interrupt is enable. Each time the REP_CNT related downcounter reaches zero, an update event is generated and it restarts counting from REP value. As REP_CNT is reloaded with REP value only at the repetition update event, any write to the RCRx register is not taken in account until the next repetition update event. It means in PWM mode (REP+1) corresponds to the number of PWM periods.
0x84			**CCR4**	Compare register for channel 4
[31:0]	rw	32'h0	CCR	Compare value CCR is the value to be loaded in the actual compare register (preload value).It is loaded permanently if the preload feature is not selected in the CR register (bit OCPE). Else the preload value is copied in the active compare register when an update event occurs. The active compare register contains the value to be compared to the counter and signaled on output.
0x88			**FIFO4**	FIFO for channel 4
[31:8]			RSVD	
[7:0]	w	8'h0	DATA	Entry of data FIFO in arbitary pulse mode. DMA or CPU will write data to this register to fill data FIFO.
0x8C			**CR5**	control register for channel 5
[31:6]			RSVD	
[5]	rw	1'h0	CCP	Compare output Polarity. 0: output active high 1: output active low
[4]	rw	1'h0	CCE	Compare output enable 0: Off - output is not active. No push-pull output. 1: On - output active.
[3]	rw	1'h0	OPM	One-pulse mode 0: Counter is not stopped at update event 1: Counter stops counting at the next update event (clearing the bit CEN)
[2]	rw	1'h0	URS	Update request source This bit is set and cleared by software to select the UEV event sources. 0: Any of the following events generate an update interrupt if enabled. These events can be: – Counter overflow – Setting the UG bit – Update generation through the slave mode controller 1: Only counter overflow generates an update interrupt if enabled.

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表 9-5: PWM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	rw	1'h0	UDIS	Update disable This bit is set and cleared by software to enable/disable UEV event generation. 0: UEV enabled. The Update (UEV) event is generated by one of the following events: – Counter overflow/underflow – Setting the UG bit – Update generation through the slave mode controller Buffered registers are then loaded with their preload values. 1: UEV disabled. The Update event is not generated, shadow registers keep their value (ARRx, PSCx, CCRx). However the counter and the prescaler are reinitialized if the UG bit is set or if a hardware reset is received from the slave mode controller.
[0]	rw	1'h0	CEN	Counter enable 0: Counter disabled 1: Counter enabled Note: Gated mode can work only if the CEN bit has been previously set by software. However trigger mode can set the CEN bit automatically by hardware. CEN is cleared automatically in one-pulse mode, when an update event occurs.
0x94			**CNT5**	Counter for channel 5
[31:16]			RSVD	
[15:0]	r	16'h0	CNT	Current counter value. Will be cleared if CEN=0.
0x98			**PSC5**	Prescaler for channel 5
[31:16]			RSVD	
[15:0]	rw	16'h0	PSC	Prescaler value The counter clock frequency is fpclk/(PSC+1). PSC contains the value to be loaded in the active prescaler register at each update event (including when the counter is cleared through UG bit of EGR register or through trigger controller when configured in "reset mode").
0x9C			**ARR5**	Auto-reload register for channel 5
[31:16]			RSVD	
[15:0]	rw	16'h0100	ARR	Auto-reload value ARR is the value to be loaded in the actual auto-reload register. ARR can be used to adjust brightness of breath light. Larger ARR leads to lower brightness.
0xA0			**RCR5**	Repetition counter register for channel 5
[31:8]			RSVD	
[7:0]	rw	8'h0	REP	Repetition counter value PWM will repeat (REP+1) times in each step of breath waveform.
0xA4			**INTV5**	Interval of breath wave for channel 5
[31:16]	rw	16'h0	PEAK	Peak duration of breath light waveform. PWM will repeat (PEAK+1) times for peak duration.
[15:0]	rw	16'h0	IDLE	Idle interval between two breath light waveform. PWM will repeat (PEAK+1) times for idle interval.

9.5 LPTIM

LPTIM1 与 LPTIM2 位于 HPSYS_AON，在 HPSYS 进入低功耗模式时 (除 hibernate 外) 能够保持工作，输入输出连接至 IO(PA) 与低功耗 IO(PA24~PA27)。

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9.5.1 简介

LPTIM (Low Power Timer) 基于一个 24 比特递增计数器，可实现计时、产生输出波形 (输出比较和 PWM) 和唤醒系统等功能。计数时钟可以为系统时钟，低功耗时钟，IO 输入信号或比较器输出，并可进行最多 128 倍的预分频以及最多 256 次的循环计数。根据计数结果可以产生 PWM 输出，并可产生中断，或产生唤醒信号将系统从低功耗模式唤醒。当用 IO 输入信号作为计数时钟时，支持不依赖于内部时钟进行计数并产生唤醒信号。

9.5.2 主要特性

- 24 位向上自动重装载计数器，最大计数 16777215(2^{24}-1)
- 计数时钟选择
  - 内部时钟，PCLK2 或低功耗时钟
  - 可选边沿的 IO 输入信号或比较器输出，可利用内部时钟进行防抖动，也可不依赖内部时钟独立计数
- 8 档预分频，计数时钟分频系数为 2 的 0~7 次方
- 1~256 循环次数
- 计数模式
  - 连续计数模式
  - 单笔计数模式，循环次数完成后计数结束
- 可配极性的输出模式
  - PWM 输出，可配脉宽，周期
  - 单次翻转输出
  - 单脉冲或指定个数脉冲输出
- 触发模式
  - 软件触发
  - IO 输入信号边沿触发，支持防抖动滤波
- 超时检测，每次外部触发时计数器复位
- 如下事件发生时产生中断或唤醒信号：
  - 更新
  - 计数器溢出
  - 输出比较
  - 外部触发

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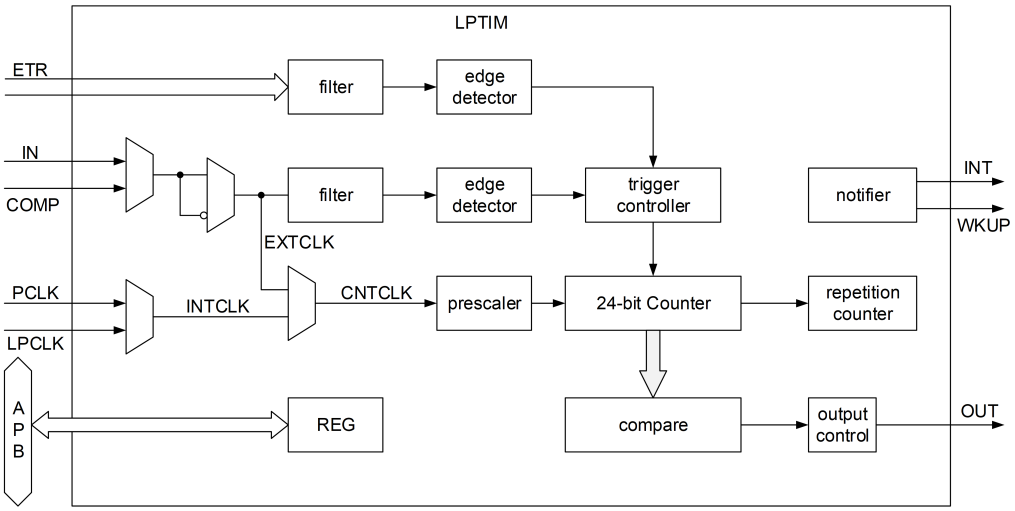


图 9-17: LPTIM 结构图

9.5.3 LPTIM 功能描述

9.5.3.1 计数器

LPTIM 的各项功能均基于一个 24 比特的计数器。计数器基于事件计数，包括时钟翻转、外部输入翻转、比较器结果翻转等。

计数事件经过预分频处理才会真正进入计数器。预分频的次数介于 1 到 128 之间 $(2^{CFGR\_PRESCPSC})$，即仅当发生了 $(2^{CFGR\_PRESCPSC})$ 次计数事件，计数器的值才真正改变一次。

计数器固定为递增计数模式，计数器从 0 计数到自动重载值 ARR，然后重新从 0 开始计数并产生计数器上溢事件。

计数值可以通过 CNT 读出。由于计数时钟与 APB 时钟异步，需要连续两次读取的数值相同才能认为是一次有效数据读取。

9.5.3.2 计数时钟

LPTIM 计数器的计数时钟 CNTCLK 可以在多个来源中选择。最常用的默认模式是选择内部低功耗时钟 LPCLK，此时 LPTIM 可以在芯片进入低功耗睡眠模式以后继续保持工作。当不处于低功耗睡眠模式时，LPTIM 也可以选择内部 PCLK 做时钟。LPTIM 还能够不依赖于内部时钟，直接用外部信号 IN 或者比较器输出信号 COMP 做时钟进行计数。时钟选择相关的寄存器包括 CFGR_EXTCKSEL/INTCKSEL/CKSEL。外部时钟的极性可以用 CFGR_CKPOL 选择。

当选择内部时钟时，还可以对外部信号 IN 或者比较器输出信号 COMP 翻转的事件进行计数，并能够进行预滤波和边沿选择处理。这种模式下应保证内部时钟的翻转频率至少为外部信号 IN 或者比较器输出信号 COMP 翻转频率的五倍。

9.5.3.3 更新事件 (UEV)

更新事件用于标志一个计数单元的结束。最基本的更新事件产生于每次计数器上溢时 (未开启重复计数时)。更新事件可以产生中断和唤醒信号，是定时器最基本的一项通知功能。

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9.5.3.4 重复计数

如果配置了重复计数器 (RCR>0)，每次计数器上溢时重复计数器会递减，并仅当重复计数器为 0 时才产生更新事件。

重复计数器的当前值可以通过 RCR 读出。由于计数时钟与 APB 时钟异步，需要连续两次读取的数值相同才能认为是一次有效数据读取。

9.5.3.5 计数器触发

计数器可配置为一级触发模式 (CFGR_TRIGEN=00) 或两级触发模式 (CFGR_TRIGEN!=00)。

一级触发模式为软件触发，包括单次触发和连续触发两种。触发前，需先将 CR_ENABLE 置 1 使能计数器。随后将 CR_SNGSTRT 置 1 启动单次触发，计数器即刻启动，并在更新事件后停止；或将 CR_CNTSTRT 置 1 启动连续触发，计数器即刻启动持续计数直到计数器关闭使能或复位。

两级触发模式在软件触发基础上增加硬件触发机制，仅当经过滤波的 ETR 可选边沿到来时才真正启动计数器。

9.5.3.6 超时监测

在两级触发模式下，如果将 CFGR_TIMOUT 置 1，则每次硬件触发时均会复位计数器并重新启动计数。该功能可用于监测两个连续触发信号之间的间隔，当间隔超出预期时产生比较或更新事件。

9.5.3.7 PWM 输出

LPTIM 可以产生周期、占空比可控的单路 PWM 输出至 OUT 端口。PWM 输出的周期由 ARR 决定，占空比由 CMP 决定。计数器值 CNT 与 CMP 进行比较，生成 PWM，极性通过 CFGR_WAVEPOL 配置。单次触发模式下，根据 RCR 的值可生成单个或多个脉冲。连续触发模式下可生成持续的 PWM。如果 CFGR_WAVE 为 1，可以生成单次置 1 波形。

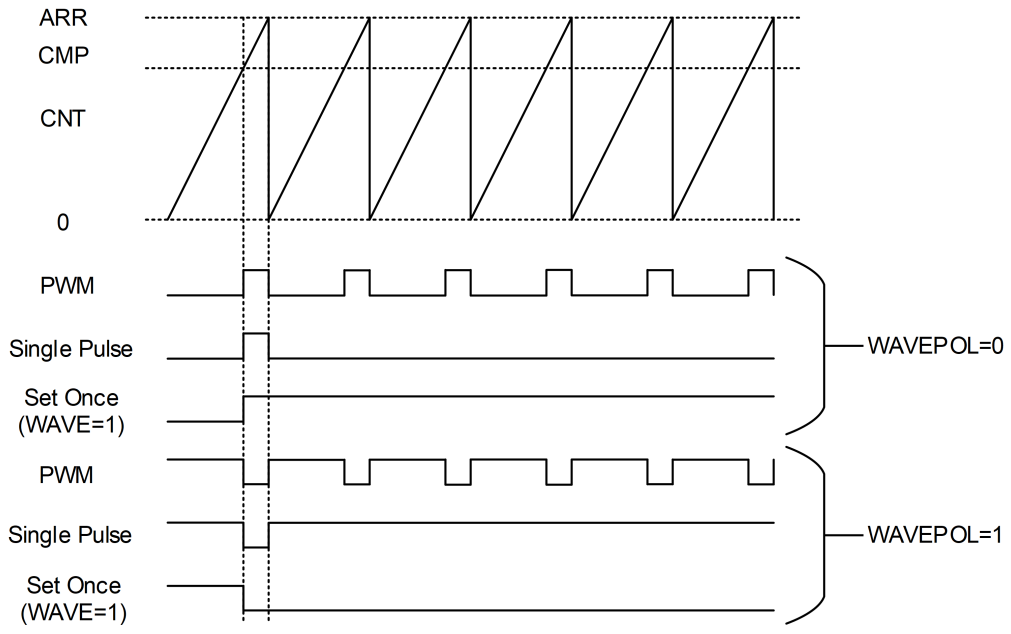


图 9-18: PWM 输出

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9.5.3.8 通知机制

LPTIM 能够产生中断和唤醒等通知。中断仅在系统处于非低功耗睡眠状态时产生。唤醒信号无论系统是否处于低功耗睡眠状态均可产生，并能够将系统唤醒。能够触发通知的事件主要包括上溢事件、更新事件、触发事件、比较器匹配等。IER 寄存器可以控制各种事件是否产生中断和唤醒。各事件状态可在 ISR 寄存器中查询。

9.5.4 LPTIM 寄存器

表 9-6: LPTIM 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**ISR**	LPTIM interrupt and status register
[31:11]			RSVD	
[10]	r	1'h0	OCWKUP	Indicates output compare wakeup occurred The OCWKUP bit is set by hardware when LPTIM_CNT register value reached the LPTIM_CMP register's value. To clear OCWKUP, first write 0 to the OCWE bit in the LPTIM_IER register to disable, then write 1 to the WKUPCLR bit in the LPTIM_ICR register.
[9]	r	1'h0	OFWKUP	Indicates overflow wakeup occurred OFWKUP is set by hardware when LPTIM_CNT register's value reached the LPTIM_ARR register's value and count from zero again. To clear OFWKUP, first write 0 to the OFWE bit in the LPTIM_IER register to disable, then write 1 to the WKUPCLR bit in the LPTIM_ICR register.
[8]	r	1'h0	UEWKUP	Indicates update event wakeup occurred UEWKUP is set by hardware when an update event was generated (overflow occurred while repetition counter reached zero). To clear UEWKUP, first write 0 to the UEWE bit in the LPTIM_IER register to disable, then write 1 to the WKUPCLR bit in the LPTIM_ICR register.
[7:4]			RSVD	
[3]	r	1'h0	ET	External trigger edge event ET is set by hardware to inform application that a valid edge on the selected external trigger input has occurred. If the trigger is ignored because the timer has already started, then this flag is not set. ET flag can be cleared by writing 1 to the ETCLR bit in the LPTIM_ICR register.
[2]	r	1'h0	OC	Output compare match The OC bit is set by hardware to inform application that LPTIM_CNT register value reached the LPTIM_CMP register's value. OC flag can be cleared by writing 1 to the OCCLR bit in the LPTIM_ICR register.
[1]	r	1'h0	OF	Overflow occurred OF is set by hardware to inform application that LPTIM_CNT register's value reached the LPTIM_ARR register's value and count from zero again. OF flag can be cleared by writing 1 to the OFCLR bit in the LPTIM_ICR register.
[0]	r	1'h0	UE	LPTIM update event occurred UE is set by hardware to inform application that an update event was generated when overflow occurred while repetition counter reached zero. UE flag can be cleared by writing 1 to the UECLR bit in the LPTIM_ICR register.
0x04			**ICR**	LPTIM interrupt and status clear register
[31:9]			RSVD	
[8]	w	1'h0	WKUPCLR	wakeup status clear flag Writing 1 to this bit clears all wakeup status flags in the LPTIM_ISR register.
[7:4]			RSVD	

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表 9-6: LPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[3]	w	1'h0	ETCLR	External trigger valid edge clear flag Writing 1 to this bit clears the ET flag in the LPTIM_ISR register
[2]	w	1'h0	OCCLR	Output compare clear flag Writing 1 to this bit clears the OC flag in the LPTIM_ISR register
[1]	w	1'h0	OFCLR	Overflow clear flag Writing 1 to this bit clears the OF flag in the LPTIM_ISR register
[0]	w	1'h0	UECLR	Update event clear flag Writing 1 to this bit clear the UE flag in the LPTIM_ISR register.
0x08			**IER**	LPTIM interrupt and wakeup enable register
[31:11]			RSVD	
[10]	rw	1'h0	OCWE	Output compare Wakeup Enable 0: Output compare wakeup disabled 1: Output compare wakeup enabled
[9]	rw	1'h0	OFWE	Overflow Wakeup Enable 0: Overflow Wakeup disabled 1: Overflow Wakeup enabled
[8]	rw	1'h0	UEWE	Update event Wakeup enable 0: Update event Wakeup disabled 1: Update event Wakeup enabled
[7:4]			RSVD	
[3]	rw	1'h0	ETIE	External trigger valid edge Interrupt Enable 0: External trigger interrupt disabled 1: External trigger interrupt enabled
[2]	rw	1'h0	OCIE	Output compare Interrupt Enable 0: Output compare interrupt disabled 1: Output compare interrupt enabled
[1]	rw	1'h0	OFIE	Overflow Interrupt Enable 0: Overflow interrupt disabled 1: Overflow interrupt enabled
[0]	rw	1'h0	UEIE	Update event interrupt enable 0: Update event interrupt disabled 1: Update event interrupt enabled
0x0C			**CFGR**	LPTIM configuration register
[31:24]			RSVD	
[23]	rw	1'h0	COUNTMODE	counter mode in internal clock source mode (CKSEL=0). If CKSEL=1, this bit has no effect. 0: the counter is incremented following each internal clock pulse 1: the counter is incremented following each valid pulse on the external clock
[22]			RSVD	
[21]	rw	1'h0	WAVPOL	Waveform shape polarity The WAVEPOL bit controls the output polarity 0: The LPTIM output reflects the compare results between LPTIM_ARR and LPTIM_CMP registers 1: The LPTIM output reflects the inverse of the compare results between LPTIM_ARR and LPTIM_CMP registers
[20]	rw	1'h0	WAVE	Waveform shape The WAVE bit controls the output shape 0: Deactivate Set-once mode 1: Activate the Set-once mode

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表 9-6: LPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[19]	rw	1'h0	TIMOUT	Timeout enable The TIMOUT bit controls the Timeout feature 0: A trigger event arriving when the timer is already started will be ignored 1: A trigger event arriving when the timer is already started will reset and restart the LPTIM counter and the repetition counter
[18:17]	rw	2'h0	TRIGEN	Trigger enable and polarity The TRIGEN bits controls whether the LPTIM counter is started by an external trigger or not. If the external trigger option is selected, three configurations are possible for the trigger active edge: 00: software trigger (counting start is initiated by software) 01: rising edge is the active edge 10: falling edge is the active edge 11: both edges are active edges
[16]			RSVD	
[15:13]	rw	3'h0	TRIGSEL	Trigger selector The TRIGSEL bits select the trigger source that will serve as a trigger event for the LPTIM among the below 8 available sources: 000: lptim_ext0 001: lptim_ext1 010: lptim_ext2 011: lptim_ext3 100: lptim_ext4 101: lptim_ext5 110: lptim_ext6 111: lptim_ext7
[12]			RSVD	
[11:9]	rw	3'h0	PRESC	Clock prescaler The PRESC bits configure the prescaler division factor. It can be one among the following division factors: 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
[8]	rw	1'h0	EXTCKSEL	External clock source selector 0: external clock source is from lptim_in 1: external clock source is from LPCOMP (if LPCOMP integrated)

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表 9-6: LPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7:6]	rw	2'h0	TRGFLT	Configurable digital filter for trigger The TRGFLT value sets the number of consecutive equal samples that should be detected when a level change occurs on an internal trigger before it is considered as a valid level transition. An internal clock source must be present to use this feature 00: any trigger active level change is considered as a valid trigger 01: trigger active level change must be stable for at least 2 clock periods before it is considered as valid trigger. 10: trigger active level change must be stable for at least 4 clock periods before it is considered as valid trigger. 11: trigger active level change must be stable for at least 8 clock periods before it is considered as valid trigger.
[5]	rw	1'h0	INTCKSEL	Internal clock source selector 0: internal clock source is clk_lp 1: internal clock source is pclk2
[4:3]	rw	2'h0	CKFLT	Configurable digital filter for external clock The CKFLT value sets the number of consecutive equal samples that should be detected when a level change occurs on an external clock signal before it is considered as a valid level transition. An internal clock source must be present to use this feature 00: any external clock signal level change is considered as a valid transition 01: external clock signal level change must be stable for at least 2 clock periods before it is considered as valid transition. 10: external clock signal level change must be stable for at least 4 clock periods before it is considered as valid transition. 11: external clock signal level change must be stable for at least 8 clock periods before it is considered as valid transition.
[2:1]	rw	2'h0	CKPOL	Clock Polarity If LPTIM is clocked by an external clock source, CKPOL bits is used to configure the active edge or edges used by the counter: 00: the rising edge is the active edge used for counting 01: the falling edge is the active edge used for counting 10: both edges are active edges. When both external clock signal edges are considered active ones, the LPTIM must also be clocked by an internal clock source with a frequency equal to at least four time the external clock frequency. 11: not allowed
[0]	rw	1'h0	CKSEL	Clock selector The CKSEL bit selects which clock source the LPTIM will use: 0: LPTIM is clocked by internal clock source, according to INTCKSEL 1: LPTIM is clocked by external clock source, according to EXTCKSEL
0x10			**CR**	LPTIM control register
[31:4]			RSVD	
[3]	rw	1'h0	COUNTRST	Counter reset This bit is set by software and cleared by hardware. When set to 1 this bit will trigger a synchronous reset of the CNT register. Due to the synchronous nature of this reset, it only takes place after a synchronization delay. COUNTRST must never be set to 1 by software before it is already cleared to 0 by hardware. Software should consequently check that COUNTRST bit is already cleared to 0 before attempting to set it to 1.

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表 9-6: LPTIM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[2]	w	1'h0	CNTSTRT	Timer start in Continuous mode This bit is set by software and cleared by hardware. In case of software start (TRIGEN[1:0] = 00), setting this bit starts the LPTIM in Continuous mode. If the software start is disabled (TRIGEN[1:0] different than 00), setting this bit starts the timer in Continuous mode as soon as an external trigger is detected. If this bit is set when a single pulse mode counting is ongoing, then the timer will not stop at the next match between ARR and CNT registers and the LPTIM counter keeps counting in Continuous mode.
[1]	w	1'h0	SNGSTRT	LPTIM start in Single mode This bit is set by software and cleared by hardware. In case of software start (TRIGEN[1:0] = 00), setting this bit starts the LPTIM in single pulse mode. If the software start is disabled (TRIGEN[1:0] different than 00), setting this bit starts the LPTIM in single pulse mode as soon as an external trigger is detected. If this bit is set when the LPTIM is in continuous counting mode, then the LPTIM will stop at the following match between ARR and CNT registers. If this bit is set simultaneously with CNTSTRT, then LPTIM will be in continuous counting mode.
[0]	rw	1'h0	ENABLE	LPTIM enable The ENABLE bit is set and cleared by software. 0:LPTIM is disabled 1:LPTIM is enabled
0x14			**CMP**	LPTIM compare register
[31:24]			RSVD	
[23:0]	rw	24'h0	CMP	Compare value CMP is the compare value used by the LPTIM.
0x18			**ARR**	LPTIM autoreload register
[31:24]			RSVD	
[23:0]	rw	24'h0	ARR	Auto reload value ARR is the autoreload value for the LPTIM. This value must be strictly greater than the CMP[15:0] value.
0x1C			**CNT**	LPTIM counter register
[31:24]			RSVD	
[23:0]	r	24'h0	CNT	Counter value When the LPTIM is running with an asynchronous clock, reading the CNT register may return unreliable values. So in this case it is necessary to perform two consecutive read accesses and verify that the two returned values are identical.
0x20			**RCR**	LPTIM repetition register
[31:8]			RSVD	
[7:0]	rw	8'h0	REP	Repetition register value REP is the repetition value for the LPTIM. Read REP will return left repetition times. It should be noted that for a reliable REP register read access, two consecutive read accesses must be performed and compared. A read access can be considered reliable when the values of the two consecutive read accesses are equal.

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9.6 WDT

芯片共有 3 个 WDT，其中 WDT1 位于 HPSYS，当 HPSYS 进入 deepsleep，standby 或 hibernate 模式后停止工作；WDT2 位于 LPSYS，当 LPSYS 进入 deepsleep，standby 或 hibernate 模式后停止工作；IWDT 位于 AON，当芯片进入低功耗模式以后仍能保持工作。具体每个 WDT 的复位作用域可参考时钟与复位章节。

9.6.1 简介

看门狗计时器作为一种计数器主要是用于在到达设定好的时间之后重置系统，以防止软件挂死。

看门狗计时器基本功能：

- 支持两种工作模式：
  - mode0
    - wdt 不会产生中断，在到达设定的时间之后会直接重置系统。
    - 最高支持 24bit 的计数器
  - mode1
    - 分为两段计数，在到达第一段设定的时间之后，会产生中断，在到达第二段设定的时间之后，再重置系统。
    - 每个时间段最高支持 24bit 的计数器
- 支持写保护，以防止软件对 wdt 进行误操作

9.6.2 WDT 的工作方式

wdt 根据需求有两种 reset 产生模式：

模式 1：只计数一轮，计数结束直接产生 reset 的信号。

模式 2：计数两轮，第一轮计数结束产生中断，第二轮计数结束产生 reset 信号。

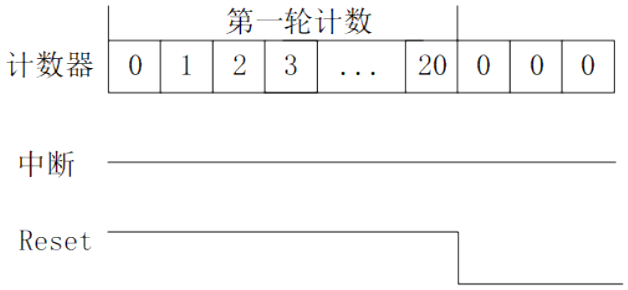


图 9-19: 模式 1 的中断以及 reset 信号产生与计数器的关系（假定超时值为 20，reset 低有效）

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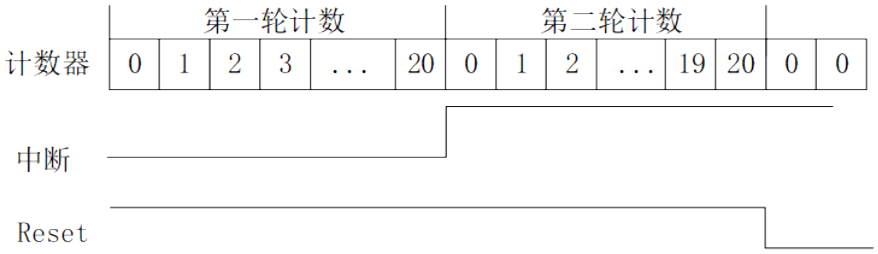


图 9-20: 模式 2 的中断以及 reset 信号产生与计数器的关系（假定超时值为 20，reset 低有效）

两种模式下的“喂狗”行为：

在模式 1 下，第一轮计数结束之前“喂狗”，则计数器从零开始重新计数；

在模式 2 下，第一轮计数结束之前“喂狗”，则计数器从零开始重新计数；如果第一轮计数器结束之前没有“喂狗”行为，则 wdt 进入第二轮计数，此时通过清除中断，或者“喂狗”的行为都可以让 wdt 重新进入第一轮开始计数。

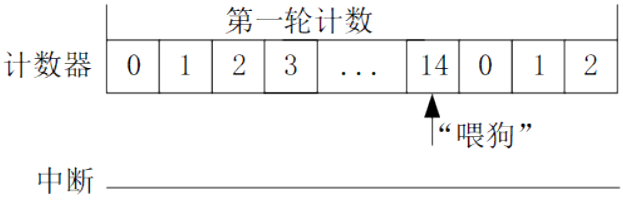


图 9-21: 模式 1“喂狗”行为对计数器的影响（假定超时值为 20）

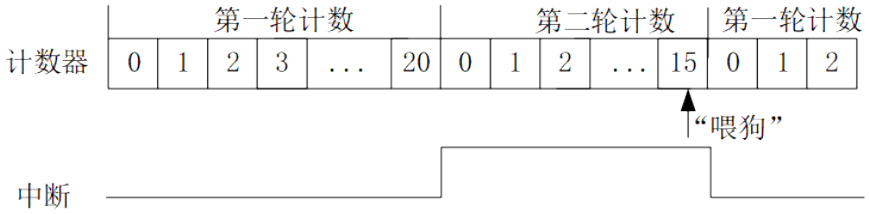


图 9-22: 模式 2 在第二轮计数时“喂狗“操作对计数器的影响，第一轮计数时的影响和模式 1 相同（假定超时值为 20）

两种模式下停止 wdt 的方式：

在模式 1 下，在计数结束之前配置寄存器 0x0C(counter_control)=0x34，wdt 则会停止；

在模式 2 下,在第一轮计数结束之前配置寄存器 0x0C(counter_control)=0x34,wdt 则会停止;如果在第二轮计数阶段则需要清除中断或者进行“喂狗”的操作让 wdt 回到第一轮计数才能进行配置寄存器 0x0C(counter_control)=0x34，让 wdt 停止。

清除中断的方法：

在模式 2 下，wdt 在第一轮计数完成之后会产生中断 0x14 WDT_SR 中 int_assert 为 1，此时可以通过配置 0x10 的 WDT_IDR 的 int_clr 来清除或者通过配置 0xc WDT_CCR 中 counter_control 为 0x76 即喂狗来清除。

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9.6.2.1 WDT 寄存器配置流程

1. 根据需要选择 wdt 的工作模式。配置 0x08 中 response_mode 寄存器，配置 0x0 选择模式 1，配置 0x1 选择模式 2
2. 根据 wdt 触发 reset 时间配置 0x00 中 count_value_0 寄存器（两种模式下第一轮计数的超时值）以及 0x04 中的 count_value_1（模式 2 下第二轮计数器的超时值）
3. 根据需求配置 0x08 中 reset length 的长度
4. 配置 0x0c 中 counter_control 寄存器（=0x76）触发 wdt 开始工作

   1~3 的顺序没有要求，只要在 4 之前完成即可。

9.6.2.2 注意事项

1. wdt 提供了 write protect 写保护功能以防止 wdt 中的配置被意外改写，使用方法如下：

   配置 0x18 中 wrpt 寄存器为 0x58ab99fc，当 0x18 寄存器中 wrpt_st 为 1 说明写保护使能，此状态下 wdt 中的所有寄存器无法被改写但不影响读操作，如要取消写保护则配置 0x18 中 wrpt 寄存器为 0x51ff8621。
2. wdt 中 0x1c 的 sync_fg 寄存器为 1 表示 start，stop，irq clear，reset flag clear 的操作已经从 pclk 同步到 wdt clk 中即已经生效。
3. rst_fg 为 1 表示此 wdt 发生了 reset，此寄存器只有 iwdt 才有效。
4. 如果 0xc 中的 counter_control 写不进去，先 check 对应 sys rcc 里面的 wdt 时钟 enable 寄存器有没有配置为 1。

9.6.3 WDT 寄存器

表 9-7: WDT 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**WDT_CVR0**	WatchDog Counter Value 0
[31:24]			RSVD	
[23:0]	rw	24'hffffff	count_value_0	Count Value for 1st TimeOut
0x04			**WDT_CVR1**	WatchDog Counter Value 1
[31:24]			RSVD	
[23:0]	rw	24'hffffff	count_value_1	Count Value for 2nd TimeOut
0x08			**WDT_CR**	WatchDog Control Register
[31:5]			RSVD	
[4]	rw	1'b1	response_mode	0:reset only, 1:interrupt and reset
[3]			RSVD	
[2:0]	rw	3'b000	reset_length	reset pulse length in number of wdt clock cycles
0x0C			**WDT_CCR**	WatchDog Counter Control Register
[31:8]			RSVD	
[7:0]	rw	8'h0	counter_control	SinglePulse /Write 8'h76 to restart, write8'h34 to stop, else do nothing
0x10			**WDT_ICR**	WatchDog Interrupt Clear Register
[31:1]			RSVD	
[0]	w1c	1'b0	int_clr	SinglePulse /A pulse to clear interrupt
0x14			**WDT_SR**	WatchDog Status Register
[31:2]			RSVD	
[1]	r	1'b0	wdt_active	Watchdog runs when 1, else 0
[0]	r	1'b0	int_assert	Interrupt assert when 1
0x18			**WDT_WP**	WatchDog Write Protect Register

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表 9-7: WDT 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31]	r	1'b0	wrpt_st	1 indicates write protect is active
[30:0]	w	31'h0	wrpt	write 0x58ab99fc generate write_protect, write 0x51ff8621 to release
0x1C			**WDT_FG**	WatchDog Flag Register
[31:4]			RSVD	
[3]	r	1'b0	sync_fg	1 indicates one transition from system clk to wdt clk has complicated
[2]	w1c	1'b0	sync_fg_clr	SinglePulse/A pulse to clear sync flag
[1]	r	1'b0	rst_fg	1 indicates wdt has already reset system
[0]	w1c	1'b0	rst_fg_clr	SinglePulse/A pulse to clear reset flag

9.7 RTC

9.7.1 RTC 寄存器

RTC 的基地址是 0x500CB000。

表 9-8: RTC 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**TR**	Time Register
[31]	rw	1'h0	PM	AM/PM notation 0: AM 1: PM
[30:29]	rw	2'h0	HT	Hour tens in BCD format
[28:25]	rw	4'h0	HU	Hour units in BCD format
[24:22]	rw	3'h0	MNT	Minute tens in BCD format
[21:18]	rw	4'h0	MNU	Minute units in BCD format
[17:15]	rw	3'h0	ST	Second tens in BCD format
[14:11]	rw	4'h0	SU	Second units in BCD format
[10]			RSVD	
[9:0]	r	10'h0	SS	Sub-second counter
0x04			**DR**	Date Register
[31]	r	1'h0	ERR	reserved for debug
[30:25]			RSVD	
[24]	rw	1'h0	CB	century bit, 0 - 2000s, 1 - 1900s/2100s
[23:20]	rw	4'h0	YT	Year tens in BCD format
[19:16]	rw	4'h0	YU	Year units in BCD format
[15:13]	rw	3'h1	WD	Week day units 000: forbidden 001: Monday ... 111: Sunday
[12]	rw	1'h0	MT	Month tens in BCD format
[11:8]	rw	4'h1	MU	Month units in BCD format
[7:6]			RSVD	
[5:4]	rw	2'h0	DT	Date tens in BCD format
[3:0]	rw	4'h1	DU	Date units in BCD format
0x08			**CR**	Control Register
[31:22]			RSVD	

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表 9-8: RTC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[21]	rw	1'h0	COE	
[20:19]	rw	2'h0	OSEL	
[18]	rw	1'h0	POL	
[17]	rw	1'h0	COSEL	
[16]	rw	1'h0	BKP	
[15]	rw	1'h0	SUB1H	
[14]	rw	1'h0	ADD1H	
[13]	rw	1'h0	TSIE	
[12]	rw	1'h0	WUTIE	
[11]	rw	1'h0	ALRMIE	
[10]	rw	1'h0	TSE	
[9]	rw	1'h0	WUTE	
[8]	rw	1'h0	ALRME	
[7]			RSVD	
[6]	rw	1'h0	FMT	
[5]	rw	1'h0	BYPSHAD	
[4]	rw	1'h0	REFCKON	
[3]	rw	1'h0	TSEDGE	
[2]			RSVD	
[1]	rw	1'h0	WUCKSEL	
[0]			RSVD	
0x0C			**ISR**	Initialization and Status Register
[31:11]			RSVD	
[10]	rw	1'h0	INIT	
[9]	r	1'h0	INITF	
[8]	r	1'h0	INITS	
[7]	rw0c	1'h0	RSF	
[6]	r	1'h0	SHPF	
[5]	r	1'h0	TSOVF	
[4]	rw0c	1'h0	TSF	
[3]	rw0c	1'h0	WUTF	
[2]	r	1'h1	WUTWF	
[1]	rw0c	1'h0	ALRMF	
[0]	r	1'h1	ALRMWF	
0x10			**PSCLR**	Prescaler Register
[31:24]	rw	8'h80	DIVA_INT	
[23:10]	rw	14'h0	DIVA_FRAC	
[9:0]	rw	10'h100	DIVB	
0x14			**WUTR**	Wakeup Timer Register
[31:18]			RSVD	
[17:0]	rw	18'h3ffff	WUT	
0x18			**ALRMTR**	Alarm Time Register
[31]	rw	1'h0	PM	
[30:29]	rw	2'h0	HT	
[28:25]	rw	4'h0	HU	
[24:22]	rw	3'h0	MNT	
[21:18]	rw	4'h0	MNU	
[17:15]	rw	3'h0	ST	

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表 9-8: RTC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[14:11]	rw	4'h0	SU	
[10]			RSVD	
[9:0]	rw	10'h0	SS	
0x1C			**ALRMDR**	Alarm Date Register
[31:30]			RSVD	
[29]	rw	1'h0	MSKWD	
[28]	rw	1'h0	MSKM	
[27]	rw	1'h0	MSKD	
[26]	rw	1'h0	MSKH	
[25]	rw	1'h0	MSKMN	
[24]	rw	1'h0	MSKS	
[23:20]	rw	4'h0	MSKSS	
[19:16]			RSVD	
[15:13]	rw	3'h1	WD	
[12]	rw	1'h0	MT	
[11:8]	rw	4'h1	MU	
[7:6]			RSVD	
[5:4]	rw	2'h0	DT	
[3:0]	rw	4'h1	DU	
0x20			**SHIFTR**	Shift Control Register
[31]	rw	1'b0	ADD1S	
[30:10]			RSVD	
[9:0]	rw	10'h0	SUBFS	
0x24			**TSTR**	Timestamp Time Register
[31]	r	1'h0	PM	
[30:29]	r	2'h0	HT	
[28:25]	r	4'h0	HU	
[24:22]	r	3'h0	MNT	
[21:18]	r	4'h0	MNU	
[17:15]	r	3'h0	ST	
[14:11]	r	4'h0	SU	
[10]			RSVD	
[9:0]	r	10'h0	SS	
0x28			**TSDR**	Timestamp Date Register
[31:16]			RSVD	
[15:13]	r	3'h1	WD	
[12]	r	1'h0	MT	
[11:8]	r	4'h1	MU	
[7:6]			RSVD	
[5:4]	r	2'h0	DT	
[3:0]	r	4'h1	DU	
0x2C			**OR**	Option Register
[31:2]			RSVD	
[1]	rw	1'h0	RTC_OUT_RMP	
[0]	rw	1'h0	RTC_ALARM_TYPE	
0x30			**BKP0R**	Backup 0 Register
[31:0]	rw	32'h0	BKP	
0x34			**BKP1R**	Backup 1 Register

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表 9-8: RTC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	BKP	
0x38			**BKP2R**	Backup 2 Register
[31:0]	rw	32'h0	BKP	
0x3C			**BKP3R**	Backup 3 Register
[31:0]	rw	32'h0	BKP	
0x40			**BKP4R**	Backup 4 Register
[31:0]	rw	32'h0	BKP	
0x44			**BKP5R**	Backup 5 Register
[31:0]	rw	32'h0	BKP	
0x48			**BKP6R**	Backup 6 Register
[31:0]	rw	32'h0	BKP	
0x4C			**BKP7R**	Backup 7 Register
[31:0]	rw	32'h0	BKP	
0x50			**BKP8R**	Backup 8 Register
[31:0]	rw	32'h0	BKP	
0x54			**BKP9R**	Backup 9 Register
[31:0]	rw	32'h0	BKP	

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10 图像和视频

10.1 ePicasso™ 高性能 2.5D 图形引擎

在 2.5D 图像处理中，有许多常见的图像运算会耗费大量的 CPU 计算资源。ePicasso™ 则是专为 2.5D 图像运算设计的加速引擎，能够对 2.5D 图像运算中常见图层叠加、缩放、旋转等功能提供指数级的速度提升。除此以外，ePicasso™ 能够兼容各种常见的 RGB 图像格式，简化了系统中不同格式的图像格式转换。

10.1.1 图层叠加

ePicasso™ 最多支持两个前景图层，一个专用的掩膜图层，和一个单色背景图层叠加，输入和输出格式包括常用 RGB565、RGB888、ARGB8565、ARGB8888、L8、A8、A4、A2、YUV。每个前景图层有独立的叠加模式和叠加区域，掩膜图层主要是提取图像中特定的形状。除此以外，每个图层还提供了单独的 filter 配置选项，可以使图层滤除某一特定的颜色，该功能可用于简单的图像捕获。

10.1.2 图形缩放

ePicasso™ 有一个图层称为功能图层，除了支持叠加的功能外，这个功能图层还能够实现图形的缩放。缩放最大比例可以到达 1024 倍，精度则可以达到 1/65536。在 X 和 Y 方向上，缩放的比例可以分别配置，以此适应各种不同的需求。

10.1.3 图形旋转

ePicasso™ 的功能图层除了可以支持缩放的功能以外，还能够支持图像的高精度旋转。用户可以自定义旋转角的 sin/cos 值，来满足任意角度的旋转需求。旋转和缩放的功能可以同时启用，一次性完成图像的两种操作，提高了图像处理的性能。

10.2 LCDC

10.2.1 简介

LCDC 全称 LCD Controller，其主要功能是从内存空间读取图像数据，然后根据不同屏幕接口，将数据发送至对应的屏幕。LCDC 支持非常丰富的屏幕接口，包括：

- DBI/8080 接口：用于中低分辨率，带 GRAM 的显示屏
- SPI/DSPI/QSPI 接口：用于带 GRAM 的 IOT 小尺寸中低分辨率屏幕
- JDI Parallel 接口：用于 JDI 厂商专用反射型显示屏

除了丰富的接口，LCDC 对图像数据的格式支持也比较丰富，可以支持 RGB565，RGB888 以及 ARGB8888 等格式。在最基础的功能基础上，LCDC 也能够支持简单的图层混叠，可以进行最基础的图像处理加速。

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10.2.2 架构介绍

如下图所示是 LCDC 的基本架构框图：

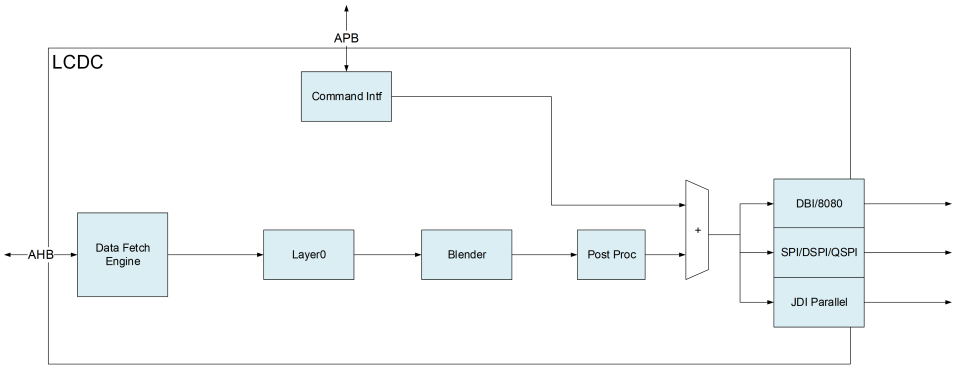


图 10-1: LCDC 架构图

图中有两条主要的数据通路。

1. 配置通路：上层通过 APB 总线发送屏幕配置指令，LCDC 接收到指令后，将对应的数据通过 Command Intf 模块发送到对应的屏幕接口上。该通路速率较低，主要用于屏幕初始化配置，以及基础功能验证。
2. 图像传输通路：LCDC 的 Data Fetch Engine 通过 AHB 总线，从内存空间读取图像数据，按配置发送到 Layer0。当 layer0 数据准备完成后，Blender 将图像数据与背景色混叠后送到对应的屏幕接口。该通路是 LCDC 向屏幕发送图像数据的主要通路。还有一点需要注意，Layer0 不使能时，Blender 可以配置成向屏幕发送单色数据。

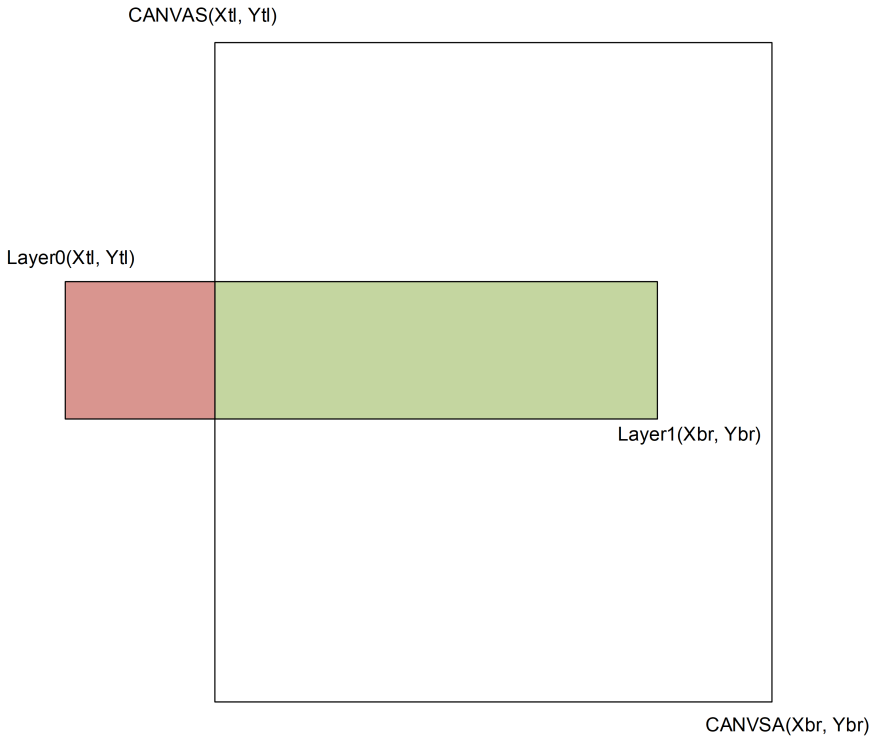
10.2.3 配置流程

LCDC 的配置主要分为两部分，第一部分是图层配置，针对的是两个 Layer 以及 Blender 的配置，第二部分是接口配置，针对的是不同接口对应的参数配置。

10.2.3.1 图层配置

图层配置包括 Layer0 的配置和 Blender 的配置，用户可以配置 Layer0_CONFIG 寄存器，对 Layer0 进行使能，并配置其色彩格式和混叠系数。当图层数据被送入 Blender 后，Blender 会根据用户配置的图层坐标和画布坐标进行混叠操作，每一个图层有自己独立的矩形区域，画布也有其自己的矩形区域，Blender 只对重叠部分的图像进行计算。具体可以参考下图：

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图中 CANVAS，Layer0，Layer1 各自有两组坐标代表各自的矩形区域，(Xtl, Ytl) 表示矩形左上角坐标，(Xbr, Ybr) 表示矩形右下角坐标。可以看到，Layer0 由两部分组成，红色部分在 CANVAS 外，所以不会参与计算，绿色区域与 CANVAS 重叠，所以会与 CANVAS 进行混叠计算。剩下白色的 CANVAS 区域因为没有与图层重叠，所以会直接输出 CANVAS 的背景色。

大部分场景下，LCDC 如果仅将图像帧缓存 (FrameBuffer) 输出到屏幕，那么只需要将图层的坐标与 CANVAS 坐标配置成一致即可。

10.2.3.2 接口配置

因为不同接口传输协议差别很大，所以对应的配置参数也不尽相同，以下根据不同接口列出了不同的配置参数。

DBI/8080 接口:

DBI/8080 接口用于驱动带有 GRAM 的屏幕，根据 MIPI 协议，DBI 并行接口本身还分为 TypeA 和 TypeB 两类，两者信号上略有不同，但逻辑上可以互相转换。在选择 LCDC 接口时也可以选择对应的 TypeA 和 TypeB。

DBI 接口的主要参数配置参考下表：

参数名	描述	配置
PWH	WRX/RDX 信号 inactive 状态周期数	周期对应时钟为系统时钟
PWL	WRX/RDX 信号 active 状态周期数	周期对应时钟为系统时钟
TAH	WRX/RDX 信号 inactive 后到 CSX 信号 inactive 延迟周期数	周期对应时钟为系统时钟
TAS	CSX 信号 active 后到 WRX/RDX 信号 active 延迟周期数	周期对应时钟为系统时钟

以上参数是 DBI 接口配置的主要参数，其中 PWH 和 PWL 决定了 DBI 接口的速率，其两者之和为单笔数据传输

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的周期数。

另一点需要注意，DBI 接口所有信号默认为低有效，如果需要调整有效相位，可以通过配置对应信号的 POL 寄存器，实现相位的反转。

除了图像传输通路，DBI 接口也支持配置通路。在设置完成 DBI 接口后，用户可以先将要写的值配置到 LCD_WR 寄存器，通过 WR_TRIG 和 RD_TRIG 寄存器触发读写操作，在通过 LCD_RD 寄存器获得读取的值。

SPI/DSPI/QSPI 接口:

SPI，DSPI 和 QSPI 都属于 SPI 类型的屏幕接口，区别在于数据线的数量。SPI 通常只有单根的数据线，DSPI 有两根，QSPI 有四根。除了数据线数量区别，SPI 接口还会基于 D/C(Data/Command 选择) 信号传输方式分为 3-wire SPI 和 4-wire SPI。3-wire SPI 的 D/C 作为一个数据 bit，通过 SDO 进行传输，4-wire SPI 的 D/C 则有一根单独的线来标识，所以相对来说 3-wire SPI 比 4-wire SPI 有效带宽略微低一些。

SPI 接口的主要参数配置参考下表：

参数名	描述	配置
CLK_DIV	SPI 时钟分频比	源时钟为系统时钟
LINE	SPI 模式	不同模式包含 3-wire/4-wire 以及对应的单数据线，双数据线和死数据线模式
SPI_CS_AUTO_DIS	SPI CS 自动停止	在数据传输阶段，如果由于总线繁忙，LCDC 没有即使获取数据送往屏幕，则会自动控制 SPI 接口的 CS 信号，使其处于非使能状态
SPI_CLK_AUTO_DIS	SPI 时钟自动停止	在数据传输阶段，如果由于总线繁忙，LCDC 没有即使获取数据送往屏幕，则会自动停止 SPI 接口的时钟信号

除了以上这些主要参数，其他还有一些参数主要用于 SPI 接口的读操作，以及 SPI 信号的相位等，具体可以参考寄存器表内的描述。

与 DBI 接口一样，SPI 接口也支持配置通路。在选择了 SPI 接口后，与 DBI 一样，用户可以通过 WR_TRIG 和 RD_TRIG 寄存器触发读写操作。对于 SPI，用户还需要配置 WR_LEN 和 RD_LEN，这两个寄存器决定了 SPI 接口的配置通路单次读写数据的字节数。0 表示 1 个字节，最高 4 个字节。

JDI Parallel 接口:

JDI Parallel 接口是 JDI 的反射屏专用的接口，JDI Parallel 作为并行接口，可以支持分辨率更高的屏幕，色彩也会更丰富一些。其配置参数也较多，具体需要参照 JDI Parallel 接口协议，对相应参数进行配置。配置参数如下：

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参数名	描述	配置
MAX_LINE	最大行数	\
MAX_COL	最大列数	\
ST_LINE	起始行数	第一行有效数据行数
END_LINE	结束行数	最后一行有效数据行数
ST_COL	起始列数	第一列有效数据列数
END_COL	结束列数	最后一列有效数据列数
HCK_WIDTH	HCK 信号宽度	基于系统时钟周期数
HST_WIDTH	HST 信号宽度	基于系统时钟周期数
VCK_WIDTH	VCK 信号宽度	基于系统时钟周期数
VST_WIDTH	VST 信号宽度	基于系统时钟周期数
VCK_DLY	VST 到 VCK 信号的延迟	基于系统时钟周期数
HST_DLY	VCK 到 HST 信号的延迟	基于系统时钟周期数
HCK_DLY	HST 到 HCK 信号的延迟	基于系统时钟周期数
ENB_ST_COL	ENB 信号起始列数	ENB 信号有效的第一列列数
ENB_END_COL	ENB 信号结束列数	ENB 信号有效的最后一列列数
ENB_ST_LINE	ENB 信号起始行数	ENB 信号有效的第一行行数
ENB_END_LINE	ENB 信号结束列数	ENB 信号有效的最后一行行数
DP_MODE	DP 模式	支持大小双像素模式

JDI Parallel 接口配置参数较多，需要结合 JDI Parallel 接口文档才能比较准确的进行参数的配置。JDI Parallel 接口同 DPI 接口类似，使能后会循环不停从 FrameBuffer 地址读取数据送到屏幕上。只有当使能关闭后，JDI Parallel 接口才会在当前帧数据发送结束后停止。

10.2.4 LCDC 寄存器

LCDC 的基地址是 0x50008000。

表 10-1: LCDC 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**COMMAND**	
[31:2]			RSVD	
[1]	rw	1'h0	reset	1: reset the whole graphics 0: release the reset
[0]	w1t	1'h0	start	write 1 to trigger the lcd interface block
0x04			**STATUS**	
[31:3]			RSVD	
[2]	r	1'h0	JDI_PAR_RUN	JDI parallel interface is running
[1]	r	1'h0	DPI_RUN	DPI interface is running
[0]	r	1'h0	LCD_BUSY	LCS controll busy flag
0x08			**IRQ**	
[31:23]			RSVD	
[22]	rw1c	1'h0	LINE_DONE_RAW_STAT	raw_status of line process done interrupt
[21]	rw1c	1'h0	JDI_PAR_UDR_RAW_STAT	raw_status of jdi parallel interface under run interrupt
[20]	rw1c	1'h0	JDI_PARL_INTR_RAW_STAT	raw_status of jdi parallel interface line interrupt

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表 10-1: LCDC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[19]	rw1c	1'h0	DPI_UDR_RAW_STAT	raw status of dpi under run interrupt
[18]	rw1c	1'h0	DPIL_INTR_RAW_STAT	raw status of dpi line interrupt
[17]	rw1c	1'h0	ICB_OF_RAW_STAT	raw status of icb overflow interrupt
[16]	rw1c	1'h0	EOF_RAW_STAT	raw status of end of frame interrupt
[15:7]			RSVD	
[6]	rw1c	1'h0	LINE_DONE_STAT	line process done interrupt, masked by mask register
[5]	rw1c	1'h0	JDI_PAR_UDR_STAT	jdi parallel interface under run interrupt, masked by mask register
[4]	rw1c	1'h0	JDI_PARL_INTR_STAT	jdi parallel interface line interrupt, masked by mask register
[3]	rw1c	1'h0	DPI_UDR_STAT	dpi under run interrupt, masked by mask register
[2]	rw1c	1'h0	DPIL_INTR_STAT	dpi line interrupt, masked by mask register
[1]	rw1c	1'h0	ICB_OF_STAT	icb overflow interrupt, masked by mask register
[0]	rw1c	1'h0	EOF_STAT	end of frame interrupt, masked by mask register
0x0C			**SETTING**	
[31:27]			RSVD	
[26:16]	rw	11'h1ff	LINE_DONE_NUM	line number of line process done interrupt
[15:9]			RSVD	
[8]	rw	1'h1	AUTO_GATE_EN	auto clock gating enable
[7]			RSVD	
[6]	rw	1'h0	LINE_DONE_MASK	line process done interrupt, 0: mask the interrupt
[5]	rw	1'h0	JDI_PAR_UDR_MASK	jdi parallel interface under run interrupt mask, 0: mask the interrupt
[4]	rw	1'h0	JDI_PARL_INTR_MASK	jdi parallel interface line interrupt, 0: mask the interrupt
[3]	rw	1'h0	DPI_UDR_MASK	dpi under run interrupt mask, 0: mask the interrupt
[2]	rw	1'h0	DPIL_INTR_MASK	dpi line interrupt, 0: mask the interrupt
[1]	rw	1'h0	ICB_OF_MASK	icb overflow interrupt mask, 0: mask the interrupt
[0]	rw	1'h0	EOF_MASK	end of frame interrupt mask, 0: mask the interrupt
0x10			**CANVAS_TL_POS**	
[31:27]			RSVD	
[26:16]	rw	11'h0	Y0	
[15:11]			RSVD	
[10:0]	rw	11'h0	X0	
0x14			**CANVAS_BR_POS**	
[31:27]			RSVD	
[26:16]	rw	11'h0	Y1	
[15:11]			RSVD	
[10:0]	rw	11'h0	X1	
0x18			**CANVAS_BG**	
[31:28]			RSVD	
[27]	rw	1'h0	H_MIRROR	set 1 to do horizontal mirror for output image
[26]	rw	1'h0	LB_BYPASS	line buffer bypass. Set 1 to bypass line buffer.
[25]	rw	1'h0	ALL_BLENDING_BYPASS	if this bit is set, lcdc is in pure dma mode. No blending operation.
[24]	rw	1'h0	BG_BLENDING_BYPASS	if this bit is set, the layer is not blending with background. The alpha value will be reserved to output.
[23:16]	rw	8'h0	RED	Red color
[15:8]	rw	8'h0	GREEN	green color
[7:0]	rw	8'h0	BLUE	blue color
0x1C			**LAYER0_CONFIG**	
[31]			RSVD	
[30]	rw	1'h0	V_MIRROR	set 1 to do vertical mirror for the layer

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表 10-1: LCDC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[29]	rw	1'h0	ALPHA_BLEND	set 1 to enable alpha blending mode. Use layer alpha as blending factor for image with Alpha. Alpha_out = Layer_alpha * Image_alpha
[28]	rw	1'h0	ACTIVE	layer active flag
[27]	rw	1'h0	LINE_FETCH_MODE	line fetch mode 0: address skip every single line 1: address skip every two line
[26]	rw	1'h0	PREFETCH_EN	preload 64 bytes extra data when reading pixel from memory
[25:13]	rw	13'h0	WIDTH	source image width(including padding), unit is bytes
[12]	rw	1'h0	FILTER_EN	layer color filter enable
[11:4]	rw	8'h0	ALPHA	layer alpha value
[3]	rw	1'h0	ALPHA_SEL	alpha selection 1'b0: select alpha according to image format 1'b1: select layer alpha
[2:0]	rw	3'h0	FORMAT	overlay layer input format 3'h0: RGB565 3'h1: RGB888 3'h2: ARGB8888 3'h3: ARGB8565 3'h4: RGB332 3'h5: A8 3'h6: L8 others: reserved
0x20			**LAYER0_TL_POS**	
[31:27]			RSVD	
[26:16]	rw	11'h0	Y0	Coordingate Y-value
[15:11]			RSVD	
[10:0]	rw	11'h0	X0	Coordinate X-value
0x24			**LAYER0_BR_POS**	
[31:27]			RSVD	
[26:16]	rw	11'h0	Y1	Coordingate Y-value
[15:11]			RSVD	
[10:0]	rw	11'h0	X1	Coordinate X-value
0x28			**LAYER0_FILTER**	
[31:24]	rw	8'h0	FILTER_MASK	layer color filter mask
[23:16]	rw	8'h0	FILTER_R	filter r color
[15:8]	rw	8'h0	FILTER_G	filter g color
[7:0]	rw	8'h0	FILTER_B	filter b color
0x2C			**LAYER0_SRC**	
[31:0]	rw	32'h0	ADDR	source image RGB data address[31:0]. For RGB565 format, address should be aligned to halfword. For ARGB8888 format, address should be aligned to word.
0x30			**LAYER0_FILL**	
[31:26]			RSVD	
[25]	rw	1'h0	ENDIAN	input 565 data format endian 0: R[4:0], G[5:3], G[2:0], B[4:0] 1: G[2:0], R[4:0], B[4:0], G[5:3]
[24]	rw	1'h0	BG_MODE	not used
[23:16]	rw	8'h0	BG_R	background r color

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表 10-1: LCDC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[15:8]	rw	8'h0	BG_G	background g color
[7:0]	rw	8'h0	BG_B	background b color
0x34			**LAYER0_DECOMP**	
[31:24]			RSVD	
[23:13]	rw	11'h0	col_size	number of colums in a line of original image, max column size is 1024
[12:1]	rw	12'h0	target_words	size of a single channel data before decompression. Unit is half word. Each line has 3 channels. So for each line, the compressed data size is target_words * 3 * 2 bytes.
[0]	rw	1'h0	enable	decompression enable
0x38			**LAYER0_DECOMP_CFG0**	
[31:20]	rw	12'h10	cfg0_reserved	
[19:16]	rw	4'h5	lossless_qidx2	condition to decrease qidx
[15:12]	rw	4'h5	lossless_qidx1	up level for adjusted qidx value for low quality block
[11:8]	rw	4'h9	use_lossless_qidx	condition to increase qidx
[7:4]	rw	4'h8	extra_threshold	the threshold to distinguish high/low quality block
[3:0]	rw	4'h2	extra_high	extra bit for high quality bit
0x3C			**LAYER0_DECOMP_CFG1**	
[31:28]	rw	4'h8	extra_low	extra bit for low quality block
[27:24]	rw	4'h0	block_min_qidx	minimum qidx for block mode
[23:20]	rw	4'h0	line_min_qidx	minimum qidx for line mode
[19:16]	rw	4'h2	failover_bits_b	failover compression mode target bits(Blue)
[15:12]	rw	4'h3	failover_bits_g	failover compression mode target bits(Green)
[11:8]	rw	4'h3	failover_bits_r	failover compression mode target bits(Red)
[7:2]	rw	6'h1	cfg1_reserved	
[1]	rw	1'b1	dither	dithering function 0: off 1: on
[0]	rw	1'b1	block_width	block_size in pixel unit. 0: 16 pixels 1: 32 pixels Small block size will cause more blocks and more bits to store block information.
0x40			**LAYER0_DECOMP_STAT**	
[31:7]			RSVD	
[6:0]	r	7'h0	buf_max_depth	buf max usage
0x60			**LAYER1_CONFIG**	
[31]			RSVD	
[30]	rw	1'h0	V_MIRROR	set 1 to do vertical mirror for the layer
[29]	rw	1'h0	ALPHA_BLEND	set 1 to enable alpha blending mode. Use layer alpha as blending factor for image with Alpha. Alpha_out = Layer_alpha * Image_alpha
[28]	rw	1'h0	ACTIVE	layer active flag
[27]	rw	1'h0	LINE_FETCH_MODE	line fetch mode 0: address skip every single line 1: address skip every two line
[26]	rw	1'h0	PREFETCH_EN	preload 64 bytes extra data when reading pixel from memory
[25:13]	rw	13'h0	WIDTH	source image width(including padding), unit is bytes
[12]	rw	1'h0	FILTER_EN	layer color filter enable
[11:4]	rw	8'h0	ALPHA	layer alpha value

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表 10-1: LCDC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[3]	rw	1'h0	ALPHA_SEL	alpha selection 1'b0: select alpha according to image format 1'b1: select layer alpha
[2:0]	rw	3'h0	FORMAT	overlay layer input format 3'h0: RGB565 3'h1: RGB888 3'h2: ARGB8888 3'h3: ARGB8565 3'h4: RGB332 3'h5: A8 3'h6: L8 others: reserved
0x64			**LAYER1_TL_POS**	
[31:27]			RSVD	
[26:16]	rw	11'h0	Y0	Coordingate Y-value
[15:11]			RSVD	
[10:0]	rw	11'h0	X0	Coordinate X-value
0x68			**LAYER1_BR_POS**	
[31:27]			RSVD	
[26:16]	rw	11'h0	Y1	Coordingate Y-value
[15:11]			RSVD	
[10:0]	rw	11'h0	X1	Coordinate X-value
0x6C			**LAYER1_FILTER**	
[31:24]	rw	8'h0	FILTER_MASK	layer color filter mask
[23:16]	rw	8'h0	FILTER_R	filter r color
[15:8]	rw	8'h0	FILTER_G	filter g color
[7:0]	rw	8'h0	FILTER_B	filter b color
0x70			**LAYER1_SRC**	
[31:0]	rw	32'h0	ADDR	source image RGB data address[31:0]. For RGB565 format, address should be aligned to halfword. For ARGB8888 format, address should be aligned to word.
0x74			**LAYER1_FILL**	
[31:26]			RSVD	
[25]	rw	1'h0	ENDIAN	input 565 data format endian 0: R[4:0], G[5:3], G[2:0], B[4:0] 1: G[2:0], R[4:0], B[4:0], G[5:3]
[24]	rw	1'h0	BG_MODE	not used
[23:16]	rw	8'h0	BG_R	background r color
[15:8]	rw	8'h0	BG_G	background g color
[7:0]	rw	8'h0	BG_B	background b color
0x78			**DITHER_CONF**	
[31:13]			RSVD	
[12]	w1t	1'h0	lfsr_load	load lfsr init value
[11:10]	rw	2'h0	lfsr_load_sel	select lfsr 0: none 1: red 2: green 3: blue
[9:7]	rw	3'h0	w_r	red dither width

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表 10-1: LCDC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[6:4]	rw	3'h0	w_g	green dither width
[3:1]	rw	3'h0	w_b	blue dither width
[0]	rw	1'h0	en	dither enable
0x7C			**DITHER_LFSR**	
[31:0]	rw	32'h0	init_val	lfsr init load value
0x80			**LCD_CONF**	
[31:21]			RSVD	
[20:19]	rw	2'h0	SPI_RD_SEL	spi read line select. 0: select line 0 1: select line 1 2: select line 2 3: select line 3
[18]	rw	1'h0	ENDIAN	LCD 565 data format endian, this bit would affect SPI, DPI, DBI and AHB interface 565 format 0: R[4:0], G[5:3], G[2:0], B[4:0] 1: G[2:0], R[4:0], B[4:0], G[5:3]
[17]	rw	1'h0	DIRECT_INTF_EN	when the target LCD is AHB LCD, this bit enable the direct interface to DSI module. Direct interface has higher bandwidth and speed than AHB interface.
[16:15]	rw	2'h0	JDI_SER_FORMAT	JDI serial format 2'b00: 3-bit mode 2'b01: 4-bit mode 2'b10: 1-bit mode 2'b11: reserved
[14:12]	rw	3'h0	DPI_LCD_FORMAT	DPI LCD format 3'b000: 16-bit conf1 3'b001: 16-bit conf2 3'b010: 16-bit conf3 3'b011: 18-bit conf1 3'b100: 18-bit conf2 3'b101: 24-bit others: Reserved
[11:10]	rw	2'h0	SPI_LCD_FORMAT	SPI LCD format 2'b00: 8-bit RGB 3:3:2 2'b01: 16-bit RGB 5:6:5 2'b10: 24-bit RGB 8:8:8 2'b11: Reserved
[9:8]	rw	2'h0	AHB_FORMAT	AHB LCD/RAM output format: 0: RGB565 1: RGB888 2: ARGB8888 3: RGB332

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表 10-1: LCDC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7:5]	rw	3'h0	LCD_FORMAT	LCD output format: 3'b000: 8-bit RGB 3:3:2 3'b001: 16-bit RGB 5:6:5 over 8-bit bus, 2 cycles/pixel 3'b010: 12-bit RGB 4:4:4 3'b011: 16-bit RGB 5:6:5 3'b100: 18-bit RGB 6:6:6 3'b101: 24-bit RGB 8:8:8 3'b110: 24-bit RGB 8:8:8 over 16-bit bus, 1.5 cycles/pixel 3'b111: 24-bit RGB 8:8:8 over 8-bit bus, 3cycles/pixel others: Reserved
[4:2]	rw	3'h0	LCD_INTF_SEL	3'b000: 8080 DBI Type B 3'b001: SPI interface 3'b010: DBI to DSI interface 3'b011: DPI interface 3'b100: JDI serial interface 3'b101: JDI parallel interface 3'b110: 8080 DBI Type A 3'b111: DPI to DSI interface
[1:0]	rw	2'h0	TARGET_LCD	The Data can be sent to four destinations: 2'b00: LCD panel 0 2'b01: LCD panel 1 2'b10: AHB LCD 2'b11: AHB RAM
0x84			**LCD_IF_CONF**	
[31:26]			RSVD	
[25]	rw	1'h0	CTRL_DLY_SET	if this bit is set to 1, LCD control output will be delayed for 1 lcdc clock cycle
[24]	rw	1'h0	DO_DLY_SET	if this bit is set to 1, LCD data output will be delayed for 1 lcdc clock cycle
[23]	rw	1'h0	LCD_RSTB	LCD RSTB pin, direct to output
[22]	rw	1'h0	RD_POL	LCD RD pin polarity. RD is 0 for write operation, 1 for idle if polarity bit is set as 0. RD bit definition is opposite if polarity bit is set as 1.
[21]	rw	1'h0	WR_POL	LCD WR pin polarity. WR is 0 for write operation, 1 for idle if polarity bit is set as 0. WR bit definition is opposite if polarity bit is set as 1.
[20]	rw	1'h0	RS_POL	LCD RS pin polarity. RS is 1 for data access, 0 for command access if polarity bit is set as 0. RS bit definition is opposite if polarity bit is set as 1.
[19]	rw	1'h0	CS1_POL	LCD0 CS pin polarity. CS is 0 for LCD chip select if polarity bit is set as 0. CS bit definition is opposite if polarity bit is set as 1.
[18]	rw	1'h0	CS0_POL	LCD1 CS pin polarity. CS is 0 for LCD chip select if polarity bit is set as 0. CS bit definition is opposite if polarity bit is set as 1.
[17:12]	rw	6'h0	PWH	inactive cycles of LCD_WR/LCD_RD for consecutive write/read operation
[11:6]	rw	6'h0	PWL	active cycles of LCD_WR/LCD_RD
[5:3]	rw	3'h0	TAH	hold cycles, delay from LCD_WR/LCD_RD inactive to LCD_CS inactive
[2:0]	rw	3'h0	TAS	setup cycles, delay from LCD_CS active to LCD_WR/LCD_RD active
0x88			**LCD_MEM**	
[31:0]	rw	32'h0	ADDR	address for AHB LCD/AHB RAM
0x8C			**LCD_O_WIDTH**	
[31:16]			RSVD	
[15:0]	rw	16'h0	OFFSET	AHB RAM address offset for each line
0x90			**LCD_SINGLE**	
[31:4]			RSVD	

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表 10-1: LCDC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[3]	r	1'h0	LCD_BUSY	LCD/SPI LCD interface is busy for single access
[2]	w1t	1'h0	RD_TRIG	Single read operation trigger
[1]	w1t	1'h0	WR_TRIG	Single write operation trigger
[0]	rw	1'h0	TYPE	LCD access type, this bit could affect all LCD interface including SPI, parellel and AHB 1'b0: command 1'b1: data
0x94			**LCD_WR**	
[31:0]	rw	32'h0	DATA	LCD write data
0x98			**LCD_RD**	
[31:0]	r	32'h0	DATA	LCD read data
0x9C			**SPI_IF_CONF**	
[31]			RSVD	
[30]	rw	1'h0	SPI_CLK_INIT	SPI CLK idle state value 1'h0: high 1'h1: low
[29]	rw	1'h0	SPI_CLK_POL	SPI CLK polarity 1'h0: normal 1'h1: inverted
[28]	rw	1'h0	SPI_CS_POL	SPI CS polarity 0: low active 1: high active
[27]	rw	1'h1	SPI_CS_AUTO_DIS	1: SPI CS is automatically disabled after data transaction 0: SPI CS is not disabled after data transaction
[26]	rw	1'h0	SPI_CS_NO_IDLE	1: SPI CS is always active during data transaction 0: SPI CS is IDLE in wait state during data transaction
[25]	rw	1'h0	SPI_CLK_AUTO_DIS	1: SPI clock auto disable in wait state during data transaction 0: SPI clock is always on in wait state during data transaction
[24]	rw	1'h0	SPI_RD_MODE	SPI read mode: 1'b0: normal read. Send write request before read. 1'b1: direct read. Read data without write request.
[23:22]	rw	2'h0	WR_LEN	SPI write data length(single access)
[21:20]	rw	2'h0	RD_LEN	SPI read data length(single access)
[19:17]	rw	3'h0	LINE	SPI line mode 0: 4-line 1: 4-line with 2 data line(support RGB565 and RGB888) 2: 4-line with 4 data line(support RGB565 and RGB888) 3: reserved 4: 3-line 5: 3-line with 2 data line(support RGB565 and RGB888) 6: 3-line with 4 data line(support RGB565 and RGB888) 7: reserved
[16:14]	rw	3'h0	DUMMY_CYCLE	SPI transaction dummy cycle
[13:6]	rw	8'ha	CLK_DIV	SPI clock divider
[5:0]	rw	6'h0	WAIT_CYCLE	SPI line wait cycle, wait cycle is after each line and is according to SPI clock. 0 refers to no wait cycle.
0xA0			**TE_CONF**	
[31:21]			RSVD	

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表 10-1: LCDC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[20]	rw	1'h0	FMARK_SOURCE	TE signal source 1: use TE signal from DSI 0: use TE signal from external pin
[19]	rw	1'h0	FMARK_MODE	TE signal trigger mode 1: edge trigger 0: pulse trigger
[18:3]	rw	16'h0	VSYNC_DET_CNT	vsync signal detect counter, used for mode 1 to detect vsync signal
[2]	rw	1'h0	MODE	0: vsync only TE mode 1: vsync+hsync TE mode
[1]	rw	1'h0	FMARK_POL	TE signal polarity
[0]	rw	1'h0	ENABLE	TE enable
0xA4			**TE_CONF2**	
[31:0]	rw	32'h0	DLY_CNT	TE delay counter
0xA8			**DPI_IF_CONF1**	
[31:27]			RSVD	
[26:16]	rw	11'h0	HSW	dpi hsync width
[15:11]			RSVD	
[10:0]	rw	11'h0	VSH	dpi vsync height
0xAC			**DPI_IF_CONF2**	
[31:27]			RSVD	
[26:16]	rw	11'h0	HBP	horizontal back porch
[15:11]			RSVD	
[10:0]	rw	11'h0	VBP	vertical back porch
0xB0			**DPI_IF_CONF3**	
[31:27]			RSVD	
[26:16]	rw	11'h0	HFP	horizontal front porch
[15:11]			RSVD	
[10:0]	rw	11'h0	VFP	vertical front porch
0xB4			**DPI_IF_CONF4**	
[31:27]			RSVD	
[26:16]	rw	11'h0	HAW	horizontal active width
[15:11]			RSVD	
[10:0]	rw	11'h0	VAH	vertical active height
0xB8			**DPI_IF_CONF5**	
[31:24]			RSVD	
[23]	rw	1'h0	clk_force_on	1: force DPI clock on 0: DPI clock is controlled by hardware
[22:12]	rw	11'h7ff	INT_LINE_NUM	DPI interrupt line number
[11]	rw	1'h0	HSPOL	hsync polarity
[10]	rw	1'h0	VSPOL	vsync polarity
[9]	rw	1'h0	DEPOL	de polarity
[8]	rw	1'h0	PCLKPOL	pixel clock polarity
[7:0]	rw	8'h1	PCLK_DIV	pixel clock divider
0xBC			**DPI_CTRL**	
[31:4]			RSVD	
[3]	rw	1'h0	DPI_UC	dpi update config
[2]	rw	1'h0	DPI_SD	dpi shutdown
[1]	rw	1'h0	DPI_CM	dpi color mode

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表 10-1: LCDC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[0]	rw	1'h0	DPI_EN	dpi interface enable
0xC0			**DPI_STAT**	
[31:16]	r	16'h1	VPOS	dpi vertical position
[15:14]			RSVD	
[13:11]	r	3'h0	HSTAT	horizontal status 0: idle 1: prep 2: hsync 3: hbp 4: hact 5: hfp 6: wait
[10:0]	r	11'h1	HPOS	dpi horizontal position
0xC4			**JDI_SER_CONF1**	
[31:16]			RSVD	
[15:8]	rw	8'h2	CLK_DIV	jdi serial clock divider
[7:5]			RSVD	
[4:0]	rw	5'd1	WR_LEN	jdi single write bit length
0xC8			**JDI_SER_CONF2**	
[31:16]	rw	16'h0	INIT_LINE_CNT	jdi serial init line counter
[15:0]	rw	16'h0	WR_CMD	jdi serial data transfer write command
0xCC			**JDI_SER_CTRL**	
[31:2]			RSVD	
[1]	rw	1'h0	EXTCOMIN	jdi serial interface extcomin control
[0]	rw	1'h0	DISP	jdi serial interface disp control
0xD0			**JDI_PAR_CONF1**	
[31:16]	rw	16'h0	MAX_LINE	jdi parallel interface max line, line number start from 0
[15:0]	rw	16'h0	MAX_COL	jdi parallel interface max column, column number start from 0
0xD4			**JDI_PAR_CONF2**	
[31:16]	rw	16'h0	ST_LINE	jdi parallel interface start line, line number start from 0
[15:0]	rw	16'h0	END_LINE	jdi parallel interface end line, line number start from 0
0xD8			**JDI_PAR_CONF3**	
[31:16]	rw	16'h0	ST_COL	jdi parallel interface start column, column number start from 0
[15:0]	rw	16'h0	END_COL	jdi parallel interface end column, column number start from 0
0xDC			**JDI_PAR_CONF4**	
[31:16]	rw	16'h0	HCK_WIDTH	jdi parallel interface HCK width, HSK width = lcd_ck_cycle * HCK_WIDTH
[15:0]	rw	16'h0	HST_WIDTH	jdi parallel interface HST width, HST width = lcd_ck_cycle * HST_WIDTH
0xE0			**JDI_PAR_CONF5**	
[31:16]	rw	16'h0	VCK_WIDTH	jdi parallel interface VCK width, VCK width = lcd_ck_cycle * VCK_WIDTH
[15:0]	rw	16'h0	VST_WIDTH	jdi parallel interface VST width, VST width = lcd_ck_cycle * VST_WIDTH
0xE4			**JDI_PAR_CONF6**	
[31:16]	rw	16'h0	VCK_DLY	jdi parallel interface VST to VCK delay, VST2VCK delay = lcd_ck_cycle * VCK_DLY
[15:0]	rw	16'h0	HST_DLY	jdi parallel interface VCK to HST delay, VCK2HST delay = lcd_ck_cycle * HST_DLY
0xE8			**JDI_PAR_CONF7**	
[31:17]			RSVD	

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表 10-1: LCDC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[16]	rw	1'h0	DP_MODE	double pixel mode. Some jdi parallel screens use large pixel+small pixel structure. Set this bit to 1 to support this structure.
[15:0]	rw	16'h0	HCK_DLY	jdi parallel interface HST to HCK delay
0xEC			**JDI_PAR_CTRL**	
[31:16]	rw	16'hffff	INT_LINE_NUM	jdi parallel interface interrupt line number, line number start from 0.
[15:10]			RSVD	
[9]	rw	1'h0	VSTPOL	jdi parallel vst polarity
[8]	rw	1'h0	VCKPOL	jdi parallel vck polarity
[7]	rw	1'h0	HSTPOL	jdi parallel hst polarity
[6]	rw	1'h0	HCKPOL	jdi parallel hck polarity
[5]	rw	1'h0	ENBPOL	jdi parallel enb polarity
[4]	rw	1'h0	XRST	jdi parallel interface XRST
[3:1]			RSVD	
[0]	rw	1'h0	ENABLE	jdi parallel interface enable
0xF0			**JDI_PAR_STAT**	
[31:16]	r	16'h0	VPOS	jdi parallel vertical position
[15:0]	r	16'h0	HPOS	jdi parallel horizontal position
0xF4			**JDI_PAR_EX_CTRL**	
[31]	r	1'h0	VCOM	VCOM value
[30]	r	1'h0	FRP	FRP value
[29]	r	1'h0	XFRP	XFRP value
[28]	rw	1'h0	CNT_EN	VCOM/FRP/XFRP counter enable
[27:24]			RSVD	
[23:0]	rw	24'h0	MAX_CNT	VCOM/FRP/XFRP max counter
0xF8			**JDI_PAR_CONF8**	
[31:16]	rw	16'h0	ENB_ST_COL	jdi parallel interface enb start column, column number start from 0
[15:0]	rw	16'h0	ENB_END_COL	jdi parallel interface enb end column, column number start from 0
0xFC			**JDI_PAR_CONF9**	
[31:16]	rw	16'h0	ENB_ST_LINE	jdi parallel interface enb start line, line number start from 0
[15:0]	rw	16'h0	ENB_END_LINE	jdi parallel interface enb end line, line number start from 0
0x100			**JDI_PAR_CONF10**	
[31:16]	rw	16'h0	HC_ST_LINE	jdi parallel interface horizontal control start line, line number start from 0
[15:0]	rw	16'h0	HC_END_LINE	jdi parallel interface horizontal control end line, line number start from 0
0x110			**CANVAS_STAT0**	
[31:27]			RSVD	
[26:16]	r	11'h0	y_cor	canvas y cordinate
[15:11]			RSVD	
[10:0]	r	11'h0	x_cor	canvas x cordinate
0x114			**CANVAS_STAT1**	
[31:12]			RSVD	
[11:9]	r	3'h0	fetch_stat	fetch status
[8:6]	r	3'h0	prec_stat	prec status
[5:3]	r	3'h0	postc_stat	postc_status
[2:0]	r	3'h0	fifo_cnt	pre calc fifo count
0x118			**OL0_STAT**	
[31:24]			RSVD	
[23:22]	r	2'h0	sc_lb0	
[21:20]	r	2'h0	sc_lb1	

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表 10-1: LCDC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[19:16]	r	4'h0	sc_fe	
[15:13]	r	3'h0	sc_be	
[12:11]	r	2'h0	sc_out	
[10:8]	r	3'h0	pf_pr	
[7:6]	r	2'h0	pf_df	
[5:4]	r	2'h0	data_conv	
[3:2]	r	2'h0	prefetch_read	
[1]	r	1'h0	prefetch_out	
[0]	r	1'h0	done_req	
0x11C			**OL1_STAT**	
[31:11]			RSVD	
[10:8]	r	3'h0	pf_pr	
[7:6]	r	2'h0	pf_df	
[5:4]	r	2'h0	data_conv	
[3:2]	r	2'h0	prefetch_read	
[1]	r	1'h0	prefetch_out	
[0]	r	1'h0	done_req	
0x120			**MEM_IF_STAT**	
[31:10]			RSVD	
[9:7]	r	3'h0	arb_main	
[6:4]	r	3'h0	arb_read_port	
[3:0]	r	4'h0	ahb	
0x124			**PERF_CNT**	
[31:0]	rw	32'h0	VAL	lcdc performance counter

10.3 eZip™ 无损压缩解码器

eZip™ 解码器是基于自有算法的实时无损解压缩模块，压缩率与 Zip 格式相当。它可以用于将通用数据解码后保存，以此加快数据的实时加载能力。如果数据是从芯片外部传输，压缩后的传输有助于缩短传输时间，减少传输功耗。

此外，eZip™ 还支持专有格式的图片压缩，压缩率与 PNG 格式相当，并支持独立 DMA 操作或与 ePicasso™ 联动读取。当独立操作时，eZip™ 可通过 DMA 机制，可以灵活地将存储在 Flash 或 RAM 的压缩图片解压缩并搬运至目标缓存中。在联动模式下，ePicasso™ 通过 eZip™ 模块，实时从存储中读取图片并实时解压缩，然后按照一般的图形流程进行所需要的 2.5D 计算，从而省去了暂存解压缩图片的缓存。

通过以上机制，eZip™ 可以有效地降低图像素材对存储容量的需求，在有限的存储中最大化素材的丰富度，减小对片外存储的带宽要求，从而提高大大系统的整体运行效率。

eZip™ 模块是将 eZip™ 压缩图片进行解码输出的模块。该模块通过 AHB 总线读入压缩数据，解码后的图像数据可配置通过 AHB 总线输出或直接送给 epic 模块进行后续处理。

该模块具有以下特点：

- 通过 AHB 总线输入\输出的数据地址可配
- 输出图片数据可直接送给 epic 模块
- 可输出一个指定区域的图片数据

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10.4 DCMI

10.4.1 DCMI 简介

数字摄像头接口是一种同步并行接口，能够接收来自外部 8 位、10 位、12 位、14 位或 16 位 CMOS 摄像头模块的高速数据流。它支持多种数据格式：YCbCr4:2:2/RGB565 逐行视频以及压缩数据（JPEG）。

该接口适用于黑白摄像头、X24 和 X5 摄像头，并且假定所有预处理（如尺寸缩放）均在摄像头模块中完成。

10.4.2 DCMI 主要特性

- 支持 8-bit/10-bit/12-bit/14-bit/16-bit DVP 格式数据
- 支持 4 线/双线/单线 SPI 数据
- 支持连续模式以及单帧模式
- 支持裁剪模式

10.4.3 DCMI 功能概述

数字摄像头接口是一种同步并行接口，能够接收高速的数据流。它由最多 16 条数据线（D15-D0）和一条像素时钟线（DCMI_PIXCLK）组成。像素时钟的极性可编程，因此可以在像素时钟的上升沿或下降沿采集数据。

数据被打包到一个 32 位数据寄存器（DCMI_DR）中，然后通过一个通用 DMA 通道传输。图像缓冲区由 DMA 管理，而不是由摄像头接口管理。

10.4.4 DCMI 框图

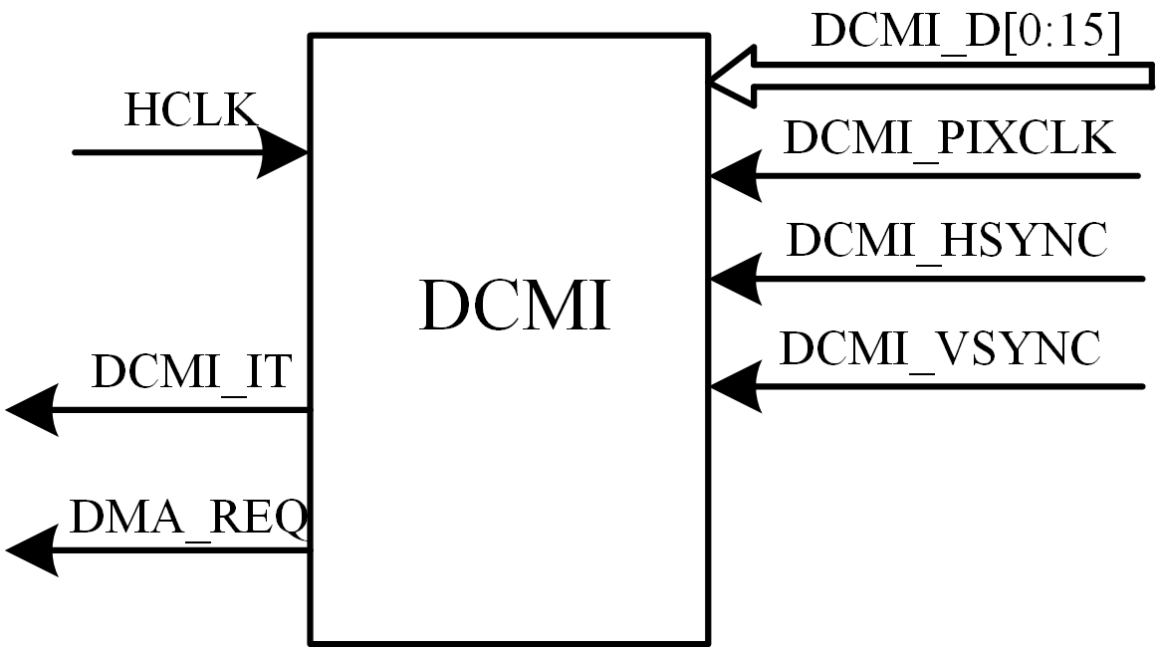


图 10-2: DCMI 结构图

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10.4.5 DMA 接口

当 DCMI_CR 寄存器中的 CAPTURE 位置位时，DMA 接口有效。每当摄像头接口在其寄存器中接收到一次 DMA 数据块时，就会产生一次 DMA 请求。

10.4.6 DCMI 物理接口

该接口由 11/13/15/17/19 个输入引脚组成。仅支持从模式（Slave mode）。

摄像头接口可根据 DCMI_CR 寄存器中的 EDM[2:0] 位采集 8 位、10 位、12 位、14 位或 16 位数据。

数据与 DCMI_PIXCLK 同步，并根据极性在像素时钟的上升沿/下降沿发生变化。

DCMI_HSYNC 信号指示一行的开始/结束。

DCMI_VSYNC 信号指示一帧的开始/结束。

8 位数据

当 DCMI_CR 中的 EDM[2:0] 编程为"000" 时，接口在其输入端（DCMI_D[0:7]）采集 8 个最低有效位，并将其存储为 8 位数据。DCMI_D[13:8] 输入被忽略。在这种情况下，要采集一个 32 位字，摄像头接口需要四个像素时钟周期。第一个采集到的数据字节被放置在 32 位字的 LSB 位置，第 4 个采集到的数据字节被放置在 32 位字的 MSB 位置。

10 位数据

当 DCMI_CR 中的 EDM[2:0] 编程为"001" 时，摄像头接口在其输入端 DCMI_D[0..9] 采集 10 位数据，并将其存储为一个 16 位字的 10 个最低有效位。DCMI_DR 寄存器中剩余的最高有效位（第 11 至 15 位）被清零。因此，在这种情况下，每两个像素时钟周期组成一个 32 位数据字。第一个采集到的数据被放置在 32 位字的 LSB 位置，第 2 个采集到的数据被放置在 32 位字的 MSB 位置。

12 位数据

当 DCMI_CR 中的 EDM[2:0] 编程为"010" 时，摄像头接口在其输入端 DCMI_D[0..11] 采集 12 位数据，并将其存储为一个 16 位字的 12 个最低有效位。剩余的最高有效位被清零。因此，在这种情况下，每两个像素时钟周期组成一个 32 位数据字。第一个采集到的数据被放置在 32 位字的 LSB 位置，第 2 个采集到的数据被放置在 32 位字的 MSB 位置。

14 位数据

当 DCMI_CR 中的 EDM[2:0] 编程为"011" 时，摄像头接口在其输入端 DCMI_D[0..13] 采集 14 位数据，并将其存储为一个 16 位字的 14 个最低有效位。剩余的最高有效位被清零。因此，在这种情况下，每两个像素时钟周期组成一个 32 位数据字。第一个采集到的数据被放置在 32 位字的 LSB 位置，第 2 个采集到的数据被放置在 32 位字的 MSB 位置。

16 位数据

当 DCMI_CR 中的 EDM[2:0] 编程为"011" 时，摄像头接口在其输入端 DCMI_D[0..15] 采集 16 位数据。因此，在这种情况下，每两个像素时钟周期组成一个 32 位数据字。第一个采集到的数据被放置在 32 位字的 LSB 位置，第 2 个采集到的数据被放置在 32 位字的 MSB 位置。

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采集模式

该接口支持两种采集类型：快照（单帧）和连续采集。

快照模式（单帧）

在此模式下，采集单帧图像（DCMI_CR 寄存器中 CM = "1"）。在 DCMI_CR 中置位 CAPTURE 位之后，接口等待检测到帧起始，然后开始采样数据。接收到第一个完整帧后，摄像头接口自动禁用（DCMI_CR 中的 CAPTURE 位需要手动清除）。如果使能了中断，则会产生 frame 中断。

连续采集模式

在此模式下（DCMI_CR 中 CM 位 = "0"），一旦在 DCMI_CR 中置位 CAPTURE 位，采集过程就会在下一个 DCMI_VSYNC 开始。该过程一直持续到 DCMI_CR 中的 CAPTURE 位被清零为止。CAPTURE 位被清零后，采集过程会一直持续到当前帧结束。

裁剪功能

借助裁剪功能，摄像头接口可以从接收到的图像中选择一个矩形窗口。起始（左上角）坐标和窗口大小（水平方向以像素时钟数表示，垂直方向以行数表示）通过两个 32 位寄存器（DCMI_CWSTRT 和 DCMI_CWSIZE）来指定。窗口大小以像素时钟数（水平方向）和行数（垂直方向）指定。

这些寄存器将采集窗口起始点的坐标指定为行号（在帧内，从 0 开始）和像素时钟数（在行内，从 0 开始），并将窗口大小指定为行数和像素时钟数。CAPCNT 值只能是 4 的倍数（两个最低有效位被强制为 0），以便数据能够通过 DMA 正确传输。

如果在 DCMI_CWSIZE 寄存器中指定的行数到达之前，DCMI_VSYNC 信号变为有效，则采集停止，并在中断使能时产生 IT_FRAME 中断。

10.4.7 DCMI 寄存器

DCMI 的基地址是 0x50040000。

表 10-2: DCMI 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**cr**	
[31:26]			RSVD	
[25]	rw	1'h0	ipi_en	0x0:parallel interface ; 0x1: spi_interface
[24]	rw	1'h0	if_sel	0x0:parallel interface ; 0x1: spi_interface
[23]	r	1'h1	rstb_s	
[22]	w1c	1'h0	rstb	
[21]	rw	1'h0	fclken	
[20:16]	rw	5'h1	fclkdiv	
[15]	rw	1'h0	ess_swap	
[14]	rw	1'h0	enable	
[13]			RSVD	
[12:10]	rw	3'h0	edm	
[9]	rw	1'h0	half_word_swap	
[8]	rw	1'h0	bit_swap	
[7]	rw	1'h1	vspol	

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表 10-2: DCMI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[6]	rw	1'h1	hspol	
[5]	rw	1'h1	pckpol	
[4]	rw	1'h0	ess	
[3]	rw	1'h0	jpeg	
[2]	rw	1'h0	crop	0x0:parallel interface ; 0x1: spi_interface
[1]	rw	1'h0	cm	
[0]	rw	1'h0	capture	
0x4			**sr**	
[31:3]			RSVD	
[2]	r	1'h0	fne	
[1]	r	1'h0	vsync	
[0]	r	1'h0	hsync	
0x8			**ris**	
[31:6]			RSVD	
[5]	r	1'h0	pack_size_err_ris	
[4]	r	1'h0	line_ris	
[3]	r	1'h0	vsync_ris	
[2]	r	1'h0	fsm_err_ris	
[1]	r	1'h0	ovr_ris	
[0]	r	1'h0	frame_ris	
0xc			**ie**	
[31:6]			RSVD	
[5]	rw	1'h0	pack_size_err_ie	
[4]	rw	1'h0	line_ie	
[3]	rw	1'h0	vsync_ie	
[2]	rw	1'h0	fsm_err_ie	
[1]	rw	1'h0	ovr_ie	
[0]	rw	1'h0	frame_ie	
0x10			**mis**	
[31:6]			RSVD	
[5]	r	1'h0	pack_size_err_mis	
[4]	r	1'h0	line_mis	
[3]	r	1'h0	vsync_mis	
[2]	r	1'h0	fsm_err_mis	
[1]	r	1'h0	ovr_mis	
[0]	r	1'h0	frame_mis	
0x14			**isc**	
[31:6]			RSVD	
[5]	w1c	1'h0	pack_size_err_isc	
[4]	w1c	1'h0	line_isc	
[3]	w1c	1'h0	vsync_isc	
[2]	w1c	1'h0	fsm_err_isc	
[1]	w1c	1'h0	ovr_isc	
[0]	w1c	1'h0	frame_isc	
0x18			**escr**	
[31:24]	rw	8'hff	fec	
[23:16]	rw	8'hff	lec	
[15:8]	rw	8'hff	lsc	

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表 10-2: DCMI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7:0]	rw	8'hff	fsc	
0x1c			**esur**	
[31:24]	rw	8'hff	feu	
[23:16]	rw	8'hff	leu	
[15:8]	rw	8'hff	lsu	
[7:0]	rw	8'hff	fsu	
0x20			**cwstrt**	
[31:29]			RSVD	
[28:16]	rw	13'h0	vst	
[15:14]			RSVD	
[13:0]	rw	14'h0	hoffcnt	
0x24			**cwsize**	
[31:30]			RSVD	
[29:16]	rw	14'h0	vline	
[15:14]			RSVD	
[13:0]	rw	14'h0	capcnt	
0x38			**dr**	
[31:0]	r	32'h0	data	
0x7c			**spi_cr**	
[31:24]			RSVD	
[23:8]	rw	16'h3c0	packet_size	
[7]	rw	1'h1	line_num_en	
[6]	rw	1'h1	low_byte_first	
[5]	rw	1'h0	data_msb_first	
[4]	rw	1'h0	header_msb_first	
[3]	rw	1'h0	di_swap	
[2:1]	rw	2'h2	di_sel	0x0: one-wire spi;0x1 two-wire spi;0x2 four-wire spi
[0]	rw	1'h1	mtk_mode	
0x80			**spi_sync**	
[31:24]			RSVD	
[23:0]	rw	24'hffffff	word	
0x84			**spi_pkt_id**	
[31:24]	rw	8'h40	line_end	
[23:16]	rw	8'h02	line_start	
[15:8]	rw	8'h00	frame_end	
[7:0]	rw	8'h01	frame_start	
0x88			**bp**	
[31:8]			RSVD	
[7:6]	rw	2'h3	byte3_po	
[5:4]	rw	2'h2	byte2_po	
[3:2]	rw	2'h1	byte1_po	
[1:0]	rw	2'h0	byte0_po	
0x8c			**spi_sr**	
[31:16]	r	16'h0	packet_size	
[15:0]	r	16'h0	line_num	
0x90			**dma_cr**	
[31:5]			RSVD	
[4:0]	rw	5'h10	dma_num	

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表 10-2: DCMI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x94			**dbg_cr**	
[31:5]			RSVD	
[4]	rw	1'h0	dbg_en	
[3:0]	rw	4'h0	dbg_sel	
0x98			**yuv2rgb_cr1**	
[31]	rw	1'h0	enable	
[30]	rw	1'h0	range_sel	
[29:20]	rw	10'd298	fy	
[19:10]	rw	10'd100	fug	
[9:0]	rw	10'd516	fub	
0x9c			**yuv2rgb_cr2**	
[31:20]			RSVD	
[19:10]	rw	10'd409	fvr	
[9:0]	rw	10'd208	fvg	
0xa0			**jpeg_byte**	
[31:0]	r	32'd0	count	
0xa4			**ipi_cr**	
[31:5]			RSVD	
[4]	rw	1'd0	embedded_bypass	
[3:0]	rw	4'd0	data_type	
0xa8			**conv_cr**	
[31:2]			RSVD	
[1]	rw	1'd0	con_to565	
[0]	rw	1'd0	con_to888	

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11 音频

11.1 PDM

HPSYS 有 2 个 PDM，支持最多 4 路麦克风输入。

11.1.1 简介

PDM (Pulse Density Modulation) 脉冲密度调制接口主要是用于将 PDM 麦克风采集到的 PDM 音频信号转化为 PCM（Pulse Code Modulation）脉冲编码调制信号以供后续的音频处理。

主要功能：

- 同时支持左右两路立体声信号，也可以单独采集单声道信号
- 可提供的 PDM 麦克风时钟速率：3.072MHz、1.536MHz、0.768MHz、1.024MHz、2.4MHz、1.6MHz、0.8MHz 等
- 支持 PCM 数据的速率：96kHz、48kHz、32kHz、24kHz、16kHz、12kHz、8kHz 等
- 支持 32bit、24bit、16bit、8bit 的 PCM 信号
- 支持分辨率为 0.5dB 并且从-15dB 到 45dB 增益可调

11.1.2 使用说明

PDM(脉冲密度调制) 模块旨在支持数字麦克风。

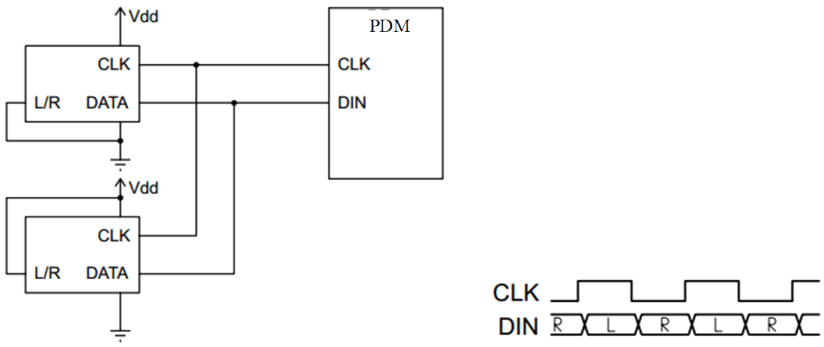


图 11-1: 数字麦克风通过 PDM 模块的典型连接

上图所示为一对数字麦克风通过 PDM 模块的典型连接，两个麦克风共用同一比特流时钟和数据线。借助麦克风的配置引脚 (L/R)，其中一个麦克风可在 CLK 上升沿提供有效数据，而另一个麦克风则在 CLK 下降沿提供有效数据。

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11.1.2.1 PDM 模块的整体结构

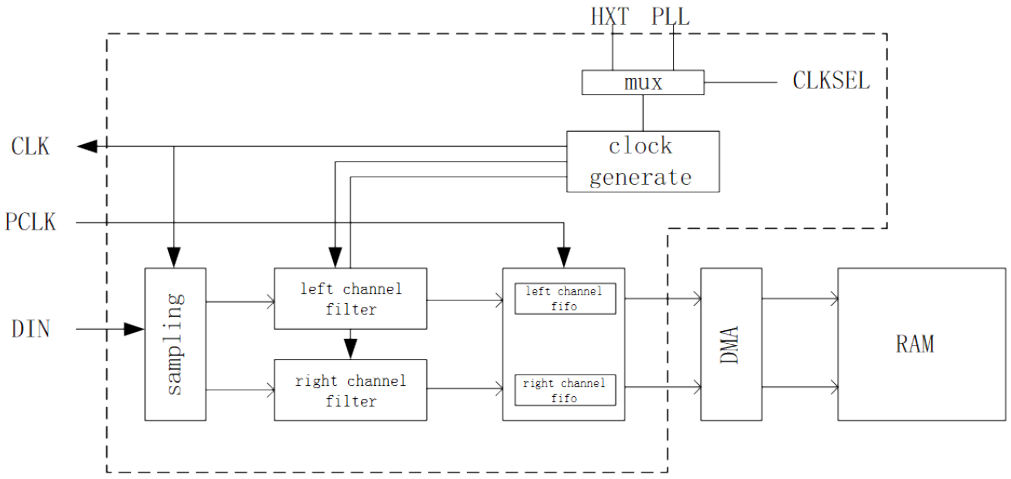


图 11-2: PDM 模块的整体结构

11.1.2.2 PDM 模块的时钟结构

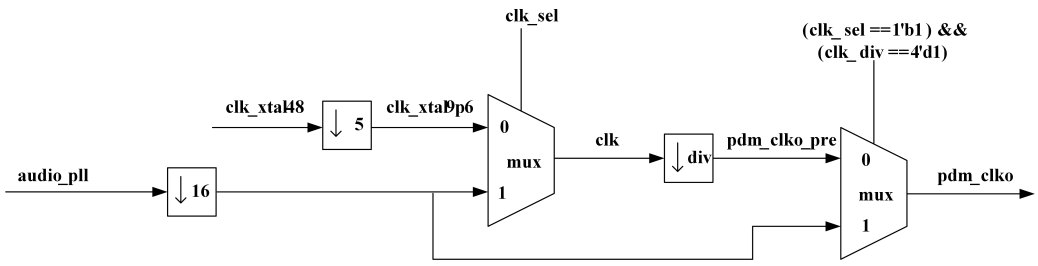


图 11-3: PDM 模块的时钟结构

PDM 模块的时钟源有两个，一个是系统的 48mHz 晶振，一个是系统的音频 PLL 经过 16 倍分频的时钟。而 48mHz 晶振在 PDM 模块内部先经过一个 5 倍的分频器得到一个 9.6mHz 的时钟，此时钟和音频 PLL 的时钟进行二选一，在经过可以配置的分频器得到最终送给数字麦克风的时钟 pdm_clko。pdm 模块最终的输出数据速率为 pdm_clko/(sinc_rate×lpf_downsample)。其中 sinc_rate 和 lpf_downsample 根据如下表格对寄存器 sinc_rate 以及 lpf_ds 进行配置得到最终的数据。

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表 11-1: PDM 麦克风时钟源以及对应输出数据速率的配置关系表

PDM_CLK(MHz)	Fs (PCM 输出 Rate, KHz)	SINCRATE(CIC 下采样率)	SINC ORDER	COMP_BYPASS	COMP_FILTER_SEL	HBF1_BYPASS	HBF1_GAIN_EN	HBF2_BYPASS	HBF2_GAIN_EN
3.072	96	16	4	0	1	0	1	1	0
3.072	48	16	4	0	1	0	1	0	1
3.072	32	24	4	0	1	0	1	0	0
3.072	16	96	3	0	0	0	1	1	0
3.072	8	96	3	0	0	0	1	0	0
1.536	48	16	4	0	1	0	1	1	0
1.536	32	24	4	0	1	0	1	1	0
1.536	16	24	4	0	1	0	1	0	0
1.536	8	96	3	0	0	0	1	1	0
1.536	16	48	3	0	0	0	1	1	0
2.4	48	25	4	0	1	0	0	1	0
2.4	16	75	3	0	0	0	1	1	0
2.4	8	75	3	0	0	0	1	0	0
1.6	32	25	4	0	1	0	0	1	0
1.6	16	25	4	0	1	0	0	0	0
1.6	8	100	3	0	0	0	0	1	0
1.6	16	50	3	0	0	0	1	1	0
2.8224	44.1	16	4	0	1	0	1	0	1

以表中第一行的配置为例对 PDM 模块的寄存器配置进行说明。输出时钟 3.072mHz，输出数据速率 48kHz。输出数据位宽 16 比特，双声道打开。

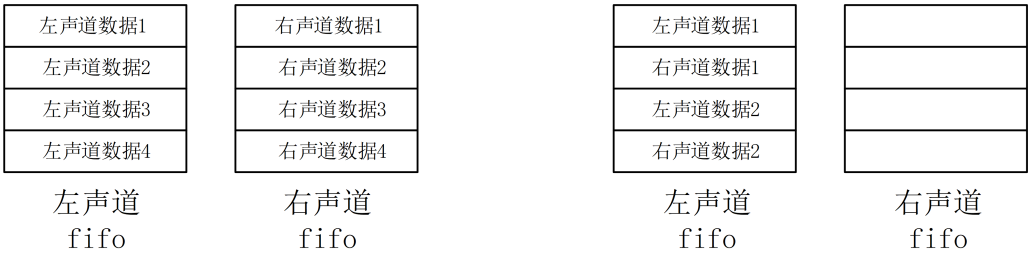
PDM 寄存器的配置流程：

1. 根据表格选择输出的速率。根据表中的 PDM_CLK 选择时钟源，配置 0x00 中 clk_sel 寄存器，0x0 表示 pdm 模块的输入时钟为 9.6mHz，0x1 表示 pdm 模块的输入时钟为音频 PLL 的十六分频时钟。此例 clk_sel 的配置为 1。（音频时钟的配置不在此处讨论）
2. 根据表格中 SINC RATE 以及 SINC ORDER 配置 0x08 中 sinc_rate 以及 sinc_order_sel 寄存器，其中 sinc_order_sel 为 1 对应表格中 SINC ORDER 为 4，0 对应 3。根据 LPF 后下采样率配置 0x34 中 lpf_ds 寄存器以及 lpf_bypass 寄存器，配置 lpf_ds 寄存器 1 表示对应 excel 中 lpf 下采样 4，配置 lpf_ds 寄存器 0 表示对应 excel 中 lpf 下采样 2，配置 lpf_bypass 为 1 对应表格中的 LPF BYPASS。此例 0x08 sinc_rate=64，sinc_order_sel=0，0x34 lpf_ds=0。
3. 根据声道配置打开对应的使能信号：

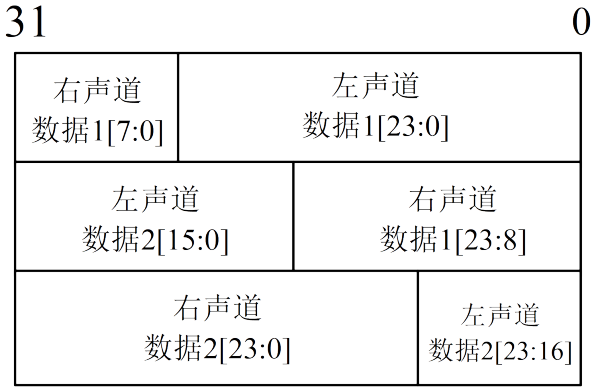
		双声道		左声道	右声道
寄存器 0x0 CFG0	left_en	1	0	1	0
	right_en	1	0	0	1
	stereo_en	0	1	0	0

   在 0x0 的 swap_en 寄存器为 0 时，pdm 模块认为的右声道采集的是 pdm mic 上升沿输出的数据，左声道采集的是 pdm mic 下降沿输出的数据；在 0x0 的 swap_en 寄存器为 1 时则正好相反，pdm 模块认为的右声道采集的时 pdm mic 下降沿输出的数据，左声道采集的时 pdm mic 上升沿输出的数据。根据需求进行配置。此例 0x0 stereo_en=1 left_en=0 rignt_en=0 或者 stereo_en=0 left_en=1 rignt_en=1。
4. 根据 pdm 模块的输出数据格式进行配置，输出数据的位宽不同对 0x38 的 byte_trunc 寄存器进行配置，配置 0 对应 24bits 输出，配置 1 对应 16bits 输出，配置 2 对应 8bits 输出，配置 3 对应 32bits 输出。此例 0x38 byte_trunc 为 1。
5. 根据左右声道数据是否需要混合到一起配置 0x38 的 byte_con 寄存器，配置 0 左右两个声道的数据各自存到各自的 fifo 中，配置 1 则左右两个声道的数据都存在左声道的 fifo 中。不同 byte_con 寄存器配置对应的输出数据的存储区别示意图。

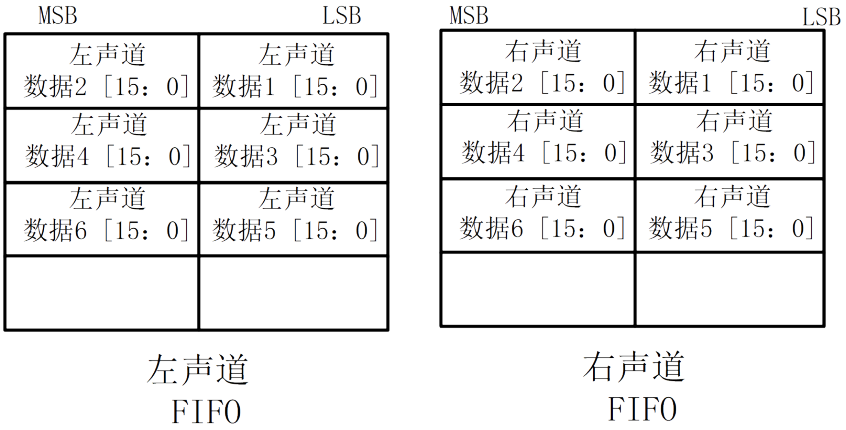
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不满 32 比特的数据会自动将下一个数据的低位补到上一个数据的高位凑成 32 比特数据，以 24 比特双声道数据，byte_con 为 1 为例如下图所示。



以 16 比特双声道数据，byte_con 为 0 为例如下图所示。



此例中对数据存储格式没有要求，请使用者根据需求自行选择配置。

6. 根据 dma 的使用说明配置 dma 的寄存器用去将 pdm fifo 中的数据一次一个 32 比特数据通过 dma 搬到指定的 ram 地址中。
7. 配置 0x0 中 pdmcoreen 寄存器使能 pdm 模块。

1~6 的顺序不固定，只要在 7 之前完成即可。

11.1.2.3 注意事项

PDM 模块产生的中断都是 fifo 出现溢出产生错误发出的中断。

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11.1.3 PDM 寄存器

PDM1 的基地址是 0x5009A000。

PDM2 的基地址是 0x5009B000。

表 11-2: PDM 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**CFG0**	
[31:10]			RSVD	
[9]	rw	1'b0	swap_en	1: Swap right channel and left channel pdm data; 0: Not swap right channel and left channel pdm data
[8]	rw	1'b0	stereo_en	1:Enable double channels pdm data sampling; 0: Disable double channels pdm data sampling
[7]	rw	1'b0	right_en	1: Enable right channel pdm data sampling; 0: Disable right channel pdm data sampling
[6]	rw	1'b0	left_en	1: Enable left channel pdm data sampling; 0: Disable left channel pdm data sampling
[5:2]	rw	4'h4	clk_div	Clock frequency division ratio of 3.072MHz or 9.6MHz according to register clk_sel
[1]	rw	1'b0	clk_sel	1:Clk select dll 3.072MHz; 0: Clk selct xtal 9.6MHz
[0]	rw	1'b0	pdmcoreen	1:Enable pdm module; 0: Disable pdm module
0x04			**CFG1**	
[31:11]			RSVD	
[10:8]	rw	3'h0	sample_dly_r	The number of delay dff before the right data stream in processing
[7:5]	rw	3'h0	sample_dly_l	The number of delay dff before the left data stream in processing
[4:0]			RSVD	
0x08			**SINC_CFG**	
[31:9]			RSVD	
[8]	rw	1'b1	sinc_order_sel	1:select four differentiators in sinc filter; 0:select three differentiators in sinc filter
[7:0]	rw	8'd32	sinc_rate	dowmsampling rate of sinc filter
0x14			**HPF_CFG**	
[31:6]			RSVD	
[5]	rw	1'b1	hpf_rst	1:high-pass filter normal operation ; 0:reset high-pass filter
[4]	rw	1'b0	hpf_bypass	1:bypass-high pass filter ; 0: enable high-pass filter
[3:0]	rw	4'hd	hpf_coeff	coefficient of high-pass filter
0x18			**PGA_CFG**	
[31:14]			RSVD	
[13:7]	rw	7'd0	pga_gain_r	right channel gain control , the range is -15dB~45dB. Resolution is 0.5dB/LSB
[6:0]	rw	7'd0	pga_gain_l	left channel gain control , the range is -15dB~45dB. Resolution is 0.5dB/LSB
0x34			**LPF_CFG6**	
[31:14]			RSVD	
[13]	rw	1'b0	lpf_bypass	1:bypass low-pass filter ; 0: enable low-pass filter
[12]	rw	1'b0	lpf_ds	1:downsampling rate of low pass filter is two;0:No downsampling of low pass filter
[11:0]			RSVD	
0x38			**FIFO_CFG**	
[31:9]			RSVD	
[8]	rw	1'b0	lr_chg	1:exchange storage location of left and right channel; 0: don't exchange storage location of left and right channel
[7]	rw	1'b0	rx_dma_msk_l	1:disable left channel dma request; 0: enable left channel dma request

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表 11-2: PDM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[6]	rw	1'b0	rx_dma_msk_r	1:disable right channel dma request; 0: enable right channel dma request
[5:3]	rw	3'h0	pdm_shift	the number of data left shift for higher data accuracy
[2:1]	rw	2'b0	byte_trunc	1: 16bits output ; 0: 24bits output ;2: 8bits output ; 3: 32bits output
[0]	rw	1'b0	byte_con	1: combine left channel and right channel; 0: not combine left channel and right channel
0x44			**FIFO_ST**	
[31:8]			RSVD	
[7]	r	1'h0	full_l	1 indicates left channel fifo is full
[6]	r	1'b0	empty_l	1 indicates left channel fifo is empty
[5]	r	1'b0	almost_full_l	1 indicates left channel fifo is less than two full
[4]	r	1'b0	almost_empty_l	1 indicates left channel fifo is less than two datas left
[3]	r	1'h0	full_r	1 indicates right channel fifo is full
[2]	r	1'b0	empty_r	1 indicates right channel fifo is empty
[1]	r	1'b0	almost_full_r	1 indicates right channel fifo is less than two full
[0]	r	1'b0	almost_empty_r	1 indicates right channel fifo is less than two datas left
0x48			**INT_ST**	
[31:2]			RSVD	
[1]	r	1'b0	overflow_l	1 indicates left channel fifo has already overflowed and as irq at same time
[0]	r	1'b0	overflow_r	1 indicates right channel fifo has already overflowed and as irq at same time
0x4c			**INT_MSK**	
[31:2]			RSVD	
[1]	rw	1'b0	int_mask_l	1:disable left channel irq to system; 0: enable left channel irq to system
[0]	rw	1'b0	int_mask_r	1:disable right channel irq to system; 0: enable right channel irq to system
0x50			**INT_CLR**	
[31:2]			RSVD	
[1]	w1c	1'b0	int_clr_l	clear left channel irq
[0]	w1c	1'b0	int_clr_r	clear right channel irq

11.2 I2S

HPSYS 有 2 个 I2S，支持主模式或从模式。

11.2.1 简介

I2S(也叫 IIS，即：Inter IC Sound) 总线, 又称集成电路内置音频总线，是飞利浦公司为数字音频设备之间的音频数据传输而制定的一种总线标准，该总线采用主/从模式，专责于音频设备之间的数据传输，广泛应用于各种多媒体系统。

目前 I2S 有 MSB 对齐（左对齐），LSB 对齐（右对齐）和 I2S 标准模式。

I2S 标准模式如下图所示：

数据在跟随 LRCLK 传输的 BCLK 的第二个上升沿时传输 MSB，其他位一直到 LSB 按顺序传。传输依赖于字长、BCLK 频率和采样率 (BCLK=Fs x 声道数 x 采样位数)，在每个采样的 LSB 和下一个采样的 MSB 之间都应该有未用的 BCLK 周期，LRCLK 为 0 传输左声道数据，LRCLK 为 1 传输右声道数据。

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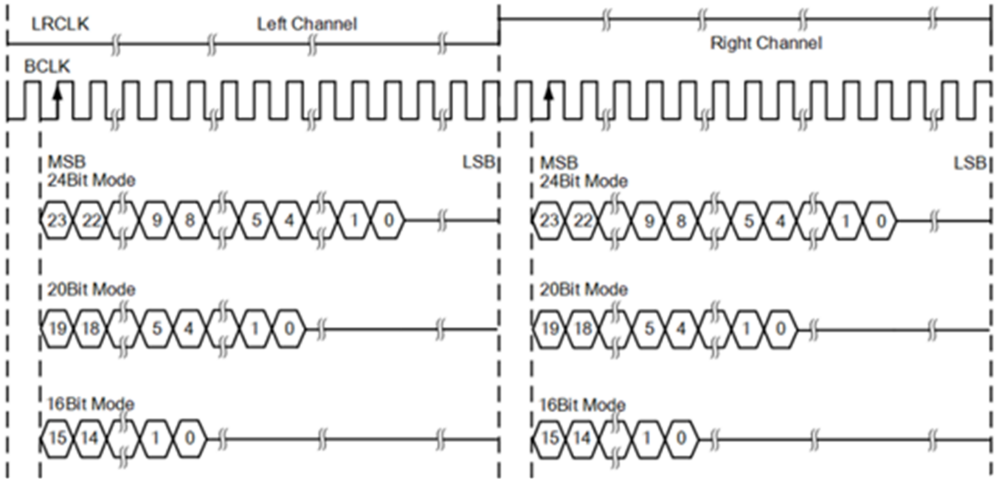


图 11-4: I2S 标准模式

I2S 左对齐如下图所示：

标准左对齐格式的数据的 MSB 没有相对于 BCLK 延迟一个时钟。左对齐格式的左右声道数据的 MSB 在 LRCLK 边沿变化后 BCLK 的第一个上升沿有效。LRCLK 为 1 传输左声道数据，LRCLK 为 0 传输右声道数据。

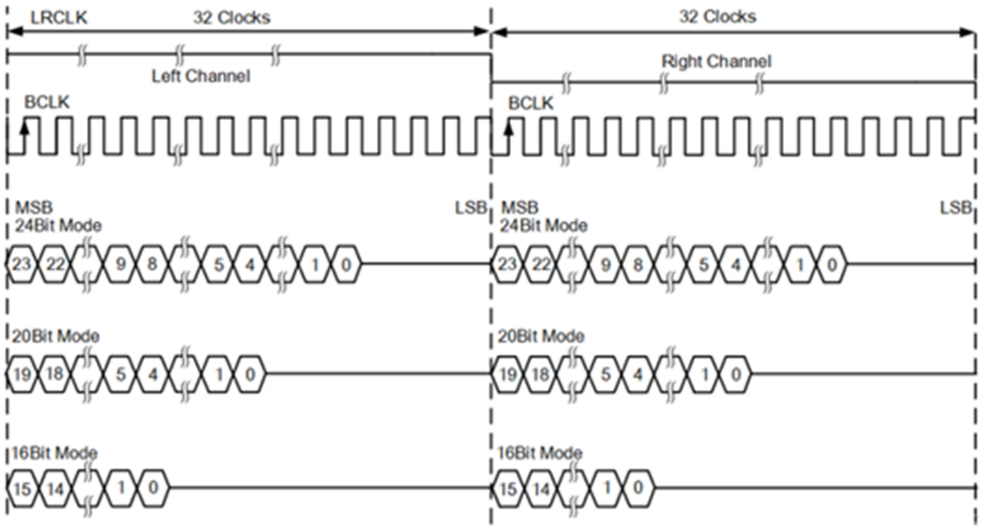


图 11-5: I2S 左对齐

I2S 右对齐如下图所示：

声音数据 LSB 传输完成的同时，LRCLK 完成第二次翻转，LRCLK 为 1 传输左声道数据，LRCLK 为 0 传输右声道数据。

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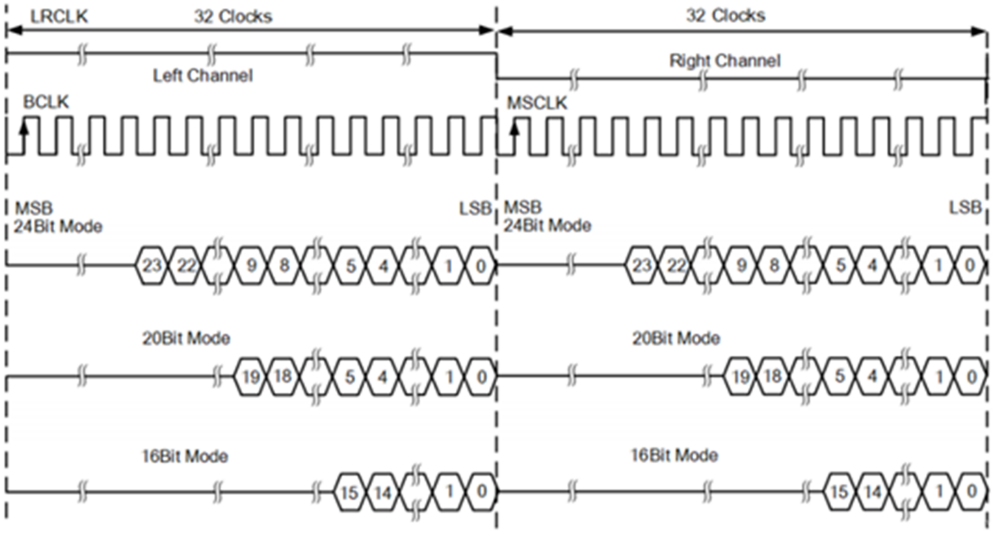


图 11-6: I2S 右对齐

11.2.2 I2S 功能描述

I2S 模块可以支持主从两种模式。主模式时，MCU 可以提供采样时钟 LRCK 和 bit 时钟 BCLK。从模式时，BCLK 和 LRCK 由外部提供，MCU 负责 I2S 的数据收发。

I2S 模块共支持左对齐和右对齐三种数据格式。在主模式下，用户可以根据需求定义 BCLK 和 LRCK 的比例关系。

当前版本的 I2S 模块还额外提供了 MCLK 的输出，MCLK 是与 BCLK 和 LRCK 同步的更高频率的时钟，可以提供给 I2S 外设更高的工作频率，用户也可以根据需求定义 MCLK 的频率。除此以外，I2S 时钟源增加了 PLL 的选项，这样提高了 I2S 时钟的灵活性。

11.2.3 I2S 寄存器

I2S1 的基地址是 0x50090000。

I2S2 的基地址是 0x5008a000。

表 11-3: I2S 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x10			**TX_PCM_FORMAT**	
[31:6]			RSVD	
[5]	rw	1'h0	track_flag	0: stereo 1: mono

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表 11-3: I2S 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[4:0]	rw	5'h10	dw	tx source pcm data width N(N>=8) common value is 8,13,14,16,18,20,22,24 This data width indicate the tx fifo output data width. When writing to tx fifo, please refer to following format: Mono 8 bit: fifo_data[31:0] = L3,L2,L1,L0, each word contains 4 samples, so four samples need read one word Stereo 8 bit: fifo_data[31:0] = R1,L1,R0,L0 , each word contains 2 samples, so two samples need read one word Mono 13/14/16 bit: fifo_data[31:0] = L1,L0, each word contains 2 samples, so two samples need read one word Stereo 13/14/16 bit: fifo_data[31:0] = R0,L0, each word contains 1 samples, so each sample need read one word Mono 18/20/22/24 bit: fifo_data[31:0] = L0, each word contains 1 samples, so each sample need read one word Stereo 18/20/22/24 bit: fifo_data[31:0][0] = L0, fifo_data[31:0][1]=R0, each 2 words contain 1 samples, so each sample need read two word
0x20			**TX_PCM_SAMPLE_CLK**	
[31:13]			RSVD	
[12:0]	rw	13'd250	fs_duty	source PCM sample clock duty cycle(with GCLK=12MHz): 250 for 48K FS 272 for 44.1K FS 375 for 32K FS 500 for 24K FS 544 for 22.05K FS 750 for 16K FS 1000 for 12K FS 1088 for 11.025K FS 1500 for 8K FS
0x30			**TX_RS_SMOOTH**	
[31:1]			RSVD	
[0]	rw	1'h0	en	0: Disable TX re-sample smooth filter 1: Enable TX re-sample smooth filter This function is not implemented.
0x40			**TX_PCM_CH_SEL**	
[31:4]			RSVD	
[3:2]	rw	2'h0	left_channel_sel	TX re-sampling module setting: 00: TX left = source left 01: TX left = source right 10,11: TX left = (source left + source right)/2
[1:0]	rw	2'h0	right_channel_sel	TX re-sampling module setting: 00: TX right = source right 01: TX right = source left 10,11: TX right = (source left + source right)/2
0x50			**TX_VOL_CTRL**	
[31:4]			RSVD	

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表 11-3: I2S 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[3:0]	rw	4'hf	vol	volume control: 0000: +6dB, 0001: +4.5dB, 0010: +3dB, 0011: +1.5dB, 0100: 0dB, 0101: -1.5dB, 0110: -3.0dB, 0111: -4.5dB, 1000: -6.0dB, 1001: -7.5dB, 1010: -9dB, 1011: -10.5dB, 1100: -12dB, 1101: -13.5dB, 1110: -15dB, 1111: mute Note: 1) +1.5db = 20log(1+1/4-1/16+1/1024) 2) -1.5dB = 20log(1-1/8-1/32-1/512-1/2048)
0x60			**TX_LR_BAL_CTRL**	
[31:6]			RSVD	
[5:4]	rw	2'h0	en	LR balance enable: 00: both left and right in full volume 10: left channel balance volume adjustment enable 01: right channel balance volume adjustment enable 11: reserved, still kepp left and right in full volume
[3:0]	rw	4'h0	bal_vol	Balance volume control: 0000: Reserved, 0001: -1.5dB, 0010: -3.0dB, 0011: -4.5dB, 0100: -6.0dB, 0101: -7.5dB, 0110: -9.0dB, 0111: -10.5dB, 1000: -12dB, 1001: -13.5dB, 1010: -15dB, 1011: -16.5dB, 1100: -18dB, 1101: -19.5dB, 1110: -21dB, 1111: mute Note: 1) bit[5:0] = 101111 for left mute 2) bit[5:0] = 011111 for right mute 3) bit[5:4] = 00 or 11, bit[3:0] is don't care 4) +1.5db = 20log(1+1/4-1/16+1/1024) 5) -1.5dB = 20log(1-1/8-1/32-1/512-1/2048)
0x70			**AUDIO_TX_LRCK_DIV**	
[31:28]			RSVD	
[27:16]	rw	12'd125	duty_high	TX LRCK duty cycle high: 125 for 48K FS 136 for 44.1K FS 185 for 32K FS 250 for 24K FS 272 for 22.05K FS 375 for 16K FS 500 for 12K FS 544 for 11.025K FS 750 for 8K FS
[15:12]			RSVD	

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表 11-3: I2S 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[11:0]	rw	12'd125	duty_low	TX LRCK duty cycle low: 125 for 48K FS 136 for 44.1K FS 190 for 32K FS 250 for 24K FS 272 for 22.05K FS 375 for 16K FS 500 for 12K FS 544 for 11.025K FS 750 for 8K FS Note: 1)duty_cycle = 12M/FS
0x80			**AUDIO_TX_BCLK_DIV**	
[31:6]			RSVD	
[5:0]	rw	6'h5	duty	TX serial bit clock duty cycle 5 for 48K FS 4 for 44.1K FS 5 for 32KFS 10 for 24K FS 8 for 22.05K FS 15 for 16K FS 20 for 12K FS 16 for 11.025K FS 30 for 8KFs
0x90			**AUDIO_TX_FORMAT**	
[31:5]			RSVD	
[4:0]	rw	5'h10	pcm_data_width	I2S out pcm data width M >= 16, common value: 16, 18, 20, 22, 24
0xa0			**AUDIO_SERIAL_TIMING**	
[31:4]			RSVD	
[3]	rw	1'h0	lrck_pol	TX LRCK polarity control. 0: disable TX_LRCK inventor 1: enable TX_LRCK inventor for standard I2S, set tx_lrck_pol to low for Left/Right Justified, set tx_lrck_pol to hgih
[2]	rw	1'h0	slave_en	audio code transmit mode select. 0: master mode, 1: slave mode
[1:0]	rw	2'h0	timing	00: I2S mode 01: Left justified 10: right justified 11: reserved
0xb0			**AUDIO_TX_FUNC_EN**	
[31:2]			RSVD	
[1]	rw	1'h0	tx_intf_sel	1: select external tx interface 0: select internal apb tx interface
[0]	rw	1'h0	tx_en	1: enable 0:disable
0xc0			**AUDIO_TX_PAUSE**	
[31:1]			RSVD	

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表 11-3: I2S 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[0]	rw	1'h0	tx_pause	TX pause control when tx_enable = 1. 1: pause 0: TX work
0xc8			**AUDIO_I2S_SL_MERGE**	
[31:1]			RSVD	
[0]	rw	1'h0	slave_timing_merge	when work as an I2S slave, and external I2S master TX/RX share an only BCLK/LRCK, we need set this bit high. 0: I2S slave use separated timing control port. TX_BCLK_IN/TX_LRCK_IN and RX_BCLK/RX_LRCK_IN are separated. 1: I2S slave use the same BCLK/LRCK, the TX_BCLK_IN/TX_LRCK also is used for RX controller.
0x100			**AUDIO_RX_FUNC_EN**	
[31:2]			RSVD	
[1]	rw	1'h0	rx_intf_sel	1: select external rx interface 0: select internal apb rx interface
[0]	rw	1'h0	rx_en	1: enable 0: disable
0x110			**AUDIO_RX_PAUSE**	
[31:1]			RSVD	
[0]	rw	1'h0	rx_pause	RX pause control when rx_enable = 1. 1: pause 0: RX work
0x120			**AUDIO_RX_SERIAL_TIMING**	
[31:4]			RSVD	
[3]	rw	1'h0	lrck_pol	RX LRCK polarity control. 0: disable RX_LRCK inventor 1: enable RX_LRCK inventor for standard I2S, set tx_lrck_pol to low for Left/Right Justified, set tx_lrck_pol to hgih
[2]	rw	1'h0	slave_en	audio code receiver mode select. 0: master mode, 1: slave mode
[1:0]	rw	2'h0	timing	00: I2S 01: Left justified 10: right justified 11: reserved
0x130			**AUDIO_RX_PCM_DW**	
[31:5]			RSVD	
[4:0]	rw	5'h10	pcm_data_width	For I2S and left justified mode, M can be 8,13,14,16 For right justified mode, M can be 8, 13, 14, 16, 18, 20, 22, 24
0x140			**AUDIO_RX_LRCK_DIV**	
[31:28]			RSVD	

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表 11-3: I2S 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[27:16]	rw	12'd125	duty_high	RX LRCK duty cycle high: 125 for 48K FS 136 for 44.1K FS 185 for 32K FS 250 for 24K FS 272 for 22.05K FS 375 for 16K FS 500 for 12K FS 544 for 11.025K FS 750 for 8K FS
[15:12]			RSVD	
[11:0]	rw	12'd125	duty_low	RX LRCK duty cycle low: 125 for 48K FS 136 for 44.1K FS 190 for 32K FS 250 for 24K FS 272 for 22.05K FS 375 for 16K FS 500 for 12K FS 544 for 11.025K FS 750 for 8K FS Note: 1)duty_cycle = 12M/FS
0x150			**AUDIO_RX_BCLK_DIV**	
[31:10]			RSVD	
[9:0]	rw	10'h5	duty	RX serial bit clock duty cycle 5 for 48K FS 4 for 44.1K FS 5 for 32KFS 10 for 24K FS 8 for 22.05K FS 15 for 16K FS 20 for 12K FS 16 for 11.025K FS 30 for 8KFs
0x160			**RECORD_DATA_SEL**	
[31:1]			RSVD	
[0]	rw	1'h0	rs_data_sel	0: I2S audio recording 1: BT recording
0x170			**RX_RE_SAMPLE_CLK_DIV**	
[31:13]			RSVD	

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表 11-3: I2S 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[12:0]	rw	13'd250	rs_duty	source PCM sample clock duty cycle: 250 for 48K FS 272 for 44.1K FS 375 for 32K FS 500 for 24K FS 544 for 22.05K FS 750 for 16K FS 1000 for 12K FS 1088 for 11.025K FS 1500 for 8K FS Note: 1)duty_cycle = 12M/FS
0x180			**RX_RE_SAMPLE**	
[31:1]			RSVD	
[0]	rw	1'h0	smooth_en	0: Disable RX re-sample smooth filter 1: Enable RX re-sample smooth filter
0x190			**RECORD_FORMAT**	
[31:2]			RSVD	
[1]	rw	1'h0	track	1: mono recording, 0: stereo recording
[0]	rw	1'h0	dw	0: 8bit 1: 16bit RX fifo data format: Mono 8 bit (unsigned): RX FIFO_DIN[31:0] = L3,L2,L1,L0, each four samples need one FIFO write operation Stereo 8 bit (unsigned): RX_FIFO_DIN[31:0] = R1,L1,R0,L0, each tow samples need one FIFO write operation Mono 16 bit (Signed 2's complement): RX_FIFO_DIN[31:0] = L1,L0, each two samples need one FIFO write operation Stereo 16 bit (Signed 2's complement): RX_FIFO_DIN[31:0] = R0,L0, each sample need one FIFO write operation
0x1a0			**RX_CH_SEL**	
[31:4]			RSVD	
[3:2]	rw	2'h0	left_channel_sel	RX re-sampling module setting: 00: RD left = RX left 01: RD left = RX right 10,11: RD left = (RX left + RX right)/2
[1:0]	rw	2'h0	right_channel_sel	RX re-sampling module setting: 00: RD right = RX right 01: RD right = RX left 10,11: RD right = (RX left + RX right)/2
0x200			**BT_PHONE_CTRL**	
[31:6]			RSVD	
[5]	rw	1'h0	bb_i2s_bps_to_cdc	bypass baseband I2S interface to audio codec i2s interface 0: no bypass, 1: bypass
[4]	rw	1'h0	bt_pcm_if_bps	bypass baseband PCM signals to BT VCI master: 0: no bypass, 1: bypass
[3]	rw	1'h0	bt_path_sel	BT path select 0: digital path, 1: analog path
[2]	rw	1'h0	bt_mix_smooth_filter_en	0: disable the smooth filter for background mixer 1: enable the smooth filer for background mixer

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表 11-3: I2S 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	rw	1'h0	bt_back_mix_en	background mixer enable 0: disable, 1: enable
[0]	rw	1'h0	bt_ph_en	BT phone enable 0: disable, 1: enable
0x210			**BB_PCM_FORMAT**	
[31:11]			RSVD	
[10]	rw	1'h0	pcm_clk_pol	input BB pcm clock polarity: 0: rising edge for data transmitting, falling edge for data receiving 1: rising edge for data receiving, falling edge for data transmitting
[9]	rw	1'h0	i2s_lrck_pol	0: no bb_i2s_lrck input inventor 1: enable bb_i2s_lrck input inventor for standard I2S, set tx_lrck_pol to low for Left/Right Justified, set tx_lrck_pol to high
[8]	rw	1'h0	pcm_lsb_flag	Serial PCM data bit sequence. 0: MSB first, 1: LSB first
[7]	rw	1'h0	pcm_sync_flag	0: short sync, 1: long sync
[6:5]	rw	2'h0	pcm_tim_sel	00: I2S timing, 01: Left Justified 10: Right Justified, 11: PCM timing
[4:0]	rw	5'h8	pcm_dw	Baseband Master PCM data width (>=8) Common value: 8, 13,14, 16, 18, 20, 22, 24. for I2S/Left Justified/Right Kistified timing, bb_pcm_dw >=16 For PCM timing, only 8, 13, 14, 16 configure value is available.
0x220			**BT_PCM_DW**	
[31:5]			RSVD	
[4:0]	rw	5'h10	dw	BT PCM master data width (>= 8), common value: 8, 13,14, 16
0x230			**BT_PCM_TIMING**	
[31:3]			RSVD	
[2]	rw	1'h0	clk_pol	BT PCM master output pcm clock polarity: 0: rising edge for data transmitting, falling edge for data receiving 1: rising edge for data receiving, falling edge for data transmitting
[1]	rw	1'h0	sync_flag	0: short sync, 1: long sync
[0]	rw	1'h0	lsb_flag	Serial PCM data bit sequence. 0: MSB first, 1: LSB first
0x240			**BT_PCM_CLK_DUTY**	
[31:10]			RSVD	
[9:0]	rw	10'h0	clk_duty	BT_PCM_CLK duty cycle <= (GCLK/(bt_pcm_sync*bt_pcm_dw))
0x250			**BT_PCM_SYNC_DUTY**	
[31:6]			RSVD	
[5:0]	rw	6'h0	sync_duty	PCM_SYNC duty cycle (bt_pcm_sync frequency = bt_pclk_clk/bt_pcm_sync_duty)
0x260			**BT_VOL_CTRL**	
[31:4]			RSVD	
[3]	rw	1'h0	vol_adj_en	BT volume adjust enable
[2:0]	rw	3'h0	vol	BT master volume
0x300			**INT_MASK**	
[31:2]			RSVD	

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表 11-3: I2S 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	rw	1'h1	tx_fifo_int_mask	Interrupt mask for TX FIFO pop underflow, high active
[0]	rw	1'h1	rx_fifo_int_mask	Interrupt mask for RX FIFO push overflow, high active
0x310			**INT_STATUS**	
[31:2]			RSVD	
[1]	rw	1'h0	tx_fifo_underflow	TX FIFO pop underflow
[0]	rw	1'h0	rx_fifo_overflow	RX FIFO push overflow
0x400			**TX_DMA_ENTRY**	
[31:0]	w	32'h0	tx_dma_entry	TX DMA entry
0x440			**RX_DMA_ENTRY**	
[31:0]	r	32'h0	rx_dma_entry	RX DMA entry
0x480			**DMA_MASK**	
[31:2]			RSVD	
[1]	rw	1'h1	tx_dma_mask	TX DMA mask enable:1: mask0: do not mask
[0]	rw	1'h1	rx_dma_mask	RX DMA mask enable:1: mask0: do not mask
0x500			**DEBUG_LOOP**	
[31:24]			RSVD	
[23:16]	rw	8'h2	sp_clk_div	sp clock divider value
[15:9]			RSVD	
[8]	w1c	1'h0	sp_clk_div_update	update sp clock divider
[7:3]			RSVD	
[2]	rw	1'h0	sp_clk_sel	clock select 0: xtal clock 1: pll clock
[1]	rw	1'h0	ad2da_loop_back	RX–>TX Loop debug control: 0: disable 1: enable, internally connect RX Resampled PCM to TX Resample PCM input
[0]	rw	1'h0	da2ad_loop_back	TX–>RX Loop debug control: 0: disable 1: enable, internally connect TX SDTO to RX SDTI
0x600			**FIFO_STATUS**	
[31:8]			RSVD	
[7:0]	rw	8'h0	fifo_status_out	FIFO Status output: Bit [7:0] = tx_full,tx_empty,tx_almost_full,tx_almost_empty, rx_full,rx_empty,rx_almost_full,rx_almost_empty
0x700			**TX_EQUALIZER_EN**	
[31:1]			RSVD	
[0]	rw	1'h0	tx_equalizer_en	0: Disable TX equalizer 1: Enable TX equalizer equalizer is not implemented
0x710			**TX_EQUALIZER_GAIN1**	
[31:30]			RSVD	
[29:25]	rw	5'h0	band6_gain	
[24:20]	rw	5'h0	band5_gain	
[19:15]	rw	5'h0	band4_gain	
[14:10]	rw	5'h0	band3_gain	
[9:5]	rw	5'h0	band2_gain	
[4:0]	rw	5'h0	band1_gain	

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表 11-3: I2S 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x720			TX_EQUALIZER_GAIN2	
[31:20]			RSVD	
[19:15]	rw	5'h0	band10_gain	
[14:10]	rw	5'h0	band9_gain	
[9:5]	rw	5'h0	band8_gain	
[4:0]	rw	5'h0	band7_gain	

11.3 Audprc

11.3.1 简介

Audprc 模块全称 Audio Process Controller，其主要功能是对采集和播放音频数据进行处理后，并将处理后的数据送到指定的模块。Audprc 内对音频的处理功能有增益调节，混音，均衡调节，采样率转换，用户可以根据需要对这些功能进行单独配置。

11.3.2 系统架构

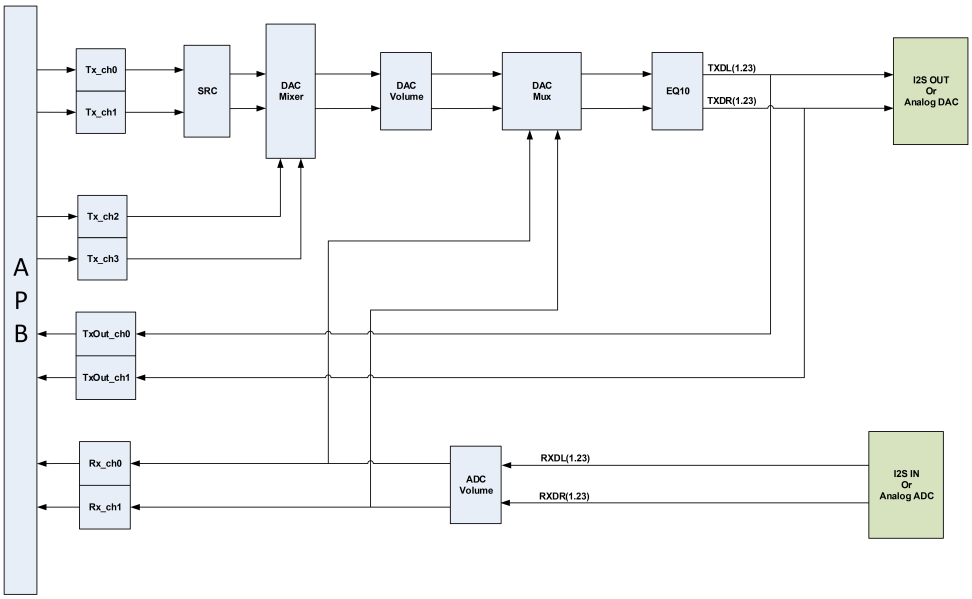


图 11-7: Audprc 结构图

Audprc 主要由两部分通路组成，输出的 TX 通路和接受的 RX 通路。TX 通路将数据从内存空间送至 I2S 输出端或者模拟的 DAC。RX 通路则从 I2S 输入端或者模拟的 ADC 接受数据，并存储到内存空间。

11.3.3 功能描述

11.3.3.1 采样率转换模块

采样率转换模块 SRC 可以根据需求改变音频数据的采样率，转换的范围是 1/16~16。采样率转换模块由多级 Half-band 滤波器和 Sinc 滤波器组成，用户需要根据输入输出的采样率，对采样率转换模块的参数进行配置，达

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到需要的转换比例。

采样率转换模块内部共有三级 Half-band 滤波器，以及一级 Sinc 滤波器。每一级 Half-band 滤波器可以实现 2 倍的上采样或者下采样，Sinc 滤波器可以实现 0.5~2 以内的高精度采样率转换。总的采样率转换比例：

Ratio = Ratio(hb1) * Ratio(hb2) * Ratio(hb3) * Ratio(sinc)

三级 Half-band 滤波器结构相同，配置方法也相同。如果需要实现 2 倍上采样，则配置 Hbf enable 为 1，同时 mode 设置为 0。如果需要实现 2 倍下采样，则配置 Hbf enable 为 1，同时 mode 设置为 0。默认情况下 Hbf 的 enable 为 0，表示该级 Half-band 滤波器不工作，不会改变采样率。三级 Half-band 滤波器的配置，要尽可能逼近最终的目标采样率转换比例。

最后一级 Sinc 滤波器有两个配置参数，是能 enable 和采样率转换比例 Sinc_ratio。Sinc_ratio 为 31bit 定点无符号数，包含 1 位整数位和 30 位小数位，对应的精度为 $1/2^{30}$。

以下将以 16KHz 转 44.1KHz 为例，对 SRC 进行配置。

16KHz 转 44.1KHz 有两种比较简单的方式：

- 方案一：16KHz->32KHz->44.1KHz
- 方案二：16KHz->32KHz->64KHz->44.1KHz

这两种情况理论上都可以，方案一中，采用一级 Half-band 滤波器进行 2 倍上采样，然后使用 Sinc 滤波器 Ratio 为 1.378 倍。方案二中，采样两级 Half-band 滤波器进行共 4 倍上采样，然后 Sinc 滤波器 Ratio 为 0.689 倍。两种方案相比较，方案二中 Sinc 滤波器的 Ratio 更接近 1，滤波器性能上会更好一些，所以选择方案二。

11.3.3.2 混音模块

混音模块 (DAC Mixer,DAC Mux) 是在 DAC 通路上，将不同源头的音频源混合在一起。

DAC Mixer 的输入是四路 TX 数据，四路音频经过重新组合，变成两路音频输出。输出的每一路都由两路音频数据相加而得，这两路音频数据可以来自与 TX 的四路数据，也可以选择静音。具体可以参考寄存器 mixlsrc0，mixlsrc1，mixrsrc0，mixrsrc1。

DAC Mux 的输入是 DAC 的两路数据，和 ADC 的两路数据。Mux 的混音方式与 Mixer 相同，也是将四路输入混合成两路输出，每一路的音频源可以任意配置。具体可以参考寄存器 muxlsrc0，muxlsrc1，muxrsrc0，muxrsrc1。

11.3.3.3 增益调节模块

DAC 和 ADC 通路由独立的增益调节模块 Volume，左右两路音频调节各自独立。范围是-18~13dB，步进是 0.5dB。

11.3.3.4 均衡器模块

均衡器模块 EQ 最多支持 10 级独立调节，用户需要配置 eq_stage 来使能需要的级数。每一级有 5 个参数，共 50 个参数可以配置。用户可以使用工具产生想要的均衡器效果，然后将参数配置入 Audprc。均衡器在使用前需要先使能 eq_clr，等到 eq_clr_done 为 1 后，清除 eq_clr 即可，这一步骤是为了清除内部临时数据残留。如果不进行清除，均衡器模块收敛时间会长一点，且有可能开启时会有瞬时噪声。

11.3.4 配置流程

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11.3.4.1 配置 Tx 和 Rx 通道

Audprc 的 Tx 通道可以支持单声道 16bit/24bit 和立体声 16bit 的音频数据格式，最多支持 4 路音频（立体声占用两路）。每个 Tx 通道可以通过配置 format 寄存器，支持单路 16bit/24bit 的音频。对于立体声 16bit 的音频源 (每 32bit 数据包含左右声道各 16bit 的数据)，仅有 Tx 通道 0 和通道 2 可以支持，可以通过 Mode 寄存器进行模式配置。当 Tx 通道 0 配置为立体声 16bit 模式时，Tx 通道 1 就会被占用，无法再使用。同样当 Tx 通道 2 配置为立体声 16bit 模式时，Tx 通道 3 也会被占用，无法再使用。

Audprc 的 Rx 通道可以支持单声道 16bit/24bit 的音频数据格式，最多支持 2 路音频。每个 Rx 通道可以通过配置 format 寄存器，支持单路 16bit/24bit 的音频。

配置完 Tx 和 Rx 的音频数据结构之后，还需要配置对应的 DMA，对 Tx 和 Rx 通道数据收发处理。

11.3.4.2 配置 DAC 通路

DAC 通路配置包含前文提到的各个模块，如 SRC，EQ，Mixer，Mux，Volume。需要注意的是，SRC 和 EQ 均支持输入端两个通道单独使能，配置是只需要使能有音频数据的输入通道即可。另外在配置 Mux 的时候，如果选择 Rx 通道的数据与 Tx 通道的数据混合，需要保证两者的采样率相同，否则会出现混音不同步的问题。

配置完成 DAC 内部模块后，可以通过寄存器 dst_sel 配置 DAC 的输出目标模块。如果 dst_sel 为 0，则 DAC 数据会被送到 Codec 模块，该通路最高支持 24bit 立体声，经过 Codec 模块后，音频数据会被转化成音频模拟信号输出。如果 dst_sel 为 1，则 DAC 数据会被送到 I2S 模块，该通路最高支持 16bit 立体声，数据最后会通过数字 I2S 接口输出。如果 dst_sel 为 2，则 DAC 数据会被送至 Audprc Tx_out 通道，该通道最高支持 24bit 立体声，用户可以配置 DMA 将数据从 Tx_out 通道读取并存储到内存空间。

除此以外，DAC 通路还需要配置采样时钟源和采样分频比。时钟源可以选择芯片内置的音频 PLL 或者 48MHz 晶振，这里需要保证 DAC 通路使用的时钟源与输出目标模块一致，且经过分频后的时钟与输出模块的采样率一致。如果输出模块为 Tx_out 通道，则没有该要求。

11.3.4.3 配置 ADC 通路

ADC 通路配置一个 Volume 模块。配置完 Volume 后可以通过寄存器 src_sel 配置 ADC 的音频源。如果 src_sel 为 0，则 ADC 数据来源为 Codec 模块，该通路最高支持 24bit 立体声，Codec 数据来源于 ADC 采集的外部音频模拟信号。如果 src_sel 为 1，则 ADC 数据来源为 I2S 模块，该通路最高支持 16bit 立体声，音频数据来源于外部 I2S 数字接口。

与 DAC 通路一样，ADC 通路需要配置采样时钟源和分频比，时钟源需要与音频源一致，经过分频后的时钟需要与音频采样率一致。

当 ADC 数据通过 Mux 送到 DAC 通路时，ADC 数据到 Rx 通道的通路不会受到影响，用户可以同时从使能 Rx 通道采集 ADC 的数据。

11.3.5 Audprc 寄存器

Audprc 的基地址是 0x50087000。

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表 11-4: Audprc 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**id**	
[31:0]	rw	32'hA0000	rev	revision id
0x04			**cfg**	
[31:21]			RSVD	
[20]	w1c	1'h0	audclk_div_update	audprc clock divider update, write 1 to update
[19:16]	rw	4'h2	audclk_div	audprc clock divider, 0 and 1 means divide by 1
[15:10]			RSVD	
[9]	rw	1'h0	stb_clk_sel	audio strobe clock select 0: use xtal clock to generate strobe 1: use pll clock to generate strobe
[8]	rw	1'h0	auto_gate_en	auto clock gating enable, high active
[7]	rw	1'h0	adc_path_en	adc path enable
[6]	rw	1'h0	dac_path_en	dac path enable
[5]	rw	1'h0	adc_path_sreset	adc path software reset, high active
[4]	rw	1'h0	dac_path_sreset	dac path software reset, high active
[3]	rw	1'h0	adc_path_flush	adc path fifo flush, high active
[2]	rw	1'h0	dac_path_flush	dac path fifo flush, high active
[1]	rw	1'h0	sreset	audprc software reset, high active
[0]	rw	1'h0	enable	audprc enable
0x08			**stb**	
[31:16]	rw	16'h1	adc_div	adc strobe divider
[15:0]	rw	16'h1	dac_div	dac strobe divider
0x0C			**irq**	
[31:26]			RSVD	
[25]	rw	1'h0	tx_out1_fifo_uf_mask	tx_out channel 1 fifo underflow mask, 0: mask the interrupt
[24]	rw	1'h0	tx_out0_fifo_uf_mask	tx_out channel 0 fifo underflow mask, 0: mask the interrupt
[23]	rw	1'h0	rx_in_fifo_of_mask	rx input fifo overflow mask, 0: mask the interrupt
[22]	rw	1'h0	tx_out_fifo_uf_mask	tx output fifo underflow mask, 0: mask the interrupt
[21]	rw	1'h0	rx1_fifo_uf_mask	rx channel 1 fifo underflow mask, 0: mask the interrupt
[20]	rw	1'h0	rx0_fifo_uf_mask	rx channel 0 fifo underflow mask, 0: mask the interrupt
[19]	rw	1'h0	tx3_fifo_of_mask	tx channel 3 fifo overflow mask, 0: mask the interrupt
[18]	rw	1'h0	tx2_fifo_of_mask	tx channel 2 fifo overflow mask, 0: mask the interrupt
[17]	rw	1'h0	tx1_fifo_of_mask	tx channel 1 fifo overflow mask, 0: mask the interrupt
[16]	rw	1'h0	tx0_fifo_of_mask	tx channel 0 fifo overflow mask, 0: mask the interrupt
[15:10]			RSVD	
[9]	rw1c	1'h0	tx_out1_fifo_uf	tx_out channel 1 fifo underflow, write 1 to clear
[8]	rw1c	1'h0	tx_out0_fifo_uf	tx_out channel 0 fifo underflow, write 1 to clear
[7]	rw1c	1'h0	rx_in_fifo_of	rx input fifo overflow, write 1 to clear
[6]	rw1c	1'h0	tx_out_fifo_uf	tx output fifo underflow, write 1 to clear
[5]	rw1c	1'h0	rx1_fifo_uf	rx channel 1 fifo underflow, write 1 to clear
[4]	rw1c	1'h0	rx0_fifo_uf	rx channel 0 fifo underflow, write 1 to clear
[3]	rw1c	1'h0	tx3_fifo_of	tx channel 3 fifo overflow, write 1 to clear
[2]	rw1c	1'h0	tx2_fifo_of	tx channel 2 fifo overflow, write 1 to clear
[1]	rw1c	1'h0	tx1_fifo_of	tx channel 1 fifo overflow, write 1 to clear
[0]	rw1c	1'h0	tx0_fifo_of	tx channel 0 fifo overflow, write 1 to clear
0x10			**tx_ch0_cfg**	
[31:8]			RSVD	
[7:4]	r	4'h0	fifo_cnt	tx fifo counter

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表 11-4: Audprc 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[3]	rw	1'h0	dma_msk	1: mask the dma request for tx ch0
[2]	rw	1'h0	mode	tx mode 1'h0: mono mode 1'h1: stereo mode This bit is only used for 16-bit mode, in 24-bit mode, channel can only be set in mono mode. In 16-bit stereo mode, tx channel 1 is not working, both left and right audio data comes from channel 0.
[1]	rw	1'h0	format	tx format 0: 16-bit mode 1: 24-bit mode
[0]	rw	1'h0	enable	tx channel 0 enable
0x14			**tx_ch0_entry**	
[31:0]	rw	32'h0	data	tx channel 0 data entry
0x18			**tx_ch1_cfg**	
[31:8]			RSVD	
[7:4]	r	4'h0	fifo_cnt	tx fifo counter
[3]	rw	1'h0	dma_msk	1: mask the dma request for tx ch1
[2]			RSVD	
[1]	rw	1'h0	format	tx format 0: 16-bit mode 1: 24-bit mode
[0]	rw	1'h0	enable	tx channel 0 enable
0x1C			**tx_ch1_entry**	
[31:0]	rw	32'h0	data	tx channel 1 data entry
0x20			**tx_ch2_cfg**	
[31:8]			RSVD	
[7:4]	r	4'h0	fifo_cnt	tx fifo counter
[3]	rw	1'h0	dma_msk	1: mask the dma request for tx ch2
[2]	rw	1'h0	mode	tx mode 1'h0: mono mode 1'h1: stereo mode This bit is only used for 16-bit mode, in 24-bit mode, channel can only be set in mono mode. In 16-bit stereo mode, tx channel 3 is not working, both left and right audio data comes from channel 2.
[1]	rw	1'h0	format	tx format 0: 16-bit mode 1: 24-bit mode
[0]	rw	1'h0	enable	tx channel 0 enable
0x24			**tx_ch2_entry**	
[31:0]	rw	32'h0	data	tx channel 2 data entry
0x28			**tx_ch3_cfg**	
[31:8]			RSVD	
[7:4]	r	4'h0	fifo_cnt	tx fifo counter
[3]	rw	1'h0	dma_msk	1: mask the dma request for tx ch3
[2]			RSVD	

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表 11-4: Audprc 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	rw	1'h0	format	tx format 0: 16-bit mode 1: 24-bit mode
[0]	rw	1'h0	enable	tx channel 0 enable
0x2C			**tx_ch3_entry**	
[31:0]	rw	32'h0	data	tx channel 3 data entry
0x30			**rx_ch0_cfg**	
[31:8]			RSVD	
[7:4]	r	4'h0	fifo_cnt	rx fifo counter
[3]	rw	1'h0	dma_msk	1: mask the dma request for rx ch0
[2]	rw	1'h0	mode	rx mode 1'h0: mono mode 1'h1: stereo mode This bit is only used for 16-bit mode, in 24-bit mode, channel can only be set in mono mode. In 16-bit stereo mode, rx channel 1 is not working, both left and right audio data comes from channel 0.
[1]	rw	1'h0	format	rx format 0: 16-bit mode 1: 24-bit mode
[0]	rw	1'h0	enable	rx channel 0 enable
0x34			**rx_ch0_entry**	
[31:0]	r	32'h0	data	rx channel 0 data entry
0x38			**rx_ch1_cfg**	
[31:8]			RSVD	
[7:4]	r	4'h0	fifo_cnt	rx fifo counter
[3]	rw	1'h0	dma_msk	1: mask the dma request for rx ch1
[2]			RSVD	
[1]	rw	1'h0	format	rx format 0: 16-bit mode 1: 24-bit mode
[0]	rw	1'h0	enable	rx channel 1 enable
0x3C			**rx_ch1_entry**	
[31:0]	r	32'h0	data	rx channel 1 data entry
0x40			**tx_out_ch0_cfg**	
[31:8]			RSVD	
[7:4]	r	4'h0	fifo_cnt	tx out fifo counter
[3]	rw	1'h0	dma_msk	1: mask the dma request for tx out ch0
[2]	rw	1'h0	mode	tx out mode 1'h0: mono mode 1'h1: stereo mode This bit is only used for 16-bit mode, in 24-bit mode, channel can only be set in mono mode. In 16-bit stereo mode, rx channel 1 is not working, both left and right audio data comes from channel 0.
[1]	rw	1'h0	format	tx out format 0: 16-bit mode 1: 24-bit mode
[0]	rw	1'h0	enable	tx out channel 0 enable

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表 11-4: Audprc 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x44			**tx_out_ch0_entry**	
[31:0]	r	32'h0	data	tx out channel 0 data entry
0x48			**tx_out_ch1_cfg**	
[31:8]			RSVD	
[7:4]	r	4'h0	fifo_cnt	tx out fifo counter
[3]	rw	1'h0	dma_msk	1: mask the dma request for tx out ch1
[2]			RSVD	
[1]	rw	1'h0	format	tx out format 0: 16-bit mode 1: 24-bit mode
[0]	rw	1'h0	enable	tx out channel 1 enable
0x4C			**tx_out_ch1_entry**	
[31:0]	r	32'h0	data	tx out channel 1 data entry
0x50			**dac_path_cfg0**	
[31:30]			RSVD	
[29:28]	rw	2'h0	dst_sel	dac path destination select 2'h0: select audio codec 2'h1: select external interface 2'h2: select apb interface 2'h3: reserved
[27:25]	rw	3'h3	mixrsrc1	dac mixer right channel input source0 select 3'h0:tx ch0 3'h1:tx ch1 3'h2:tx ch2 3'h3:tx ch3 3'h4:mute other: mute
[24:22]	rw	3'h2	mixrsrc0	dac mixer right channel input source0 select 3'h0:tx ch0 3'h1:tx ch1 3'h2:tx ch2 3'h3:tx ch3 3'h4:mute other: mute
[21:19]	rw	3'h1	mixlsrc1	dac mixer left channel input source1 select 3'h0:tx ch0 3'h1:tx ch1 3'h2:tx ch2 3'h3:tx ch3 3'h4:mute other: mute
[18:16]	rw	3'h0	mixlsrc0	dac mixer left channel input source0 select 3'h0:tx ch0 3'h1:tx ch1 3'h2:tx ch2 3'h3:tx ch3 3'h4:mute other: mute

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表 11-4: Audprc 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[15:12]	rw	4'h0	fine_vol_r	dac mixer right channel fine volume control range from 0dB to 6dB step is 0.5dB 4'h0: 0dB 4'h1: 0.5dB ..... 4'hb: 5.5dB 4'hc, 4'hd, 4'he, 4'hf: mute
[11:8]	rw	4'h6	rough_vol_r	dac mixer right channel rough volume control range from -36dB to 54dB step is 6dB 4'h0: -36dB 4'h1: -30dB ..... 4'h6: 0dB ..... 4'he: 48dB 4'hf: 54dB
[7:4]	rw	4'h0	fine_vol_l	dac mixer left channel fine volume control range from 0dB to 6dB step is 0.5dB 4'h0: 0dB 4'h1: 0.5dB ..... 4'hb: 5.5dB 4'hc, 4'hd, 4'he, 4'hf: mute
[3:0]	rw	4'h6	rough_vol_l	dac mixer left channel rough volume control range from -36dB to 54dB step is 6dB 4'h0: -36dB 4'h1: -30dB ..... 4'h6: 0dB ..... 4'he: 48dB 4'hf: 54dB
0x54			**dac_path_cfg1**	
[31:30]	rw	2'h0	src_ch_clr	clear src channal internal data
[29:28]	r	2'h0	src_ch_clr_done	src channel internal data clear done
[27]	rw	1'h0	src_hbf3_mode	3rd stage hbf mode: 0: upsampling 1: downsampling
[26]	rw	1'h0	src_hbf3_en	3rd stage hbf enable
[25]	rw	1'h0	src_hbf2_mode	2nd stage hbf mode: 0: upsampling 1: downsampling
[24]	rw	1'h0	src_hbf2_en	2nd stage hbf enable

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表 11-4: Audprc 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[23]	rw	1'h0	src_hbf1_mode	1st stage hbf mode: 0: upsampling 1: downsampling
[22]	rw	1'h0	src_hbf1_en	1st stage hbf enable
[21:20]	rw	2'h0	src_ch_en	source rate converter channel enable
[19]	rw	1'h0	eq_clr	equalizer clear request
[18]	r	1'h0	eq_clr_done	equalizer clear done flag
[17:14]	rw	4'ha	eq_stage	set equalizer stage, max is 10.
[13:12]	rw	2'h0	eq_ch_en	equalizer channel enable 2'b11: enable both channel 2'b10: enable right chanel only 2'b01: enable left channel only 2'b00: bypass equalizer
[11:9]	rw	3'h3	muxrsrc1	dac mux right channel input source0 select 3'h0:tx ch0 3'h1:tx ch1 3'h2:rx ch0 3'h3:rx ch1 3'h4:mute other: mute
[8:6]	rw	3'h2	muxrsrc0	dac mux right channel input source0 select 3'h0:tx ch0 3'h1:tx ch1 3'h2:rx ch0 3'h3:rx ch1 3'h4:mute other: mute
[5:3]	rw	3'h1	muxlsrc1	dac mux left channel input source1 select 3'h0:tx ch0 3'h1:tx ch1 3'h2:rx ch0 3'h3:rx ch1 3'h4:mute other: mute
[2:0]	rw	3'h0	muxlsrc0	dac mux left channel input source0 select 3'h0:tx ch0 3'h1:tx ch1 3'h2:rx ch0 3'h3:rx ch1 3'h4:mute other: mute
0x58			**dac_path_cfg2**	
[31]	rw	1'h0	src_sinc_en	sinc filter enable
[30:0]	rw	31'h0	sinc_ratio	sinc filter ratio, s31.30 format. Range from 0~2
0x5C			**dac_path_cfg3**	
[31:18]			RSVD	
[17:16]	r	2'h0	ramp_stat_r	dac mixer right channel ramp module status
[15:12]	rw	4'h0	ramp_interval_r	dac mixer right channel volume ramp interval.
[11]	rw	1'h0	zero_adjust_en_r	dac mixer right channel volume adjustment during 0 volume cross enable

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表 11-4: Audprc 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[10]	rw	1'h0	ramp_mode_r	dac mixer right channel volume ramp mode: 1: slowly ramp to target volume. Step is 0.5db 0: directly ramp to target volume.
[9]	rw	1'h0	ramp_en_r	dac mixer right channel volume ramp enable
[8:7]	r	2'h0	ramp_stat_l	dac mixer left channel ramp module status
[6:3]	rw	4'h0	ramp_interval_l	dac mixer left channel volume ramp interval.
[2]	rw	1'h0	zero_adjust_en_l	dac mixer left channel volume adjustment during 0 volume cross enable
[1]	rw	1'h0	ramp_mode_l	dac mixer left channel volume ramp mode: 1: slowly ramp to target volume. Step is 0.5db 0: directly ramp to target volume.
[0]	rw	1'h0	ramp_en_l	dac mixer left channel volume ramp enable
0x60			**adc_path_cfg0**	
[31:19]			RSVD	
[18]	rw	1'h0	rx2tx_loopback	rx to tx loopback enable
[17]	rw	1'h0	data_swap	swap adc path left and right channel data
[16]	rw	1'h0	src_sel	adc path source select 1'h0: select audio codec 1'h1: select external interface
[15:12]	rw	4'h0	fine_vol_r	adc right channel fine volume control range from 0dB to 6dB step is 0.5dB 4'h0: 0dB 4'h1: 0.5dB ..... 4'hb: 5.5dB 4'hc, 4'hd, 4'he, 4'hf: mute
[11:8]	rw	4'h6	rough_vol_r	adc right channel rough volume control range from -36dB to 54dB step is 6dB 4'h0: -36dB 4'h1: -30dB ..... 4'h6: 0dB ..... 4'he: 48dB 4'hf: 54dB
[7:4]	rw	4'h0	fine_vol_l	adc left channel fine volume control range from 0dB to 6dB step is 0.5dB 4'h0: 0dB 4'h1: 0.5dB ..... 4'hb: 5.5dB 4'hc, 4'hd, 4'he, 4'hf: mute

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表 11-4: Audprc 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[3:0]	rw	4'h6	rough_vol_l	adc left channel rough volume control range from -36dB to 54dB step is 6dB 4'h0: -36dB 4'h1: -30dB ..... 4'h6: 0dB ..... 4'he: 48dB 4'hf: 54dB
0x70			**dac_eq_cfg0**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x74			**dac_eq_cfg1**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x78			**dac_eq_cfg2**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x7C			**dac_eq_cfg3**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x80			**dac_eq_cfg4**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x84			**dac_eq_cfg5**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x88			**dac_eq_cfg6**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x8C			**dac_eq_cfg7**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x90			**dac_eq_cfg8**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x94			**dac_eq_cfg9**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x98			**dac_eq_cfg10**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x9C			**dac_eq_cfg11**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xA0			**dac_eq_cfg12**	
[31:24]			RSVD	

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表 11-4: Audprc 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[23:0]	rw	24'h0	coef	
0xA4			**dac_eq_cfg13**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xA8			**dac_eq_cfg14**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xAC			**dac_eq_cfg15**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xB0			**dac_eq_cfg16**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xB4			**dac_eq_cfg17**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xB8			**dac_eq_cfg18**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xBC			**dac_eq_cfg19**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xC0			**dac_eq_cfg20**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xC4			**dac_eq_cfg21**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xC8			**dac_eq_cfg22**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xCC			**dac_eq_cfg23**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xD0			**dac_eq_cfg24**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xD4			**dac_eq_cfg25**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xD8			**dac_eq_cfg26**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xDC			**dac_eq_cfg27**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xE0			**dac_eq_cfg28**	
[31:24]			RSVD	

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表 11-4: Audprc 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[23:0]	rw	24'h0	coef	
0xE4			**dac_eq_cfg29**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xE8			**dac_eq_cfg30**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xEC			**dac_eq_cfg31**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xF0			**dac_eq_cfg32**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xF4			**dac_eq_cfg33**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xF8			**dac_eq_cfg34**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0xFC			**dac_eq_cfg35**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x100			**dac_eq_cfg36**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x104			**dac_eq_cfg37**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x108			**dac_eq_cfg38**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x10C			**dac_eq_cfg39**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x110			**dac_eq_cfg40**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x114			**dac_eq_cfg41**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x118			**dac_eq_cfg42**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x11C			**dac_eq_cfg43**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x120			**dac_eq_cfg44**	
[31:24]			RSVD	

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表 11-4: Audprc 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[23:0]	rw	24'h0	coef	
0x124			**dac_eq_cfg45**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x128			**dac_eq_cfg46**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x12C			**dac_eq_cfg47**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x130			**dac_eq_cfg48**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x134			**dac_eq_cfg49**	
[31:24]			RSVD	
[23:0]	rw	24'h0	coef	
0x138			**RESERVED_IN**	
[31:24]			RSVD	
[23:16]	rw	8'hf	CTRL_2	reserved control 2
[15:8]	rw	8'hf	CTRL_1	reserved control 1
[7:0]	rw	8'hf	CTRL_0	reserved control 0
0x13C			**RESERVED_OUT**	
[31:8]			RSVD	
[7:0]	r	8'h0	STAT	reserved status

11.4 Audcodec

11.4.1 模块功能

Audcodec 模块内包含 DAC 和 ADC 的配置以及相关的供电和时钟配置。

11.4.2 通路架构

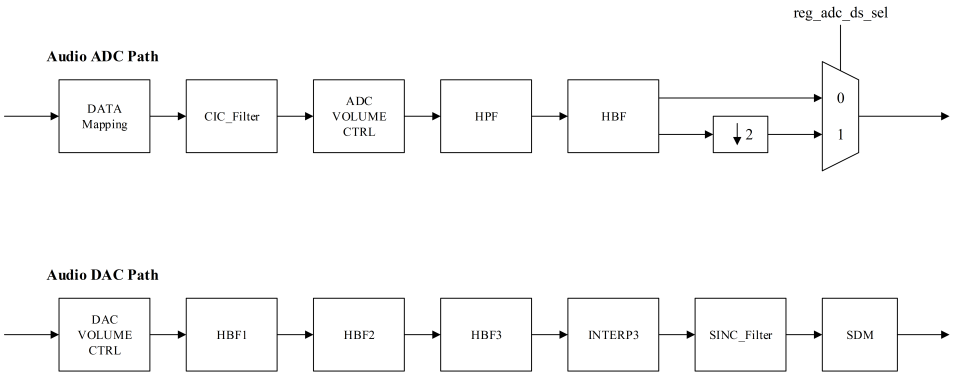


图 11-8: Audcodec 通路架构图

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ADC 和 DAC 的通路上有多个滤波器，针对不同的过采样率配置，硬件会启动相对应的滤波器，保证通路的过采样率满足配置要求。

11.4.3 各模块功能描述

11.4.3.1 供电模块

供电模块负责给 Audio PLL，DAC，ADC，Mic 提供合适的电压和电流。

11.4.3.2 时钟模块

用户可以配置时钟模块，选择 XTAL48M 或者 Audio PLL 作为音频系统的时钟源，为音频系统提供时钟。如果选择 Audio PLL，则需要在配置对 PLL 进行校准，完成后，配置 SDM 模块，设置 Audio PLL 的工作频率。

11.4.3.3 ADC 模块

Audcodec 支持一路 ADC，可以支持 24bit/16bit 两种模式，用户可以配置 APB 模式或者 Normal 模式。APB 模式下，用户可以通过 APB 总线读取 ADC 数据，或者启动 DMA 将音频数据送至内存空间。Normal 模式下，ADC 的数据会被送至 Audprc 模块，用户需要从 Audprc 模块读取 ADC 通路数据。

11.4.3.4 DAC 模块

Audcodec 支持一路 DAC，可以支持 24bit/16bit 两种摸手机，同样用户可以配置 APB 模式或者 Normal 模式。APB 模式下，DAC 数据来自 Audprc 模块，用户配置 Audrpc 模块，将音频数据从内存经过处理后送到 DAC 模块。

11.4.4 Audcodec 配置流程

11.4.4.1 供电部分的配置

供电部分配置分为两部分，第一部分为 bandgap 的配置，bandgap 为整个 audio 模块提供电流，audio 任何子模块启动，都需要先启动 bandgap。第二部分为各个子模块的供电配置，时钟模块，每一路 ADC 和 DAC 均有独立的供电使能配置，用户需要先使能子模块后才能使其正常工作，所有 audio 供电相关配置均在 audcodec 中。

11.4.4.2 时钟部分的配置

Audio 系统提供两种时钟选择，第一种为 Xtal48Mhz，第二种为专用音频 PLL。前者相对功耗低，配置简单，但频率无法微调，且只能支持 48KHz 以及其整数倍分频的采样率。后者功耗高，但可以对频率进行微调，并能够支持 48KHz 以下所有的采样率。时钟的相关配置均在 audcodec 中。

11.4.4.3 ADC 配置

如果需要启动 ADC，则需要对 ADC 的模拟和数字部分分别进行配置。配置信息包括采样率，音量，时钟源，ADC 数据通路滤波器，ADC 数据目标地址等信息。

11.4.4.4 DAC 配置

如果需要启动 DAC，则需要对 DAC 的模拟和数字部分分别进行配置。配置信息包括采样率，音量，时钟源，DAC 数据源地址等信息。

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11.4.5 Audcodec 寄存器

11.4.5.1 Audcodec 寄存器

表 11-5: Audcodec 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**id**	
[31:0]	r	32'hC0DEC000	func	function id
0x04			**cfg**	
[31:5]			RSVD	
[4:3]	rw	2'h0	adc_en_dly_sel	codec adc enable delay count 0: no delay 1: 32 pclk 2: 64 pclk 3: 128 pclk
[2]	rw	1'h0	dac_1k_mode	codec dac sine 1k mode
[1]	rw	1'h0	dac_enable	dac codec enable
[0]	rw	1'h0	adc_enable	adc codec enable
0x08			**irq**	
[31:22]			RSVD	
[21]	rw1c	1'h0	adc_ch1_sat	adc ch1 saturation interrupt
[20]	rw1c	1'h0	adc_ch1_apb_uf	adc ch1 apb fifo underflow interrupt status. Write 1 to clear.
[19]	rw1c	1'h0	adc_ch1_apb_of	adc ch1 apb fifo overflow interrupt status. Write 1 to clear.
[18]	rw1c	1'h0	adc_ch0_sat	adc ch0 saturation interrupt
[17]	rw1c	1'h0	adc_ch0_apb_uf	adc ch0 apb fifo underflow interrupt status. Write 1 to clear.
[16]	rw1c	1'h0	adc_ch0_apb_of	adc ch0 apb fifo overflow interrupt status. Write 1 to clear.
[15:6]			RSVD	
[5]	rw1c	1'h0	dac_ch1_stb_of	dac ch1 input stb fifo overflow interrupt status. Write 1 to clear.
[4]	rw1c	1'h0	dac_ch1_out_uf	dac ch1 output fifo underflow interrupt status. Write 1 to clear.
[3]	rw1c	1'h0	dac_ch1_apb_of	dac ch1 apb fifo overflow interrupt status. Write 1 to clear.
[2]	rw1c	1'h0	dac_ch0_stb_of	dac ch0 input stb fifo overflow interrupt status. Write 1 to clear.
[1]	rw1c	1'h0	dac_ch0_out_uf	dac ch0 output fifo underflow interrupt status. Write 1 to clear.
[0]	rw1c	1'h0	dac_ch0_apb_of	dac ch0 apb fifo overflow interrupt status. Write 1 to clear.
0x0C			**irq_msk**	
[31:22]			RSVD	
[21]	rw	1'h0	adc_ch1_sat	interrupt mask. 0: mask the interrupt.
[20]	rw	1'h0	adc_ch1_apb_uf	interrupt mask. 0: mask the interrupt.
[19]	rw	1'h0	adc_ch1_apb_of	interrupt mask. 0: mask the interrupt.
[18]	rw	1'h0	adc_ch0_sat	interrupt mask. 0: mask the interrupt.
[17]	rw	1'h0	adc_ch0_apb_uf	interrupt mask. 0: mask the interrupt.
[16]	rw	1'h0	adc_ch0_apb_of	interrupt mask. 0: mask the interrupt.
[15:6]			RSVD	
[5]	rw	1'h0	dac_ch1_stb_of	interrupt mask. 0: mask the interrupt.
[4]	rw	1'h0	dac_ch1_out_uf	interrupt mask. 0: mask the interrupt.
[3]	rw	1'h0	dac_ch1_apb_of	interrupt mask. 0: mask the interrupt.
[2]	rw	1'h0	dac_ch0_stb_of	interrupt mask. 0: mask the interrupt.
[1]	rw	1'h0	dac_ch0_out_uf	interrupt mask. 0: mask the interrupt.
[0]	rw	1'h0	dac_ch0_apb_of	interrupt mask. 0: mask the interrupt.
0x10			**dac_cfg**	
[31:27]			RSVD	

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表 11-5: Audcodec 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[26:25]	rw	2'h0	sdm_osr_sel_m	0:100 1:150 2:300 3:256
[24:22]	rw	3'h0	sinc_rate_sel_m	0:25 1:50 2:16 3:32 4:64
[21]	rw	1'h0	interp3_bypass_m	
[20]	rw	1'h0	hbf4_bypass_m	
[19]	rw	1'h0	hbf3_bypass_m	
[18]	rw	1'h0	hbf2_bypass_m	
[17]	rw	1'h0	hbf1_bypass_m	
[16]	rw	1'h0	manual_osr_mode	set 1 to manually set hbf, interp3, sinc and sdm module
[15:8]	rw	8'h1	clk_div	dac clock divider
[7]	rw	1'h0	clk_src_sel	dac clock source select 1: pll 0: xtal
[6]	rw	1'h0	path_reset	dac path reset, set 1 to reset dac path
[5:4]	rw	2'h0	op_mode	dac operation mode 2'h0: normal mode: send dac data through tx interface 2'h1: apb mode: send dac data out through apb interface 2'h2, 2'h3: reserved
[3:0]	rw	4'h0	osr_sel	DAC oversample rate 4'b0000: 100 4'b0001: 150 4'b0010: 200 4'b0011: 300(sdm osr = 150) 4'b0100: 300(sdm osr = 300) 4'b0101: 400 4'b0110: 600 4'b0111: 800 4'b1000: 1200 4'b1001: 256 4'b1010: 512 4'b1011: 1024 other: reserved
0x14			**adc_cfg**	
[31:16]			RSVD	
[15:8]	rw	8'h1	clk_div	adc clock divider
[7]			RSVD	
[6]	rw	1'h0	clk_src_sel	adc clock source select 1: pll 0: xtal
[5]	rw	1'h0	path_reset	adc path reset, set 1 to reset adc path
[4:3]	rw	2'h0	op_mode	adc operation mode 2'h0: normal mode: send adc data out through rx interface 2'h1: apb mode: send adc data out through apb interface 2'h2: raw data apb mode: send adc raw data out through apb interface 2'h3: reserved

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表 11-5: Audcodec 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[2:0]	rw	3'h0	osr_sel	ADC oversample rate 3'b000: 200 3'b001: 300 3'b010: 400 3'b011: 600 other: reserved
0x18			**apb_stat**	
[31:24]			RSVD	
[23:20]	r	4'h0	adc_ch1_fifo_cnt	
[19:16]	r	4'h0	adc_ch0_fifo_cnt	
[15:8]			RSVD	
[7:4]	r	4'h0	dac_ch1_fifo_cnt	
[3:0]	r	4'h0	dac_ch0_fifo_cnt	
0x20			**adc_ch0_cfg**	
[31:20]			RSVD	
[19:18]	rw	2'h0	sat_det_len	adc saturation detect pattern length 2'b00: 16 2'b01: 24 2'b10: 32 2'b11: 48
[17]	rw	1'h0	sat_det_en	adc saturation detect
[16]	rw	1'h0	data_format	adc data format 1: 16-bit 0: 24-bit this bit only affect the data format accessed by apb interface. For 24-bit, every 24-bit data occupied 32-bit word. Bit[31:24] are zeros. For 16-bit mode, every 32-bit word contains two 16-bit audio dataD1, D0
[15:12]	rw	4'h0	fine_vol	adc fine volume control range from 0dB to 6dB step is 0.5dB 4'h0: 0dB 4'h1: 0.5dB ..... 4'hb: 5.5dB 4'hc, 4'hd, 4'he, 4'hf: mute
[11:8]	rw	4'ha	rough_vol	adc rough volume control range from -60dB to 30dB step is 6dB 4'h0: -60dB 4'h1: -54dB ..... 4'ha: 0dB ..... 4'he: 24dB 4'hf: 30dB
[7]	rw	1'h0	dma_en	dma interface enable in apb mode and raw data apb mode 1: enable adc ch0 dma request interface 0: disable adc ch0 dma request interface
[6]	rw	1'h0	stb_inv	adc strobe inverter

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表 11-5: Audcodec 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[5:2]	rw	4'h0	hpf_coef	high-pass filter coefficient
[1]	rw	1'h0	hpf_bypass	high-pass filter bypass
[0]	rw	1'h0	enable	adc channel enable
0x24			**adc_ch1_cfg**	
[31:20]			RSVD	
[19:18]	rw	2'h0	sat_det_len	adc saturation detect pattern length 2'b00: 16 2'b01: 24 2'b10: 32 2'b11: 48
[17]	rw	1'h0	sat_det_en	adc saturation detect
[16]	rw	1'h0	data_format	adc data format 1: 16-bit 0: 24-bit this bit only affect the data format accessed by apb interface. For 24-bit, every 24-bit data occupied 32-bit word. Bit[31:24] are zeros. For 16-bit mode, every 32-bit word contains two 16-bit audio dataD1, D0
[15:12]	rw	4'h0	fine_vol	adc fine volume control range from 0dB to 6dB step is 0.5dB 4'h0: 0dB 4'h1: 0.5dB ..... 4'hb: 5.5dB 4'hc, 4'hd, 4'he, 4'hf: mute
[11:8]	rw	4'ha	rough_vol	adc rough volume control range from -60dB to 30dB step is 6dB 4'h0: -60dB 4'h1: -54dB ..... 4'ha: 0dB ..... 4'he: 24dB 4'hf: 30dB
[7]	rw	1'h0	dma_en	dma interface enable in apb mode and raw data apb mode 1: enable adc ch0 dma request interface 0: disable adc ch0 dma request interface
[6]	rw	1'h0	stb_inv	adc strobe inverter
[5:2]	rw	4'h0	hpf_coef	high-pass filter coefficient
[1]	rw	1'h0	hpf_bypass	high-pass filter bypass
[0]	rw	1'h0	enable	adc channel enable
0x30			**dac_ch0_cfg**	
[31]			RSVD	
[30]	rw	1'h0	clk_ana_pol	analog dac clock polarity
[29]	rw	1'h0	dither_en	sdm dither enable
[28:26]	rw	3'h3	dither_gain	sdm dither gain
[25:17]	rw	9'h0	sinc_gain	dac sinc filter gain

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表 11-5: Audcodec 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[16]	rw	1'h0	data_format	dac data format 1: 16-bit 0: 24-bit this bit only affect the data format accessed by apb interface. For 24-bit, every 24-bit data occupied 32-bit word. Bit[31:24] are zeros. For 16-bit mode, every 32-bit word contains two 16-bit audio dataD1, D0
[15:12]	rw	4'h0	fine_vol	dac fine volume control range from 0dB to 6dB step is 0.5dB 4'h0: 0dB 4'h1: 0.5dB ..... 4'hb: 5.5dB 4'hc, 4'hd, 4'he, 4'hf: mute
[11:8]	rw	4'h6	rough_vol	dac rough volume control range from -36dB to 54dB step is 6dB 4'h0: -36dB 4'h1: -30dB ..... 4'h6: 0dB ..... 4'he: 48dB 4'hf: 54dB
[7]	rw	1'h0	dma_en	dma interface enable in apb mode 1: enable dac ch0 dma request interface 0: disable dac ch0 dma request interface
[6:4]	r	3'h0	stb_fifo_cnt	dac input stb fifo cnt
[3:2]	rw	2'h1	dem_mode	dem output mode 2'h0: no shift for dem output 2'h1: shift dem output incrementally 2'h2: shift dem output according to input 2'h3: reserved
[1]	rw	1'h1	dout_mute	dac output mute, set 1 to mute the output
[0]	rw	1'h0	enable	dac channel enable
0x34			**dac_ch0_cfg_ext**	
[31:9]			RSVD	
[8:7]	r	2'h0	ramp_stat	ramp module status
[6:3]	rw	4'h0	ramp_interval	volume ramp interval.
[2]	rw	1'h0	zero_adjust_en	enable volume adjustment during 0 volume cross.
[1]	rw	1'h0	ramp_mode	volume ramp mode: 1: slowly ramp to target volume. Step is 0.5db 0: directly ramp to target volume.
[0]	rw	1'h0	ramp_en	volume ramp enable
0x38			**dac_ch1_cfg**	
[31]			RSVD	
[30]	rw	1'h0	clk_ana_pol	analog dac clock polarity
[29]	rw	1'h0	dither_en	sdm dither enable
[28:26]	rw	3'h3	dither_gain	sdm dither gain

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表 11-5: Audcodec 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[25:17]	rw	9'h0	sinc_gain	dac sinc filter gain
[16]	rw	1'h0	data_format	dac data format 1: 16-bit 0: 24-bit this bit only affect the data format accessed by apb interface. For 24-bit, every 24-bit data occupied 32-bit word. Bit[31:24] are zeros. For 16-bit mode, every 32-bit word contains two 16-bit audio dataD1, D0
[15:12]	rw	4'h0	fine_vol	dac fine volume control range from 0dB to 6dB step is 0.5dB 4'h0: 0dB 4'h1: 0.5dB ..... 4'hb: 5.5dB 4'hc, 4'hd, 4'he, 4'hf: mute
[11:8]	rw	4'h6	rough_vol	dac rough volume control range from -36dB to 54dB step is 6dB 4'h0: -36dB 4'h1: -30dB ..... 4'h6: 0dB ..... 4'he: 48dB 4'hf: 54dB
[7]	rw	1'h0	dma_en	dma interface enable in apb mode 1: enable dac ch0 dma request interface 0: disable dac ch0 dma request interface
[6:4]	r	3'h0	stb_fifo_cnt	dac input stb fifo cnt
[3:2]	rw	2'h1	dem_mode	dem output mode 2'h0: no shift for dem output 2'h1: shift dem output incrementally 2'h2: shift dem output according to input 2'h3: reserved
[1]	rw	1'h1	dout_mute	dac output mute, set 1 to mute the output
[0]	rw	1'h0	enable	dac channel enable
0x3C			**dac_ch1_cfg_ext**	
[31:9]			RSVD	
[8:7]	r	2'h0	ramp_stat	ramp module status
[6:3]	rw	4'h0	ramp_interval	volume ramp interval.
[2]	rw	1'h0	zero_adjust_en	enable volume adjustment during 0 volume cross.
[1]	rw	1'h0	ramp_mode	volume ramp mode: 1: slowly ramp to target volume. Step is 0.5db 0: directly ramp to target volume.
[0]	rw	1'h0	ramp_en	volume ramp enable
0x40			**adc_ch0_entry**	
[31:0]	r	32'h0	data	adc channel0 data output
0x44			**adc_ch1_entry**	
[31:0]	r	32'h0	data	adc channel1 data output

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表 11-5: Audcodec 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x50			**dac_ch0_entry**	
[31:0]	rw	32'h0	data	dac channel0 data input
0x54			**dac_ch1_entry**	
[31:0]	rw	32'h0	data	dac channel0 data input
0x58			**dac_ch0_debug**	
[31:17]			RSVD	
[16]	rw	1'h0	bypass	debug bypass mode
[15:0]	rw	16'hff	data_out	debug dac output
0x5C			**dac_ch1_debug**	
[31:17]			RSVD	
[16]	rw	1'h0	bypass	debug bypass mode
[15:0]	rw	16'hff	data_out	debug dac output
0x60			**dac_ch0_dc**	
[31:24]			RSVD	
[23:0]	rw	24'h0	offset	dac ch0 dc offset
0x64			**dac_ch1_dc**	
[31:24]			RSVD	
[23:0]	rw	24'h0	offset	dac ch1 dc offset
0x70			**common_cfg**	
[31:9]			RSVD	
[8:6]	rw	3'h0	DC_MR	DC test Macro select
[5:3]	rw	3'h0	DC_BR	DC test Block select
[2:0]	rw	3'h0	DC_TR	DC test point select
0x74			**bg_cfg0**	
[31:14]			RSVD	
[13]	rw	1'h0	SET_VC	set vc
[12]	rw	1'h1	EN_AMP	enable bg opamp
[11:9]	rw	3'h4	MIC_VREF_SEL	select mic vref
[8]	rw	1'h1	EN_RCFLT	enable bandgap rc filter
[7]	rw	1'h1	EN_SMPL	enable bandgap sample
[6]	rw	1'h1	EN_CHOP	enable bandgap chop
[5:2]	rw	4'hc	VREF_SEL	set vref, 12: 2.2V
[1]	rw	1'h0	LP_MODE	1: bandgap lp mode
[0]	rw	1'h0	EN	enable bandgap
0x78			**bg_cfg1**	
[31:0]	rw	32'h0	SAMPCLK_HI	bg sample clock high cycle width, based on 0: stop bg sample clock
0x7C			**bg_cfg2**	
[31:0]	rw	32'h0	SAMPCLK_LO	bg sample clock low cycle width. 0: stop bg sample clock
0x80			**refgen_cfg**	
[31:9]			RSVD	
[8]	rw	1'h0	DISCHG	discharge vref
[7:6]	rw	2'h0	RZSEL	sel Rz, 0: 1uF cap
[5]	rw	1'h0	LV_MODE	low vol mode
[4]	rw	1'h0	LP_MODE	1: lpmode(adc), 0:dac
[3:2]	rw	2'h1	BM	bias mode
[1]	rw	1'h1	EN_CHOP	enable ref gen chop
[0]	rw	1'h0	EN	enable ref gen
0x84			**pll_cfg0**	

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表 11-5: Audcodec 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31]			RSVD	
[30:29]	rw	2'h2	SEL_CKREF	select ref clock, 2: 24MHz
[28]	rw	1'h0	EN_IARY	enable I array
[27]	rw	1'h0	EN_VCO	enable vco
[26:23]	rw	4'h7	SEL_VREF_VCO	ldo vref, 7:1.1V
[22]	rw	1'h1	EN_VCO_FLT	vco bais filter
[21:17]	rw	5'ha	FC_VCO	VCO Fcode
[16]	rw	1'h0	VCO_LP_MODE	1: lp mode
[15]	rw	1'h0	EN_ANA	enable ana block
[14:11]	rw	4'h7	SEL_VREF_ANA	ldo vref, 7:1.1V
[10:6]	rw	5'h1	ICP_SEL	select Icp, 1:1.25u
[5]	rw	1'h0	OPEN	1: pll open
[4:0]	rw	5'h0	ICP_OS_SEL	Icp os
0x88			**pll_cfg1**	
[31:16]			RSVD	
[15]	rw	1'h0	CSD_EN	enable CSD
[14]	rw	1'h0	CSD_RST	reset CSD, high active
[13:11]	rw	3'h6	CZ_SEL	select Cz
[10:8]	rw	3'h5	C2_SEL	select C2
[7:4]	rw	4'hb	RZ_SEL	select Rz
[3:0]	rw	4'hb	R3_SEL	select R3
0x8C			**pll_cfg2**	
[31:19]			RSVD	
[18]	rw	1'h0	EN_LF_VCIN	enable vcin for vco
[17:15]	rw	3'h4	SEL_LF_VCIN	select vcin, 4: 550mV
[14]	rw	1'h0	EN_LF_TSTBUF	enable vctrl buf
[13]	rw	1'h0	EN_DIG	enable dig block
[12:9]	rw	4'h7	SEL_VREF_DIG	ldo vref, 7:1.1V
[8]	rw	1'h1	RSTB	resetb
[7]	rw	1'h1	RSTB_SYNC_EN	resetb sync
[6]	rw	1'h0	TE_DTEST	enable dtest
[5:2]	rw	4'h0	TR_DTEST	select dtest
[1:0]	rw	2'h0	MMD_STG	mmd stg
0x90			**pll_cfg3**	
[31]	rw	1'h0	SDMCLK_POL	sdm dig clk polarity
[30]	rw	1'h0	EN_SDM	enable sdm
[29]	rw	1'h1	SDM_DITHER	sdm dither
[28]	rw	1'h1	EN_SDM_DITHER	enable sdm dither
[27]	rw	1'h1	SDM_MODE	sdm mode
[26]	rw	1'h0	SDMIN_BYPASS	1: bypass FCW and SDIN sdm control signal
[25]	rw1c	1'h0	SDM_UPDATE	write 1 to update FCW and SDIN value
[24:20]	rw	5'h4	FCW	FCW
[19:0]	rw	20'h0	SDIN	sdm input
0x94			**pll_cfg4**	
[31:24]			RSVD	
[23]	rw	1'h1	EN_CLK_DIG	enable dig clk
[22:18]	rw	5'h2	DIVA_CLK_DIG	DIVA dig clk
[17:16]	rw	2'h1	CLK_DIG_STR	strength

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表 11-5: Audcodec 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[15]	rw	1'h0	SEL_CLK_DIG	select dig clk 0: pll 1: 24MHz from xtal
[14:13]	rw	2'h0	SEL_CLK_DAC_SOURCE	0: xtal 1: pll
[12]	rw	1'h1	SEL_CLK_DAC	1: select 9.6MHz as DAC clock
[11]	rw	1'h0	EN_CLK_DAC	enable dac clk
[10:6]	rw	5'h5	DIVA_CLK_DAC	DIVA dac clk
[5]	rw	1'h0	EN_CLK_CHOP_DAC	enable dac chop clk
[4:2]	rw	3'h4	DIVA_CLK_CHOP_DAC	DIVA dac chop clk
[1:0]	rw	2'h2	DIVB_CLK_CHOP_DAC	DIVB dac chop clk
0x98			**pll_cfg5**	
[31:29]			RSVD	
[28]	rw	1'h1	SEL_CLK_DAC2	1: select 9.6MHz as DAC clock
[27]	rw	1'h0	EN_CLK_DAC2	enable dac2 clk
[26:22]	rw	5'h5	DIVA_CLK_DAC2	DIVA dac2 clk
[21]	rw	1'h0	EN_CLK_CHOP_DAC2	enable dac2 chop clk
[20:18]	rw	3'h4	DIVA_CLK_CHOP_DAC2	DIVA dac2 chop clk
[17:16]	rw	2'h2	DIVB_CLK_CHOP_DAC2	DIVB dac2 chop clk
[15]	rw	1'h0	EN_CLK_CHOP_REFGEN	enable ref chop clk
[14:10]	rw	5'h14	DIVA_CLK_CHOP_REFGEN	DIVA ref chop clk
[9:8]	rw	2'h2	DIVB_CLK_CHOP_REFGEN	DIVB ref chop clk
[7]	rw	1'h0	EN_CLK_CHOP_BG	enable bg chop clk
[6:2]	rw	5'h14	DIVA_CLK_CHOP_BG	DIVA bg chop clk
[1:0]	rw	2'h2	DIVB_CLK_CHOP_BG	DIVB bg chop clk
0x9C			**pll_cfg6**	
[31:26]			RSVD	
[25:24]	rw	2'h0	SEL_CLK_ADC_SOURCE	0: xtal, 1: pll
[23]	rw	1'h0	EN_CLK_ADC0	enable adc0 clk
[22:20]	rw	3'h5	DIVA_CLK_ADC0	DIVA adc0 clk
[19]	rw	1'h1	SEL_CLK_ADC0	select adc0 clk
[18]	rw	1'h0	EN_CLK_ADC1	enable adc1 clk
[17:15]	rw	3'h5	DIVA_CLK_ADC1	DIVA adc1 clk
[14]	rw	1'h1	SEL_CLK_ADC1	select adc1 clk
[13]	rw	1'h0	EN_CLK_ADC2	enable adc2 clk
[12:10]	rw	3'h5	DIVA_CLK_ADC2	DIVA adc2 clk
[9]	rw	1'h1	SEL_CLK_ADC2	select adc2 clk
[8]	rw	1'h0	EN_CLK_CHOP_MICBIAS	enable micbias chop clk
[7:6]	rw	2'h3	SEL_CLK_CHOP_MICBIAS	select micbias chop clk
[5]	rw	1'h0	EN_CLK_RCCAL	enable RC CAL clk
[4]	rw	1'h0	EN_TST_CLK	enable test clk
[3:0]	rw	4'h0	SEL_TST_CLK	select clk to test
0xA0			**pll_stat**	
[31:3]			RSVD	
[2]	r	1'h0	SLIPPED_DN	slip dn
[1]	r	1'h0	SLIPPED_UP	slip up
[0]	r	1'h0	UNLOCK	1:pll unlock
0xA4			**pll_cal_cfg**	
[31:16]	rw	16'hff	len	calibration length
[15:2]			RSVD	
[1]	r	1'h0	done	calibration done

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表 11-5: Audcodec 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[0]	rw	1'h0	en	calibration enable
0xA8			**pll_cal_result**	
[31:16]	r	16'h0	pll_cnt	pll calibration counter result
[15:0]	r	16'h0	xtal_cnt	xtal calibration counter result
0xAC			**adc_ana_cfg**	
[31:7]			RSVD	
[6:2]	rw	5'hb	CAPCODE	ADC cap code
[1]	rw	1'h0	MICBIAS_EN	micbias enable
[0]	rw	1'h1	MICBIAS_CHOP_EN	micbias chopping enable
0xB0			**adc1_cfg1**	
[31:25]			RSVD	
[24:23]	rw	2'h0	FSP	sampling frequency: 0x0:9.6M 0x1:8.82M 0x2:4.8M 0x3:4.41M
[22]	rw	1'h0	DIFF_EN	enable differential input mode
[21]	rw	1'h0	DACN_EN	enable negative DAC1
[20:18]	rw	3'h1	GC	gaincode: 0x0:-6dB 0x1:0dB ... 0x4:18dB
[17:15]	rw	3'h4	VST_SEL	start voltage 0x0:VCM+200mV 0x7:VCM+550mV
[14:12]	rw	3'h5	BM_INT1	bias mode of first opamp
[11:9]	rw	3'h5	BM_INT2	bias mode of 2nd and 3rd opamp
[8:6]	rw	3'h4	VREF_SEL	vref code from proper vcm in flash7 0x0:1.2V 0x1:1.4V 0x7:2.6V
[5:4]	rw	2'h3	FCHOP_SEL	chopping frequncy 0x0:/8 0x1:/16 0x2:/32 0x3:/64
[3]	rw	1'h0	VCMST	VCM quick settling
[2]	rw	1'h0	CLKOUT_INV	inverse output clock
[1:0]	rw	2'h3	PERI_BM	peripheral circuits biasmode
0xB4			**adc1_cfg2**	
[31:4]			RSVD	
[3]	rw	1'h0	EN	enable adc
[2]	rw	1'h1	RSTB	reset adc
[1]	rw	1'h1	CHOP_EN	chopping enable
[0]	rw	1'h0	CLEAR	clear adc
0xB8			**adc2_cfg1**	
[31:25]			RSVD	

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表 11-5: Audcodec 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[24:23]	rw	2'h0	FSP	sampling frequency: 0x0:9.6M 0x1:8.82M 0x2:4.8M 0x3:4.41M
[22:18]	rw	5'ha	GC	gaincode: 0x0:-10dB 0xa:0dB 0x1e:20dB
[17:15]	rw	3'h4	VST_SEL	start voltage 0x0:VCM+200mV 0x7:VCM+550mV
[14:12]	rw	3'h5	BM_INT1	bias mode of first opamp
[11:9]	rw	3'h5	BM_INT2	bias mode of 2nd and 3rd opamp
[8:6]	rw	3'h4	VREF_SEL	vref code from proper vcm in flash7 0x0:1.2V 0x1:1.4V 0x7:2.6V
[5:4]	rw	2'h3	FCHOP_SEL	chopping frequncy 0x0:/8 0x1:/16 0x2:/32 0x3:/64
[3]	rw	1'h0	VCMST	VCM quick settling
[2]	rw	1'h0	CLKOUT_INV	inverse output clock
[1:0]	rw	2'h3	PERI_BM	peripheral circuits biasmode
0xBC			**adc2_cfg2**	
[31:4]			RSVD	
[3]	rw	1'h0	EN	enable adc
[2]	rw	1'h1	RSTB	reset adc
[1]	rw	1'h1	CHOP_EN	chopping enable
[0]	rw	1'h0	CLEAR	clear adc
0xC0			**dac1_cfg**	
[31:26]			RSVD	
[25:24]	rw	2'h1	SEL_VSTART	select Vstart
[23]	rw	1'h0	EN_DAC	enable dac
[22]	rw	1'h0	EN_VCM	enable vcm
[21]	rw	1'h0	EN_AMP	enable amp
[20]	rw	1'h1	EN_CHOP	enable chop
[19:18]	rw	2'h1	BM	bias mode
[17:15]	rw	3'h7	SEL_VCM	select vcm
[14]	rw	1'h0	LP_MODE	0: 3.3V sup, 1: 1.8V supply
[13]	rw	1'h0	POL_CLK	dac clk polarity
[12]	rw	1'h1	SR	dac short switch
[11:8]	rw	4'h0	GAIN	dac gain
[7:1]	rw	7'h0	OS_DAC	os dac
[0]	rw	1'h0	EN_OS_DAC	enable os dac
0xC4			**dac2_cfg**	

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表 11-5: Audcodec 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:26]			RSVD	
[25:24]	rw	2'h1	SEL_VSTART	select Vstart
[23]	rw	1'h0	EN_DAC	enable dac
[22]	rw	1'h0	EN_VCM	enable vcm
[21]	rw	1'h0	EN_AMP	enable amp
[20]	rw	1'h1	EN_CHOP	enable chop
[19:18]	rw	2'h1	BM	bias mode
[17:15]	rw	3'h7	SEL_VCM	select vcm
[14]	rw	1'h0	LP_MODE	0: 3.3V sup, 1: 1.8V supply
[13]	rw	1'h0	POL_CLK	dac clk polarity
[12]	rw	1'h1	SR	dac short switch
[11:8]	rw	4'h0	GAIN	dac gain
[7:1]	rw	7'h0	OS_DAC	os dac
[0]	rw	1'h0	EN_OS_DAC	enable os dac
0xD0			**RESERVED_IN0**	
[31:24]	rw	8'h0	CTRL3	reserved control 3
[23:16]	rw	8'h0	CTRL2	reserved control 2
[15:8]	rw	8'h0	CTRL1	reserved control 1
[7:0]	rw	8'h0	CTRL0	reserved control 0
0xD4			**RESERVED_IN1**	
[31:16]			RSVD	
[15:8]	rw	8'hff	CTRL5	reserved control 5
[7:0]	rw	8'h0	CTRL4	reserved control 4
0xD8			**RESERVED_OUT**	
[31:16]			RSVD	
[15:8]	r	8'h0	STAT1	reserved status1
[7:0]	r	8'h0	STAT0	reserved status0

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12 加速器

12.1 数字信号处理加速器

12.1.1 Cordic 协处理器

Cordic 协处理器用于计算三角函数和双曲函数及其推演出的一些算术运算。只在 HPSYS 中集成了一个 Cordic 协处理器。

Cordic 协处理器特性如下：

- 支持 ARM coprocessor 协处理器指令
- 支持 ARM Custom Datapath Extention 指令（只有 HPSYS）
- 支持三角函数类运算：cos、sin、ang、mod、atan、rot
- 支持双曲函数类运算 cosh、sinh、atanh、angh、modh、mul、div、ln、exp、sqrt
- 支持 32 位定点输入输出

12.2 CRC

12.2.1 简介

CRC(Cyclic Redundancy Check) 可进行特定位宽，任意生成多项式，任意初始值的 CRC 计算。数据可以通过 CPU 或 DMA 输入，最小输入单元为单字节，没有最长字节数限制。单 HCLK 周期即能够完成单字节输入的计算。数据输入全部完成后即时得到校验结果。支持输入数据高低位倒转和输出数据高低位倒转。支持不同有效位宽的输入数据。

12.2.2 主要特性

- 7/8/16/32 比特 CRC 计算
- 任意自定义多项式
- 任意初始值
- 输入数据支持单字节/双字节/三字节/四字节有效位宽
- 输入数据支持字节/双字节/四字节高低位比特倒转
- 输出数据支持高低位比特倒转
- 计算速度为每 HCLK 周期 1 字节

12.2.3 CRC 配置方法

启动 CRC 计算前，需要预先配置相应寄存器，包括多项式宽度，有效数据位宽，输入输出倒转模式，多项式和初始值等。主流的 CRC 格式配置方法见下表。

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表 12-1: CRC 配置方法

CRC 算法	多项式公式	POLYSIZE	POL	INIT	REV_IN	REV_OUT	结果异或值
CRC-7/MMC	x^7+x^3+1	3	0x09	0x00	0	0	0x00
CRC-8	x^8+x^2+x+1	2	0x07	0x00	0	0	0x00
CRC-8/ITU	x^8+x^2+x+1	2	0x07	0x00	0	0	0x55
CRC-8/ROHC	x^8+x^2+x+1	2	0x07	0xFF	1	1	0x00
CRC-8/MAXIM	$x^8+x^5+x^4+1$	2	0x31	0x00	1	1	0x00
CRC-16/IBM	$x^{16}+x^5+x^2+1$	1	0x8005	0x0000	1	1	0x0000
CRC-16/MAXIM	$x^{16}+x^5+x^2+1$	1	0x8005	0x0000	1	1	0xFFFF
CRC-16/USB	$x^{16}+x^5+x^2+1$	1	0x8005	0xFFFF	1	1	0xFFFF
CRC-16/ MODBUS	$x^{16}+x^5+x^2+1$	1	0x8005	0xFFFF	1	1	0x0000
CRC-16/CCITT	$x^{16}+x^{12}+x^5+1$	1	0x1021	0x0000	1	1	0x0000
CRC-16/ CCITT-FALSE	$x^{16}+x^{12}+x^5+1$	1	0x1021	0xFFFF	0	0	0x0000
CRC-16/x5	$x^{16}+x^{12}+x^5+1$	1	0x1021	0xFFFF	1	1	0xFFFF
CRC-16/ XMODEM	$x^{16}+x^{12}+x^5+1$	1	0x1021	0x0000	0	0	0x0000
CRC-16/DNP	$x^{16}+x^{13}+x^{12}+x^{11}+$ $x^{10}+x^8+x^6+x^5+x^2+1$	1	0x3D65	0x0000	1	1	0xFFFF
CRC-32	$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+$ $x^{12}+x^{11}+x^{10}+x^8+x^7+$ $x^5+x^4+x^2+x+1$	0	0x04C11DB7	0xFFFFFFFF	1	1	0xFFFFFFFF
CRC-32/ MPEG-2	$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+$ $x^{12}+x^{11}+x^{10}+x^8+x^7+$ $x^5+x^4+x^2+x+1$	0	0x04C11DB7	0xFFFFFFFF	0	0	0x00000000

CRC 模块不进行结果异或运算，需要由软件读出结果后进行后处理。

12.2.4 数据格式

CRC 计算的基本数据单元为字节。向 DR 寄存器写入的数据固定为 4 字节，该数据中哪些字节参与运算由 CR_DATASIZE 指定。下表中灰色格子参与运算。

表 12-2: 参与运算的数据

CR_DATASIZE	DR			
0	BYTE3	BYTE2	BYTE1	BYTE0
1	BYTE3	BYTE2	BYTE1	BYTE0
2	BYTE3	BYTE2	BYTE1	BYTE0
3	BYTE3	BYTE2	BYTE1	BYTE0

可以单独指定每一笔数据参与运算的字节，但应注意改变 CR_DATASIZE 必须在 SR_DONE 为 1 时，否则可能影响当前数据的计算结果。

运算顺序由 BYTE0,BYTE1,BYTE2,BYTE3 依次进行。计算每个字节时，默认按照从最高比特到最低比特的次序进行。如果配置了输入倒转模式，则按照倒转后从最高比特到最低比特的次序进行。下表为配置的示例，可根据内存中的数据格式灵活调整输入格式。

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表 12-3: 运算顺序

DATASIZE	REV_IN	DR	倒转后输入	第一拍计算字节	第二拍计算字节	第三拍计算字节	第四拍计算字节
0	0	0x12345678	/	0x78	/	/	/
1	0	0x12345678	/	0x78	0x56	/	/
2	0	0x12345678	/	0x78	0x56	0x34	/
3	0	0x12345678	/	0x78	0x56	0x34	0x12
3	1	0x12345678	0x482C6A1E	0x1E	0x6A	0x2C	0x48
3	2	0x12345678	0x2C481E6A	0x6A	0x1E	0x48	0x2C
3	3	0x12345678	0x1E6A2C48	0x48	0x2C	0x6A	0x1E

12.2.5 计算速率

CRC 每个 HCLK 周期完成一个字节的计算。数据连续输入时，计算花费的时间约为字节数 ×HCLK 周期。

12.2.6 CRC 配置流程

1. 配置 CRC 格式，依需求设置 POL，INIT，CR_POLYSIZE，CR_REV_IN，CR_REV_OUT，CR_DATASIZE。
2. CR_RESET 置 1 初始化 CRC。
3. 由 CPU 或 DMA 向 DR 寄存器连续搬运所需数据。
4. 如果还剩余的数据字节数与 CR_DATASIZE 不匹配，则需首先查询 SR_DONE，为 1 时改变 CR_DATASIZE，并将剩余数据写入 DR 寄存器。
5. 读 DR 寄存器获取计算结果，并根据需求进行软件异或运算，得到最终 CRC 值。

12.2.7 CRC 寄存器

表 12-4: CRC 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**DR**	Data register
[31:0]	rw	32'hffffffff	DR	Data register bits. This register is used to write new data to the CRC calculator. It holds the previous CRC calculation result when it is read. If the data size is less than 32 bits, the least significant bits are used to write/read the correct value.
0x04			**SR**	Status register
[31:2]			RSVD	
[1]	r	1'h0	overflow	Overflow when new data arrive while last calculation not done yet
[0]	r	1'h0	done	Done flag. When DR written, done flag will be cleared automatically. The flag will assert after CRC operation of current DR finished.
0x08			**CR**	Control register
[31:8]			RSVD	
[7]	rw	1'h0	REV_OUT	Reverse output data This bit controls the reversal of the bit order of the output data. 0: Bit order not affected 1: Bit-reversed output format

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表 12-4: CRC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[6:5]	rw	2'h0	REV_IN	Reverse input data These bits control the reversal of the bit order of the input data 00: Bit order not affected 01: Bit reversal done by byte 10: Bit reversal done by half-word 11: Bit reversal done by word
[4:3]	rw	2'h0	POLYSIZE	Polynomial size These bits control the size of the polynomial. 00: 32 bit polynomial 01: 16 bit polynomial 10: 8 bit polynomial 11: 7 bit polynomial
[2:1]	rw	2'h3	DATASIZE	Valid input data size These bits control the valid size of the input data. 00: lower 8-bit 01: lower 16-bit 10: lower 24-bit 11: all 32-bit
[0]	w	1'h0	RESET	This bit is set by software to reset the CRC calculation unit and set the data register to the value stored in the CRC_INIT register. This bit can only be set, it is automatically cleared by hardware
0x10			**INIT**	Initial CRC value
[31:0]	rw	32'hffffffff	INIT	Programmable initial CRC value
0x14			**POL**	CRC polynomial
[31:0]	rw	32'h04c11db7	POL	Programmable polynomial This register is used to write the coefficients of the polynomial to be used for CRC calculation. If the polynomial size is less than 32 bits, the least significant bits have to be used to program the correct value.

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13 安全

13.1 AES

13.1.1 简介

SF32LB57x 的 AES_ACC 模块主要针对安全领域的专用算法进行加解密的运算加速。对称加密算法包括 AES128、AES192、AES256 和 SM4。模式包括 ECB、CTR 和 CBC。散列算法包括 SHA1、SHA224、SHA256 和 SM3。启动后，AES_ACC 模块调用内部的 DMA 读入原始数据，根据算法将相应的结果通过内部 DMA 写入目标地址，或者存储在模块内部寄存器中。

13.1.2 AES 功能描述

13.1.2.1 对称加密算法

对称加密算法主要包括 AES 和 SM4，其中 AES 根据 Key 的长度不同又分为 AES128、AES192 和 AES256，SM4 则是国密的对称加密算法。强度上密码长度越长则强度越高，同时加解密花费的时间也会更长，SM4 算法花费的时间则是最长。

13.1.2.2 对称加密模式

对称加密模式主要包括 ECB、CTR 和 CBC。

ECB 模式：ECB 模式通过 KEY 直接对明文数据进行加解密，数据按 16byte 为一组，每次加解密都是对整个 16byte 进行操作。优点是每组数据之间相互独立，可以并行计算，支持数据按组的随机读写。缺点是不同组数据若明文相同，则密文也相同，容易被破解。

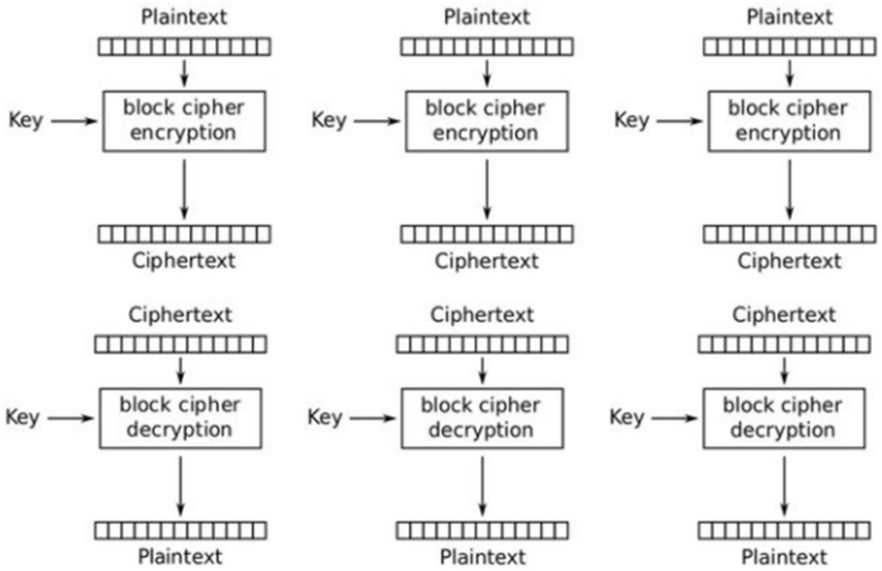


图 13-1: ECB 模式解密

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CTR 模式：CTR 模式通过 KEY 对一个由 NONCE 和 COUNTER 组成的向量进行加密，然后用加密后的结果与明文数据进行异或，得到数据密文，实现加密操作。解密时用相同的向量加密后的结果与密文数据进行异或，得到明文数据，实现解密操作。实际使用中，NONCE 通常用常数表示，COUNTER 则会使用数据的地址，这样保证每组数据的向量不同，从而使加解密过程中使用的异或数据也不相同。在了解 CTR 使用的向量组成方式的情况下，该模式每组数据加解密互相独立，可以并行计算，这一点与 ECB 模式相同。同时该模式只有加密和异或运算，结构也相对简单。加解密时对向量的运算与数据无关，所以该模式常用于外部存储的数据进行加解密。

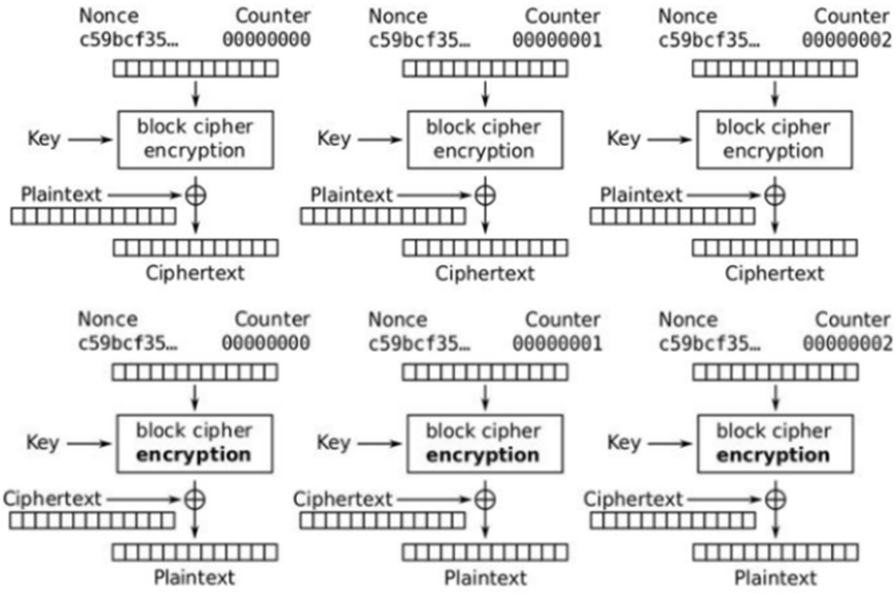


图 13-2: CTR 模式解密

CBC 模式：CBC 模式是将上一组数据的密文，作为初始化向量与当前组异或之后，用 KEY 进行加密生成密文。解密时用 KEY 将密文解密后与上一组的密文进行异或，生成明文。该模式既可以对数据进行加解密也可以将最后一组密文数据作为数据的 MAC 值进行完整性校验，因为该模式加解密过程中，每组数据之间都相互关联，所以安全度更高，但无法做到并行计算，也无法对单独某组数据进行随机读写。

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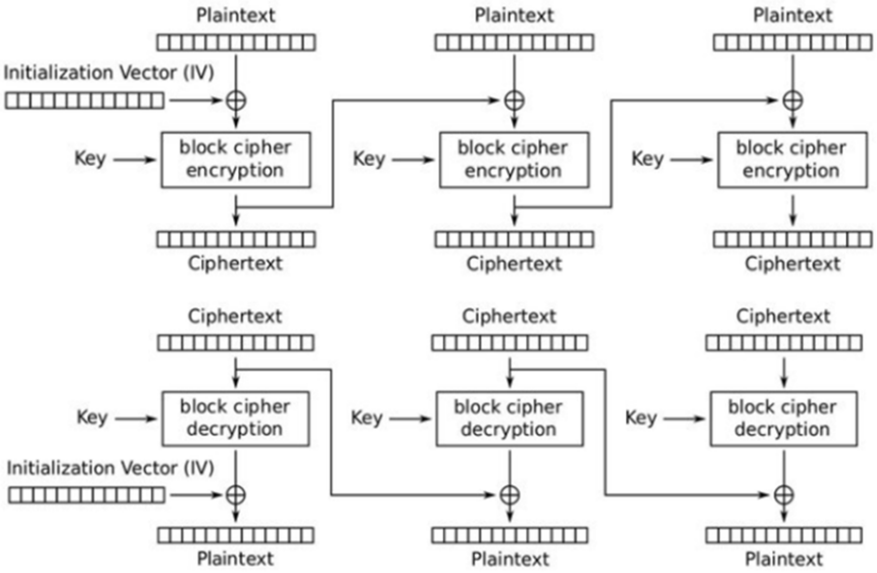


图 13-3: CBC 模式解密

13.1.2.3 对称加解密的多次调用

有时候需要对大量数据进行加解密的操作，但受限制与存储空间或者传输速率的影响，数据会被分为多批次进行处理，当需要多次调用对称加解密模块对一大段数据进行连续处理时就需要考虑到调用之间数据上下文的保存和维护。

ECB 模式：

ECB 模式对于每一组 16byte 数据进行单独的加解密操作的，对于单次加解密的数据，需要保证数据量为 16byte 的整数倍，多余的数据可以等到下一批数据准备好以后合并进行处理。

CTR 模式：

CTR 模式对于每一组 16byte 的数据均有对应的 NONCE 和 COUNTER 值，通常情况下，NONCE 为常数，COUNTER 为当前数据组的编号，数据组编号按每次加 1 递增。对于单次加解密的数据，上层软件调用时需要保证数据量为 16byte 的整数倍，同时根据数据量记录下 COUNTER 值，在下一次调用将累计的 COUNTER 值作为初始向量输入到对应的 IV 寄存器。多余的数据可以等到下一批数据准备好后合并进行处理。

CBC 模式：

CBC 模式的每组数据使用的初始向量均来自上一组数据的密文，对于单次加解密数据，上层软件调用时需要保证数据量为 16byte 的整数倍，同时需要记录下当前加解密操作最后一组数据的密文，在下一次操作时作为初始向量输入到对应的 IV 寄存器中。多余的数据则等到下一批数据准备好之后合并进行处理。

13.1.2.4 散列算法

散列算法包括 SHA1，SHA224，SHA256 和 SM3，不同算法的摘要长度不同。SHA1 摘要为 160bit，SHA224 为 224bit，SHA256 和 SM3 均为 256bit，碰撞性角度来说，摘要越长碰撞概率则会越低。

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13.1.2.5 散列值计算的多次调用

有时候需要对大量数据进行散列值计算，但受限于存储空间或者传输速率的影响，数据会被分为多批次进行处理。当需要多次调用散列值计算模块对一大段数据进行处理时，需要注意以下几点。

第一，除最后一次以外，每一次处理的数据量必须为 4byte 的整数倍，单次处理多余的数据需保存，与下一批次的数据进行合并处理。

第二，对于所有散列算法，每一次计算前需要将上一次散列计算的中间结果 H0~H7 写入对应的寄存器，然后设置散列值计算模块使用外部 H0~H7 的初始值并且装载入模块。

第三，每次调用 HASH 时需要将上一次结束时的 HASH LEN RESULT 更新到当前 HASH LEN 寄存器，并且装载入模块。

第四，除最后一次调用以外，需要设置散列值计算模块不使用 padding。

13.1.3 AES 寄存器

AES 的基地址是 0x5000D000。

表 13-1: AES 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**COMMAND**	
[31:5]			RSVD	
[4]	rw	1'h0	AUTO_GATE	auto clock gating
[3]	rw	1'h0	HASH_RESET	HASH_ACC soft reset, 1'h1: reset the HASH_ACC block
[2]	w1t	1'h0	HASH_START	write 1 to trigger the HASH_ACC block
[1]	rw	1'h0	AES_ACC_RESET	AES_ACC soft reset, 1'h1: reset the AES_ACC block
[0]	w1t	1'h0	START	write 1 to trigger the AES_ACC block
0x04			**STATUS**	
[31:3]			RSVD	
[2]	r	1'h0	HASH_BUSY	HASH_ACC block is busy
[1]	r	1'h0	FLASH_KEY_VALID	flash key valid indicator
[0]	r	1'h0	BUSY	AES_ACC block is busy
0x08			**IRQ**	
[31:22]			RSVD	
[21]	rw1c	1'h0	HASH_PAD_ERR_RAW_STAT	HASH_ACC padding error raw status
[20]	rw1c	1'h0	HASH_BUS_ERR_RAW_STAT	HASH_ACC bus error raw status
[19]	rw1c	1'h0	HASH_DONE_RAW_STAT	HASH_ACC done raw status
[18]	rw1c	1'h0	SETUP_ERR_RAW_STAT	AES_ACC setup error raw status
[17]	rw1c	1'h0	BUS_ERR_RAW_STAT	AES_ACC bus error raw status
[16]	rw1c	1'h0	DONE_RAW_STAT	AES_ACC done raw status
[15:6]			RSVD	
[5]	rw1c	1'h0	HASH_PAD_ERR_STAT	HASH_ACC padding error status
[4]	rw1c	1'h0	HASH_BUS_ERR_STAT	HASH_ACC bus error status
[3]	rw1c	1'h0	HASH_DONE_STAT	HASH_ACC done status
[2]	rw1c	1'h0	SETUP_ERR_STAT	AES_ACC setup error status
[1]	rw1c	1'h0	BUS_ERR_STAT	AES_ACC bus error status
[0]	rw1c	1'h0	DONE_STAT	AES_ACC done status
0x0C			**SETTING**	

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表 13-1: AES 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:6]			RSVD	
[5]	rw	1'h0	HASH_PAD_ERR_MASK	HASH_ACC padding error interrupt mask, 0: mask the interrupt
[4]	rw	1'h0	HASH_BUS_ERR_MASK	HASH_ACC bus error interrpt mask, 0: mask the interrupt
[3]	rw	1'h0	HASH_DONE_MASK	HASH_ACC done interrupt mask, 0: mask the interrupt
[2]	rw	1'h0	SETUP_ERR_IRQ_MASK	AES_ACC setup error interrupt mask, 0: mask the interrupt
[1]	rw	1'h0	BUS_ERR_IRQ_MASK	AES_ACC bus error interrupt mask, 0: mask the interrupt
[0]	rw	1'h0	DONE_IRQ_MASK	AES_ACC done interrupt mask, 0: mask the interrupt
0x10			**AES_SETTING**	
[31:9]			RSVD	
[8]	rw	1'h0	AES_BYPASS	1'h0: normal operation 1'h1: bypass
[7]	rw	1'h0	AES_OP_MODE	1'h0: decryption 1'h1: encryption
[6]	rw	1'h0	ALGO_STANDARD	1'h0: AES 1'h1: SM4
[5]	rw	1'h0	KEY_SEL	1'h0: select key from AES_ACC key registers 1'h1: use internal root key
[4:3]	rw	2'h0	AES_LENGTH	AES Length: 2'h0: 128-bit 2'h1: 192-bit 2'h2: 256-bit 2'h3: Reserved
[2:0]	rw	3'h0	AES_MODE	AES Mode: 3'h0: ECB 3'h1: CTR 3'h2: CBC Others: Reserved
0x14			**DMA_IN**	
[31:0]	rw	32'h0	ADDR	AES_ACC input data address
0x18			**DMA_OUT**	
[31:0]	rw	32'h0	ADDR	AES_ACC output data address
0x1C			**DMA_DATA**	
[31:28]			RSVD	
[27:0]	rw	28'h0	SIZE	AES_ACC data block size, AES_ACC only support block aligned transaction. Each block contains 16 bytes.
0x20			**IV_W0**	
[31:0]	rw	32'h0	DATA	Initial Vector Word0
0x24			**IV_W1**	
[31:0]	rw	32'h0	DATA	Initial Vector Word1
0x28			**IV_W2**	
[31:0]	rw	32'h0	DATA	Initial Vector Word2
0x2C			**IV_W3**	
[31:0]	rw	32'h0	DATA	Initial Vector Word3
0x30			**EXT_KEY_W0**	
[31:0]	rw	32'h0	DATA	External Key Word0
0x34			**EXT_KEY_W1**	
[31:0]	rw	32'h0	DATA	External Key Word1
0x38			**EXT_KEY_W2**	

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表 13-1: AES 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	DATA	External Key Word2
0x3c			**EXT_KEY_W3**	
[31:0]	rw	32'h0	DATA	External Key Word3
0x40			**EXT_KEY_W4**	
[31:0]	rw	32'h0	DATA	External Key Word4
0x44			**EXT_KEY_W5**	
[31:0]	rw	32'h0	DATA	External Key Word5
0x48			**EXT_KEY_W6**	
[31:0]	rw	32'h0	DATA	External Key Word6
0x4C			**EXT_KEY_W7**	
[31:0]	rw	32'h0	DATA	External Key Word7
0x50			**HASH_SETTING**	
[31:9]			RSVD	
[8]	w1t	1'h0	HASH_LEN_LOAD	write 1 to load hash length
[7]	w1t	1'h0	HASH_IV_LOAD	write 1 to load hash iv
[6]	rw	1'h0	RESULT_ENDIAN	hash result endian setting: 1'h0: little endian 1'h1: big endian
[5]	rw	1'h0	DFT_IV_SEL	HASH default iv select. 1'h0: default iv according to hash mode 1'h1: default iv from HASH_IV_H* registers
[4]	rw	1'h0	BYTE_SWAP	HASH byte swap option. Set 1 to swap byte order when read data from memory.
[3]	rw	1'h0	DO_PADDING	HASH padding enable. Set 1 to do padding after data transfer.
[2:0]	rw	3'h0	HASH_MODE	HASH Mode: 3'h0: SHA-1 3'h1: SHA-224 3'h2: SHA-256 3'h3: SM3 Others: Reserved
0x54			**HASH_DMA_IN**	
[31:0]	rw	32'h0	ADDR	input data address
0x58			**HASH_DMA_DATA**	
[31:0]	rw	32'h0	SIZE	HASH input data byte size.
0x5C			**HASH_IV_H0**	
[31:0]	rw	32'h0	DATA	HASH IV H0
0x60			**HASH_IV_H1**	
[31:0]	rw	32'h0	DATA	HASH IV H1
0x64			**HASH_IV_H2**	
[31:0]	rw	32'h0	DATA	HASH IV H2
0x68			**HASH_IV_H3**	
[31:0]	rw	32'h0	DATA	HASH IV H3
0x6C			**HASH_IV_H4**	
[31:0]	rw	32'h0	DATA	HASH IV H4
0x70			**HASH_IV_H5**	
[31:0]	rw	32'h0	DATA	HASH IV H5
0x74			**HASH_IV_H6**	

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表 13-1: AES 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	rw	32'h0	DATA	HASH IV H6
0x78			**HASH_IV_H7**	
[31:0]	rw	32'h0	DATA	HASH IV H7
0x7C			**HASH_RESULT_H0**	
[31:0]	r	32'h0	DATA	HASH result H0
0x80			**HASH_RESULT_H1**	
[31:0]	r	32'h0	DATA	HASH result H1
0x84			**HASH_RESULT_H2**	
[31:0]	r	32'h0	DATA	HASH result H2
0x88			**HASH_RESULT_H3**	
[31:0]	r	32'h0	DATA	HASH result H3
0x8C			**HASH_RESULT_H4**	
[31:0]	r	32'h0	DATA	HASH result H4
0x90			**HASH_RESULT_H5**	
[31:0]	r	32'h0	DATA	HASH result H5
0x94			**HASH_RESULT_H6**	
[31:0]	r	32'h0	DATA	HASH result H6
0x98			**HASH_RESULT_H7**	
[31:0]	r	32'h0	DATA	HASH result H7
0x9C			**HASH_LEN_L**	
[31:0]	rw	32'h0	DATA	HASH load length l
0xA0			**HASH_LEN_H**	
[31:29]			RSVD	
[28:0]	rw	29'h0	DATA	HASH load length h
0xA4			**HASH_RESULT_LEN_L**	
[31:0]	r	32'h0	DATA	HASH result length l
0xA8			**HASH_RESULT_LEN_H**	
[31:29]			RSVD	
[28:0]	r	29'h0	DATA	HASH result length h

13.2 TRNG

13.2.1 简介

TRNG 全称真随机数发生器（True Random Number Generator），该模块利用由数字逻辑组成的震荡电路来生成随机熵源，经过一系列校验生成了随机数种子，在通过伪随机数发生器由种子产生随机数提供给系统使用。

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13.2.2 模块架构

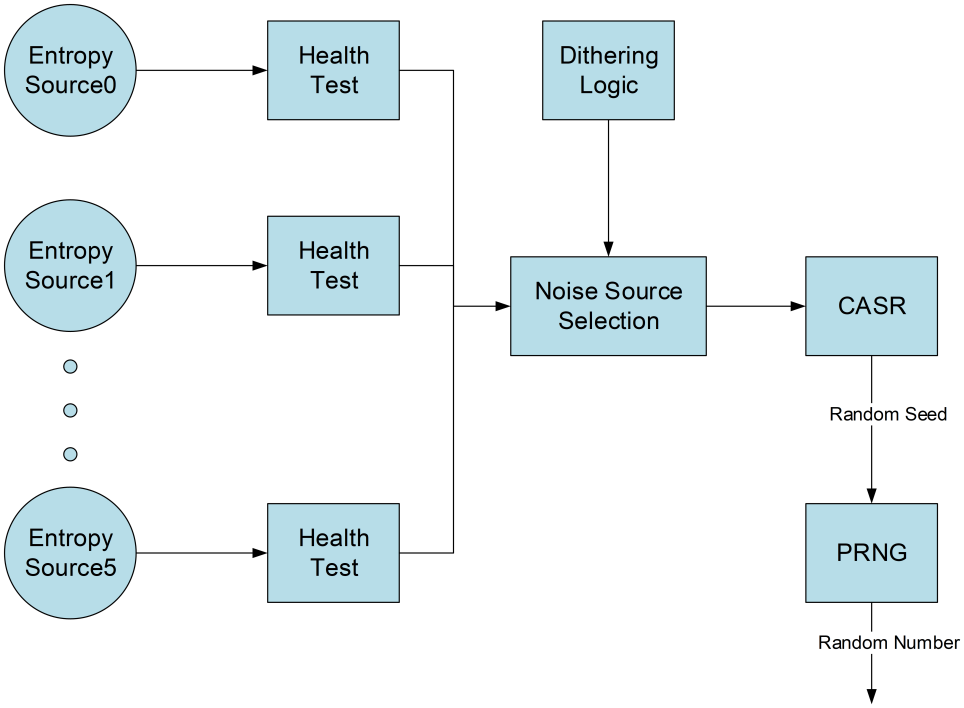


图 13-4: TRNG 结构图

真随机数发生器主要由 3 部分组成：熵源，随机种子发生器，随机数发生器。

13.2.3 功能描述

13.2.3.1 熵源

熵源由六条反相器链组成，每次产生新的随机种子的时候，都会启动所有反相器链，通过一定的校验算法生成随机数种子。随机数种子生成时间较长，同时消耗功耗也会较大，通常建议两种情况下重新生成新的种子，一种是原种子生命周期耗尽，需要定期生成新的种子覆盖，另一种是软件在特殊需求下手动生成新的种子。

熵源会在每次生成种子的时候启动，VN 校验器门限用来筛选熵源，门限越高则对于熵源筛选更宽松，生成种子速度更快，随机性会有所下降。

用户可以直接触发 gen_seed_start，启动熵源模块来生成新的随机种子。

13.2.3.2 随机种子发生器

随机种子发生器从熵源收集数据，通过 CASR(Cellular Automata Shift Register) 模块，生成随机种子，提供给下一级的 PRNG 使用。用户也可以通过寄存器直接获得随机种子。当用户配置 use_ext_seed 为 1 之后，下一级的 PRNG 模块，将不适用随机种子发生器产生的种子，转而使用外部种子来生成随机数。

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13.2.3.3 随机数发生器

随机数发生器是基于现有随机种子的伪随机数发生器，相对时间较短且固定。需要注意的是，伪随机数发生器有概率进入自锁状态，原因是内部一些数据序列导致了线性反馈寄存器的死锁，当检测到 prng_lockup 的状态时，建议重新生成一组随机种子来生成新的随机数。

用户可以触发 gen_rand_num_start 来启动随机数发生器，若当前随机种子没有生成，则随机数发生器会先生成随机种子，然后在生成随机数。

13.2.3.4 其他功能模块

TRNG 模块额外提供了反相器链的震荡周期测量，由此可以简介推断芯片所在的工艺角。具体过程首先要确定使用的反相器链编号，因为不同的反相器链长度不同，对应的震荡周期也不同，然后设置震荡的周期数，这个周期数对应的系统 pclk 对应的频率。开启测量后，会有两个计数器分别统计 pclk 的时钟周期和反相器链的时钟周期，当 pclk 的时钟周期数达到设置的阈值时就会停止。此时可以根据 pclk 的时钟频率 Fpclk，周期数 Npclk，还有反相器链的周期数 Ninv 推算出反相器链的频率 Finv=Fpclk*Npclk/Ninv。由此可以推断该芯片所对应的工艺角。

13.2.4 TRNG 寄存器

表 13-2: TRNG 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**CTRL**	
[31:5]			RSVD	
[4]	rw	1'h0	gen_rand_num_suspend	Set 1 to suspend random number generation and update. Set 0 to recover the process.
[3]	rw	1'h0	gen_rand_num_stop	Set 1 to stop random number generation and update. This will reset the random number generation engine. After release the stop bit, user should write 1 to gen_rand_num_start to trigger the random number engine.
[2]	rw	1'h0	gen_seed_stop	Set 1 to stop random seed generation. This will reset the random seed generation engine. After release the stop bit, user should write 1 to gen_seed_start to trigger the random seed engine.
[1]	w1t	1'h0	gen_rand_num_start	write 1 to trigger the random number generation engine
[0]	w1t	1'h0	gen_seed_start	write 1 to trigger the random seed generation engine
0x04			**STAT**	
[31:4]			RSVD	
[3]	r	1'h0	rand_num_valid	random number valid flag
[2]	r	1'h0	rand_num_gen_busy	random number engine busy flag
[1]	r	1'h0	seed_valid	random seed valid flag
[0]	r	1'h0	seed_gen_busy	random seed engine busy flag
0x08			**CFG**	
[31:16]			RSVD	
[15:8]	rw	8'ha	reject_threshold	random seed internal VN corrector check threshold
[7:2]			RSVD	
[1]	rw	1'h0	use_ext_seed	set 1 to use external seed to generate random number
[0]	rw	1'h0	auto_clock_enable	auto clock gating enable
0x0c			**IRQ**	
[31:19]			RSVD	

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表 13-2: TRNG 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[18]	rw	1'h1	prng_lockup_msk	prng lockup interrupt mask
[17]	rw	1'h1	rand_num_avail_msk	random number available interrupt mask
[16]	rw	1'h1	seed_gen_done_msk	random seed generation done interrupt mask
[15:3]			RSVD	
[2]	rw1c	1'h0	prng_lockup	prng lockup raw interrupt
[1]	rw1c	1'h0	rand_num_avail	random number available raw interrupt
[0]	rw1c	1'h0	seed_gen_done	random seed generation done raw interrupt
0x10			**rand_seed0**	
[31:0]	rw	32'h0	val	random seed value0. If using external random seed, write value to this register will update the random seed in use.
0x14			**rand_seed1**	
[31:0]	rw	32'h0	val	random seed value1. If using external random seed, write value to this register will update the random seed in use.
0x18			**rand_seed2**	
[31:0]	rw	32'h0	val	random seed value2. If using external random seed, write value to this register will update the random seed in use.
0x1c			**rand_seed3**	
[31:0]	rw	32'h0	val	random seed value3. If using external random seed, write value to this register will update the random seed in use.
0x20			**rand_seed4**	
[31:0]	rw	32'h0	val	random seed value4. If using external random seed, write value to this register will update the random seed in use.
0x24			**rand_seed5**	
[31:0]	rw	32'h0	val	random seed value5. If using external random seed, write value to this register will update the random seed in use.
0x28			**rand_seed6**	
[31:0]	rw	32'h0	val	random seed value6. If using external random seed, write value to this register will update the random seed in use.
0x2c			**rand_seed7**	
[31:0]	rw	32'h0	val	random seed value7. If using external random seed, write value to this register will update the random seed in use.
0x30			**rand_num0**	
[31:0]	r	32'h0	val	random number value0
0x34			**rand_num1**	
[31:0]	r	32'h0	val	random number value1
0x38			**rand_num2**	
[31:0]	r	32'h0	val	random number value2
0x3c			**rand_num3**	
[31:0]	r	32'h0	val	random number value3
0x40			**rand_num4**	
[31:0]	r	32'h0	val	random number value4
0x44			**rand_num5**	
[31:0]	r	32'h0	val	random number value5
0x48			**rand_num6**	
[31:0]	r	32'h0	val	random number value6
0x4c			**rand_num7**	
[31:0]	r	32'h0	val	random number value7
0x50			**cal_cfg**	

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表 13-2: TRNG 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:16]	rw	16'hff	length	calibration length
[15:6]			RSVD	
[5]	r	1'h0	done	calibration done
[4]	rw	1'h0	enable	calibration enable
[3:1]	rw	3'h0	osc_clk_sel	osc clock select
[0]	rw	1'h0	osc_clk_force_on	osc force enable
0x54			**cal_result**	
[31:16]	r	16'h0	osc_cnt	osc clock calibration counter result
[15:0]	r	16'h0	pclk_cnt	pclk calibration counter result

13.3 efusec

13.3.1 简介

efusec 即 efuse control, 通过写操作可控制 efuse 相应位的熔断，熔断后的 bit 信息读回为 1，通过读操作可读出所存储的信息值。

13.3.2 主要特性

- 可控制 4 块 256 bit 的 efuse 单元
- 可读\写 1024 bit 信息
- 每次可控制一个 efuse 单元的读\写操作
- 读\写操作为单 bit 串行
- 读\写完成可产生中断信号
- 可实现读写屏蔽功能
- 部分存储信息直接通过模块接口输出
- efuse 的默认值为全 0

13.3.3 写操作

efusec 的写操作就是对 efuse 的一个编程操作，写数据为 1 的 bit，通过熔断的方式将该 bit 设置为开路，使得读回的数据值为 1。写入的信息通过寄存器 PGM_DATA0~7 配置，四个单元共用 8 个 PGM_DATA* 寄存器。写操作的控制流程如下：

- 配置 BANKSEL 寄存器选择要写的 efuse 单元
- 配置 MODE 寄存器选择写操作
- 配置 IE 寄存器使能中断状态
- 配置 PGM_DATA* 寄存器写入编程数据
- 配置 TIMER 寄存器设置关键时长
- 配置 EN 寄存器启动写操作
- 等待中断到来或查询 SR 寄存器获得写完成状态

熔断的 bit 无法恢复到 0 状态，未熔断的 bit 可再次通过写操作进行熔断。

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13.3.4 读操作

eFusec 的读操作就是对 efuse 的存储信息进行读取，读出的存储信息可通过 BANK*_DATA* 寄存器查询，每个单元都有独立的寄存器进行数据查询。读操作的控制流程如下：

- 配置 BANKSEL 寄存器选择要读的 efuse 单元
- 配置 MODE 寄存器选择读操作
- 配置 IE 寄存器使能中断状态
- 配置 TIMER 寄存器设置关键时长
- 配置 EN 寄存器启动写操作
- 等待中断到来或查询 SR 寄存器获得读完成状态
- 读取 BANK*_DATA* 寄存器获得读取值
- 部分读取值直接通过接口信号送出

13.3.4.1 读写时间控制

efuse 的读写时序有一定要求，特别是熔断时间，当 efusec 模块的工作时钟变化时，需调整时钟的计数值以满足 efuse 的读写时序要求。需要进行时序控制的时间点有以下三个：

- TCKHP：单 bit 熔断时间，10us
- THPCK：启动写使能的保持时间，>20ns
- THRCK：启动读使能的保持时间，>500ns

通过 TIME 寄存器可配置这三个时间基于工作时钟的计数值。寄存器复位值为 48MHz 工作时钟下的计数值。

13.3.4.2 读写屏蔽功能

为了防止恶意的读写操作，在配置好数据后不再进行数据更新的情况下，可通过控制 bank0 的固定 bit 屏蔽 bank1~3 的 efuse 模块的读\写功能，屏蔽后无法对相应 efuse 进行写操作，也无法再更新读出的数值。

- bank0[255:254]=2’b11, 屏蔽 bank3 写功能；
- bank0[253:252]=2’b11, 屏蔽 bank3 读功能；
- bank0[251:250]=2’b11, 屏蔽 bank2 写功能；
- bank0[249:248]=2’b11, 屏蔽 bank2 读功能；
- bank0[247:246]=2’b11, 屏蔽 bank1 写功能；
- bank0[245:244]=2’b11, 屏蔽 bank1 读功能；

13.3.4.3 模块接口输出信号

efuse 的部分数值会通过模块接口信号输出，他们分别是：

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表 13-3: efuse 接口信号

序号	信号名
1	idsel
2	swddis
3	pkgid[1:0]
4	uid[127:0]
5	rootkey[255:0]

13.3.5 efusec 寄存器

表 13-4: efusec 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**CR**	Control Register
[31:5]			RSVD	
[4]	rw	1'h0	IE	Interrupt enable
[3:2]	rw	2'h0	BANKSEL	Bank select
[1]	rw	1'h0	MODE	0 - READ, 1 - PGM
[0]	w1s	1'h0	EN	Write 1 to enable PGM/READ. Self clear
0x04			**TIMR**	Timer Register
[31:21]			RSVD	
[20:10]	rw	11'h78	TCKHP	SCLK high period for PGM. Recommended value ~10us
[9:7]	rw	3'h0	THPCK	SCLK to CSB hold time into PGM mode. Recommended value > 20ns
[6:0]	rw	7'h6	THRCK	SCLK to CSB hold time into READ mode. Recmmended value > 500ns
0x08			**SR**	Status Register
[31:1]			RSVD	
[0]	rw1c	1'h0	DONE	Indicates PGM/READ done. Write 1 to clear
0x0C			**RSVDR**	Reserved Register
0x0C			RSVDR	
[31:0]			RSVD	
0x10			**PGM_DATA0**	Program Data0
[31:0]	rw	32'h0	DATA	
0x14			**PGM_DATA1**	Program Data1
[31:0]	rw	32'h0	DATA	
0x18			**PGM_DATA2**	Program Data2
[31:0]	rw	32'h0	DATA	
0x1C			**PGM_DATA3**	Program Data3
[31:0]	rw	32'h0	DATA	
0x20			**PGM_DATA4**	Program Data4
[31:0]	rw	32'h0	DATA	
0x24			**PGM_DATA5**	Program Data5
[31:0]	rw	32'h0	DATA	
0x28			**PGM_DATA6**	Program Data6
[31:0]	rw	32'h0	DATA	
0x2C			**PGM_DATA7**	Program Data7
[31:0]	rw	32'h0	DATA	
0x30			**BANK0_DATA0**	Bank0 Data0
[31:0]	r	32'h0	DATA	
0x34			**BANK0_DATA1**	Bank0 Data1

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表 13-4: efusec 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	r	32'h0	DATA	
0x38			**BANK0_DATA2**	Bank0 Data2
[31:0]	r	32'h0	DATA	
0x3C			**BANK0_DATA3**	Bank0 Data3
[31:0]	r	32'h0	DATA	
0x40			**BANK0_DATA4**	Bank0 Data4
[31:0]	r	32'h0	DATA	
0x44			**BANK0_DATA5**	Bank0 Data5
[31:0]	r	32'h0	DATA	
0x48			**BANK0_DATA6**	Bank0 Data6
[31:0]	r	32'h0	DATA	
0x4C			**BANK0_DATA7**	Bank0 Data7
[31:0]	r	32'h0	DATA	
0x50			**BANK1_DATA0**	Bank1 Data0
[31:0]	r	32'h0	DATA	
0x54			**BANK1_DATA1**	Bank1 Data1
[31:0]	r	32'h0	DATA	
0x58			**BANK1_DATA2**	Bank1 Data2
[31:0]	r	32'h0	DATA	
0x5C			**BANK1_DATA3**	Bank1 Data3
[31:0]	r	32'h0	DATA	
0x60			**BANK1_DATA4**	Bank1 Data4
[31:0]	r	32'h0	DATA	
0x64			**BANK1_DATA5**	Bank1 Data5
[31:0]	r	32'h0	DATA	
0x68			**BANK1_DATA6**	Bank1 Data6
[31:0]	r	32'h0	DATA	
0x6C			**BANK1_DATA7**	Bank1 Data7
[31:0]	r	32'h0	DATA	
0x70			**BANK2_DATA0**	Bank2 Data0
[31:0]	r	32'h0	DATA	
0x74			**BANK2_DATA1**	Bank2 Data1
[31:0]	r	32'h0	DATA	
0x78			**BANK2_DATA2**	Bank2 Data2
[31:0]	r	32'h0	DATA	
0x7C			**BANK2_DATA3**	Bank2 Data3
[31:0]	r	32'h0	DATA	
0x80			**BANK2_DATA4**	Bank2 Data4
[31:0]	r	32'h0	DATA	
0x84			**BANK2_DATA5**	Bank2 Data5
[31:0]	r	32'h0	DATA	
0x88			**BANK2_DATA6**	Bank2 Data6
[31:0]	r	32'h0	DATA	
0x8C			**BANK2_DATA7**	Bank2 Data7
[31:0]	r	32'h0	DATA	
0x90			**BANK3_DATA0**	Bank3 Data0
[31:0]	r	32'h0	DATA	
0x94			**BANK3_DATA1**	Bank3 Data1

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表 13-4: efusec 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:0]	r	32'h0	DATA	
0x98			**BANK3_DATA2**	Bank3 Data2
[31:0]	r	32'h0	DATA	
0x9C			**BANK3_DATA3**	Bank3 Data3
[31:0]	r	32'h0	DATA	
0xA0			**BANK3_DATA4**	Bank3 Data4
[31:0]	r	32'h0	DATA	
0xA4			**BANK3_DATA5**	Bank3 Data5
[31:0]	r	32'h0	DATA	
0xA8			**BANK3_DATA6**	Bank3 Data6
[31:0]	r	32'h0	DATA	
0xAC			**BANK3_DATA7**	Bank3 Data7
[31:0]	r	32'h0	DATA	
0xB0			**ANACR**	Bank3 Data7
[31:24]	r	8'h0	RESERVE1	
[23:16]	rw	8'h0	RESERVE0	
[15:11]			RSVD	
[10:8]	rw	3'h0	LDO_DC_TR	
[7:5]			RSVD	
[4]	rw	1'h0	LDO_MODE	
[3:1]	rw	3'h4	LDO_VREF_SEL	
[0]	rw	1'h0	LDO_EN	
0xB4			**DB_SEL**	debug signal select
[31:0]	rw	32'h0	db_sel	debug signal select

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14 存储接口

14.1 SD/SDIO/eMMC

HPSYS 有 2 个 SDMMC。

14.1.1 简介

SDMMC 支持 SD 协议 3.0 以及 eMMC 标准 4.51，可作为 HOST 控制器与 SD/SDIO/eMMC 设备交互，并与 DMAC 配合进行数据读写。SDMMC 支持 SDR 单线和 4 线模式，不支持 DDR，不支持 SPI 模式。

14.1.2 主要特性

- 兼容 SD Host Controller Standard Specification Version 3.0
- 兼容 SD 3.0 Physical Layer Specification Version 3.01
- 兼容 SDIO Specification Version 3.0
- 兼容 JEDEC JESD84-B451 eMMC 4.51 Specification
- 支持 SDSC/SDHC/SDXC/SDHS 卡
- 支持 SDR12/SDR25/SDR50
- 支持 SDR 单线、4 线模式
- 内置 2K 字节 FIFO，最大支持单 block 512 字节
- 可配置时钟
- 配合 DMAC 进行数据搬运

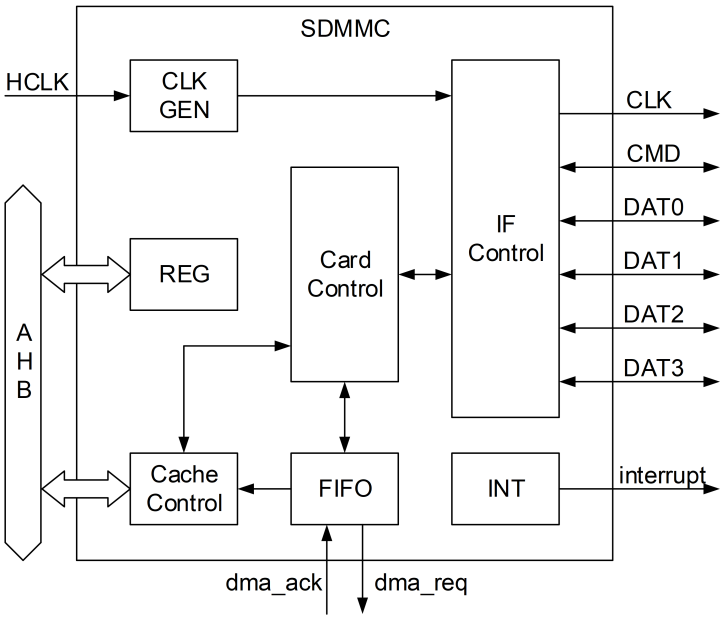


图 14-1: SDMMC 结构图

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14.1.3 功能描述

14.1.3.1 SD/eMMC 接口

控制器支持的 SD/eMMC 接口共包括一根 CLK 线，一根 CMD 线和 4 根 DAT 线 (DAT0-DAT3)。单线模式下 DAT 线仅使用一根 (DAT0)。CLK 线用于输出时钟。CMD 线依照协议打包传输 CMD 命令以及应答 RSP。DAT 线依照协议传输数据流。本模块仅支持单边沿 (SDR) 传输，CMD 与 DAT 仅在 CLK 的上升沿有效。

14.1.3.2 时钟设置

控制器工作在系统时钟 HCLK 频率上。输出到 SD/eMMC 接口的 CLK 是由 HCLK 分频产生，分频比由 CLKCR_DIV 指定。分频公式为 CLK 频率 =HCLK 频率/(CLKCR_DIV+1)。例如当 HCLK 为 48M，要输出 400KHz 的 CLK，就需要将 CLKCR_DIV 配置成 119。CLKCR_DIV 最小支持设置为 1，即分频比至少为 2。

CLK 输出由 CLKCR_STOP_CLK 控制，设置为 0 以后时钟会持续输出，设置为 1 关闭输出。

14.1.3.3 发送命令

命令是由控制器通过 CMD 线发送，由 SD/eMMC/SDIO 设备接收的固定格式的包，用于配置 SD/eMMC/SDIO 设备的状态，并控制数据的传输。命令的包长度固定为 48bit。

命令包格式						
Bit position	47	46	[45:0]	[39:8]	[7:1]	0
Width(bits)	1	1	6	32	7	1
Value	0	1	x	x	x	1
Description	Start bit	Transimission bit	Command index	Argument	CRC7	End bit

每条命令通过 6bit 的命令编号区分不同功能，并附带 32bit 的参数。设备通过 7bit CRC 判断接收到的命令是否正确，并在需要回复时发送响应。

根据 6bit 的命令编号，命令通常被命名为 CMDn，其中 n 就是命令编号，由 CCR_CMD_INDEX 寄存器配置。

命令的 32bit 参数由 CAR 寄存器配置。

某些命令如 CMD0，CMD4 等不需要接收响应；某些命令如 CMD8,CMD11 等需要接收 48bit 的响应；某些命令如 CMD2 需要接收 136bit 的响应。发送命令前，需要通过配置 CCR_CMD_HAS_RSP 和 CCR_CMD_LONG_RSP 寄存器选择命令期望的响应。

响应配置				
响应	CMD 示例	RSP 示例	CCR_CMD_HAS_RSP	CCR_CMD_LONG_RSP
无	CMD0，CMD4	无	0	0
48bit	CMD8，CMD11	R1,R7	1	0
136bit	CMD2，CMD9	R2	1	1

控制器每次发送命令前，需要将命令的各项配置完成，并置位 CCR_CMD_TX_EN，随后置位 CMD_START，控制器就会启动命令发送流程。

命令发送流程有两种结束方式：

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1. 命令完成，SR_CMD_DONE 拉高，且当 IER_CMD_DONE_MASK 为 1 时可产生中断。当命令发送完成且不需要接收响应，或者在超时时间以内接收到响应，不论响应的 CRC 是否正确，均会完成命令。如果接收响应出现 CRC 错误，SR_CMD_RSP_CRC 会拉高，且当 IER_CMD_RSP_CRC_MASK 为 1 时可产生中断。

2. 命令超时，SR_CMD_TIMEOUT 拉高，且当 IER_CMD_TIMEOUT_MASK 为 1 时可产生中断。当命令发送完成且需要接收响应，但在 TOR 寄存器配置的超时时间以内没有接收到响应 (未收到响应的 start bit)，会产生超时。一旦发生命令超时，控制器在发送下一条命令前需要被复位 (通过 RCC 模块)，并恢复配置 (仅需重新配置 SDMMC 控制器，与设备交互的状态不需改变)。

通过 SR_CMD_BUSY 可以查询命令发送流程是否完成。当前一条命令发送流程未结束时，控制器不响应新的命令发送请求。调试过程中，如果发现 SR_CMD_BUSY 长时间不拉低，请检查 TOR 设置是否合理，并检查上一条命令超时以后是否进行了控制器复位和重配置操作。

某些命令在期望响应 (如 R1b) 时，还需要检查设备通过 DAT 线反馈的 busy 状态，可以通过查询 DSR 寄存器判断 busy 是否撤销。

控制器接收到响应的 command index 保存在 RIR 寄存器中，argument 保存在 RAR1 RAR4 中，其中 48bit 响应的 argument 保存在 RAR1 中。

命令发送的建议流程：1. 配置 index，argument 以及期望响应类型，启动命令发送
2. 等待命令完成中断或命令超时中断
3. 如果命令完成，检查返回的响应并获取 argument
4. 如果命令超时，复位控制器并重新配置 (主要包括时钟设置和超时时间等)。

14.1.3.4 数据传输

数据传输包括从设备读取数据和向设备写入数据，由控制器发送特定命令 (如 CMD17，CMD24 等) 启动，数据传输预设长度后结束，或由控制器发送特定命令 (如 CMD12) 结束。

SD 和 SDIO 协议定义的数据传输可采用单线或 4 线模式。eMMC 协议定义的数据传输可采用单线，4 线或 8 线模式。本控制器只支持单线或 4 线传输，通过 DCR_WIRE_MODE 寄存器配置。单线模式下，数据通过 DAT0 传输，DAT0 也同时用于表示数据传输的 busy 状态。4 线模式下，数据通过 DAT0~DAT3 传输，DAT0 也同时用于表示数据传输的 busy 状态。

数据采用分块传输的形式，每块的数据量根据设备类型有所不同。对于 SD 和 eMMC 设备，单块数据量通常为 512byte，但也有例外。某些设备允许通过命令 (如 CMD16) 改变单块数据量。控制器在开始数据传输前，应当根据单块数据量将 DCR_BLOCK_SIZE 寄存器配置成相应值 (单块数据字节数等于 DCR_BLOCK_SIZE 加 1)。控制器还需配置 DLR_DATA_LEN 寄存器来确定单次数据传输的总量 (总字节数等于 DLR_DATA_LEN 加 1)。对于单块传输，DLR_DATA_LEN 应等于 DCR_BLOCK_SIZE。对于多块传输，(DLR_DATA_LEN+1) 应当为 (DCR_BLOCK_SIZE+1) 的整数倍。

数据传输的方向由 DCR_R_WN 配置。DCR_TRAN_DATA_EN 寄存器是数据传输使能，在传输过程中应当保持为高。DCR_DATA_START 用于启动数据传输。

数据传输需经过控制器内部的 FIFO 缓存。待发送的数据由 CPU 或 DMA 向 FIFO 写入，随后控制器再将 FIFO 中的数据写入到设备。从设备读取的数据也暂存在 FIFO 中，再由 CPU 或 DMA 取出。FIFO 的寄存器地址空间共占据 512byte，访问其中任何一个 word 对齐的地址效果相同。如果 FIFO 发生了上溢出或下溢，会产生 SR_FIFO_OVERRUN 或 SR_FIFO_UNDERRUN 记录，并可产生中断。

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数据传输有可能正常结束，也可能在规定时间内未收到数据或 CRC 而产生超时。不论发生哪种情况，SR_DATA_DONE 都会拉高，并可产生中断。如果读设备时读取 CRC 错误，或者写设备时，设备返回了 CRC 错误，都会产生 SR_DATA_CRC 记录。如果读设备时在 TOR 配置的超时时间内未检测到数据起始位，或写设备时在 TOR 配置的超时时间内未收到设备返回的 CRC 响应，都会产生 SR_DATA_TIMEOUT 记录。

通过 SR_DATA_BUSY 可以查询数据传输是否完成。当前一次数据传输未结束时，控制器不响应新的数据传输请求。

数据读取的建议流程：1. 配置单块数据量和总数据量，启动数据读取
2. 配置 DMAC 为读取 FIFO，并启动 DMAC
3. 发送读命令 (如 CMD17)
4. 等待命令中断，处理设备响应 (如 R1)
5. 等待数据传输完成中断
6. 如果是多块读取，发送传输结束命令 (如 CMD12)
7. 等待 DMA 完成中断

数据写入的建议流程：1. 发送写命令 (如 CMD24)
2. 等待命令中断，处理设备响应 (如 R1)
3. 配置单块数据量和总数据量，启动数据写入
4. 配置 DMAC 为写入 FIFO，并启动 DMAC
5. 等待数据传输完成中断
6. 如果是多块写入，发送传输结束命令 (如 CMD12)

14.1.3.5 中断产生

SDMMC 能够产生中断，用于通知 CPU 特定事件发生。这些事件包括命令发送完成，命令超时，数据完成，数据超时，以及各种错误等。能够产生中断的事件通过 IER 寄存器配置。发生的事件通过 SR 寄存器查询。

14.1.3.6 FIFO 管理

SDMMC 内置 2KB 大小的 FIFO 用于缓存读写数据。FIFO 能够根据内容的空满情况产生 DMA 请求，与 DMAC 配合完成数据搬运。在多块数据传输时，DMAC 搬运数据的带宽通常能够满足设备数据传输的带宽，因此能够持续进行数据传输。但如果 DMAC 搬运的另一端存储空间发生了堵塞，导致没有及时响应 FIFO 的请求，就可能使得 FIFO 产生 overflow 或 underflow，数据传输出错。为避免这种情况发生，可以设置 CLKCR_VOID_FIFO_ERROR 寄存器，使得当 FIFO 内容无法满足数据传输要求时，自动停止接口 CLK，并停止数据传输，直到 FIFO 内容满足要求为止，此时会在接口上观察到 CLK 的暂停。

14.1.3.7 eMMC 开漏模式

当 eMMC 设备处于某些状态 (如 inactive，idle，identification 状态，详见 eMMC 协议) 时，CMD 线需要配置成开漏模式，通过将 CDR_CMD_OD 配置成 1 实现。

当访问 SD/SDIO 设备时，以及当 eMMC 进入其它状态时，需要将 CMD 线配置成推挽模式，即 CDR_CMD_OD 配置成 0。

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14.1.3.8 SDIO 中断

SDIO 设备可以通过拉低 DAT1 产生 SDIO 中断通知控制器。

如果控制器需要响应 SDIO 中断，单线模式下需要将 CEATA_ENABLE_SDIO_IRQ 寄存器配置为 1。4 线模式下需要额外将 CEATA_SDIO_4WIRES_IRQ 配置为 1。

4 线模式下，不支持 CMD53 多块数据传输间隔内的中断请求 (Block Gap Interrupt)。单次 CMD 数据传输前或传输完成后的中断请求可以正常被响应。

14.1.3.9 卡片检测

SD 卡支持热拔插。卡片的插入与弹出检测通常有以下 3 种方式实现。

1. 通过专用 CD(card detect) 管脚检测。支持插入检测的 SD 卡槽通常提供一个专用的卡片检测管脚 (CD)，该管脚与电源间存在上拉电阻。芯片需要分配一个独立 IO 用于检测该管脚电平。当没有插入 SD 卡时，该管脚电平为高。当 SD 卡片插入卡槽时，该管脚与地导通，电平为低。通过判断该 IO 的 GPIO 输入电平，可以实现 SD 卡的插入与弹出检测。

2. 通过 DAT3 管脚检测。SD 卡上电时，卡片内部的 DAT3 到电源有 50K 欧姆的上拉电阻。芯片外部电路需要在 DAT3 管脚上放置到地的弱下拉电阻 (通常需大于 470K 欧姆)。芯片通过检测与 DAT3 相连接的 IO 电平，判断卡片是否插入。当没有插入 SD 卡时，该管脚电平为低。当 SD 卡片插入卡槽时，该管脚被上拉到高电平。通过判断该 IO 的 GPIO 输入电平，可以实现 SD 卡的插入与弹出检测。SD 卡启动数据传输时，应当停止该检测，将 DAT3 作为正常数据线使用。

3. 通过命令轮询检测。芯片每隔一段时间向 SD 卡发起命令交互，根据命令是否得到响应判断卡片是否存在。

SDMMC 仅支持通过 DAT3 进行卡片检测。SR_CARD_EXIST 根据 DAT3 的电平报告卡片是否存在，而卡片的插入和拔出事件通过 SR_CARD_INSERT 和 SR_CARD_REMOVE 报告，并可产生中断。

14.1.3.10 总线直接读取模式

SDMMC 允许将 SD 卡的数据空间映射到 AHB 总线上，使得其它主控模块能够通过 AHB 总线直接访问地址的方式读取 SD 卡的数据。在使用这个功能前，SDMMC 需要首先将 SD 卡配置进入数据传输模式。随后当总线上有对映射空间的读访问时，SDMMC 自动向 SD 卡发出命令并读取多块数据，将数据保存在内置缓存内 (与 FIFO 共享存储空间)，并通过总线返回数据。如果后续总线要读取的数据位于缓存内，SDMMC 不会发起新的读取命令，而是直接返回缓存内的结果。

14.1.3.11 采样时钟调节

SDMMC 与设备通信时，需要在 CLK 的上升沿采样从设备输入的 CMD 与 DAT 信号。由于信号传输存在时延，可能需要调节采样时钟的边沿以保证采样正确。CLKCR_CLK_TUNE_SEL 寄存器可以用来向后调节采样时钟的边沿，共有 4 档，可根据产品的实际情况调整。当 CLK 频率大于 50M 时，往往需要调节采样时钟以保证接口功能正确。

14.1.4 SDMMC 寄存器

SDMMC1 的基地址是 0x50045000。SDMMC2 的基地址是 0x50046000。

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表 14-1: SDMMC 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**SR**	command and data status register
[31:18]			RSVD	
[17]	rw	1'h0	cache_err	Detect cache error Read 1: cache error occur Read 0: no cache error Write 1: clear the bit Write 0: no any influence to the bit
[16]	rw	1'h0	sdio	Detect SDIO Card Interrupt Read 1: detect sdio card generating interrupt Read 0: no interrupt Write 1: clear the bit Write 0: no any influence to the bit
[15]	r	1'h0	card_exist	Card exist status Read 1: card exist Read 0: no card exist This bit will be valid after enable detect card.
[14]	rw	1'h0	card_remove	Detect card removed Read 1: detect card removed. When detect card inserted bit is set, the bit will also be back to 0 Read 0: no meaning Write 1: clear the bit Write 0: no any influence to the bit
[13]	rw	1'h0	card_insert	Detect card inserted Read 1: detect card inserted. When detect card removed bit is set, the bit will also be back to 0 Read 0: no meaning Write 1: clear the bit Write 0: no any influence to the bit
[12]	rw	1'h0	cmd_sent	Command sent (perhaps no response back yet) Read 1: command sent. When command start bit is set, the bit will also be back to 0 Read 0: command transferring or others Write 1: clear the bit Write 0: no any influence to the bit
[11]			RSVD	
[10]	rw	1'h0	fifo_overrun	FIFO overrun Read 1: FIFO overrun error Read 0: no FIFO overrun error Write 1: clear the bit Write 0: no any influence to the bit
[9]	rw	1'h0	fifo_underrun	FIFO underrun Read 1: FIFO underrun error Read 0: no FIFO underrun error Write 1: clear the bit Write 0: no any influence to the bit

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表 14-1: SDMMC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[8]	rw	1'h0	startbit_error	Wide bus start bits error Didn't detect all start bits in data bus Read 1: start bits error Read 0: no start bits error Write 1: clear the bit Write 0: no any influence to the bit
[7]	rw	1'h0	data_timeout	Data timeout Read 1: timeout Read 0: no timeout Write 1: clear the bit Write 0: no any influence to the bit
[6]	rw	1'h0	data_crc	Data CRC error Read 1: data CRC error Read 0: data CRC right Write 1: clear the bit Write 0: no any influence to the bit
[5]	rw	1'h0	data_done	Data transfer done Read 1: transfer data done, and start a new transfer will take the bit into 0 Read 0: data transferring or idle Write 1: clear the bit Write 0: no any influence to the bit
[4]	r	1'h0	data_busy	Transfer Data busy 1: busy, and when busy, start transfer data bit is no usage and you should not modify the relative register. If want to do this, first disable transfer data enable bit, then the busy bit will be back to 0, and this transfer will also be cancelled. 0: data idle
[3]	rw	1'h0	cmd_timeout	Command timeout (response timeout) Read 1: timeout Read 0: no timeout Write 1: clear the bit Write 0: no any influence to the bit
[2]	rw	1'h0	cmd_rsp_crc	Command response CRC error status Read 1: response CRC error Read 0: response CRC right Write 1: clear the bit Write 0: no any influence to the bit
[1]	rw	1'h0	cmd_done	Command done Read 1: transfer command done, and start a new transfer will take the bit into 0 Read 0: command transferring or idle Write 1: clear the bit Write 0: no any influence to the bit
[0]	r	1'h0	cmd_busy	Command busy 1: busy, and when busy, start TX command bit is no usage and should not modify the relative register 0: command idle
0x04			**CCR**	command control register
[31:24]			RSVD	
[23:18]	rw	6'h0	cmd_index	Command index

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表 14-1: SDMMC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[17]	rw	1'h0	cmd_long_rsp	1: Response will be 136-bit, long response 0: Response will be 48-bit, normal response
[16]	rw	1'h1	cmd_has_rsp	1: Response expected after command 0: No response expected after command
[15:10]			RSVD	
[9]	rw	1'h0	cmd_pend	Command pending enable When prepare to send stop command, this bit should be set. Controller will calculate a proper time point to send out the command to guarantee all the data have been transferred. And this is mainly used in stream mode. Recommend using set_block_count (SD/MMC basis command) to control transferring data for block mode. If send stop command for canceling this transfer (such as CRC error in multi-block), no need to set the bit.
[8]	rw	1'h0	cmd_tx_en	TX command enable 1: enable TX command 0: disable TX command
[7:1]			RSVD	
[0]	rw	1'h0	cmd_start	Command start write 1 to start command TX, and when begin to TX command, the bit will return into 0.
0x08			**CAR**	command argument register
[31:0]	rw	32'h0	cmd_arg	Command argument
0x0C			**RIR**	response command index register
[31:6]			RSVD	
[5:0]	r	6'h0	rsp_index	Response command index
0x10			**RAR1**	response command argument1 register
[31:0]	rw	32'h0	rsp_arg1	Response command content If long response, it is rsp_arg[39:8]
0x14			**RAR2**	response command argument2 register
[31:0]	rw	32'h0	rsp_arg2	Long response, it is rsp_arg[71:40]
0x18			**RAR3**	response command argument3 register
[31:0]	rw	32'h0	rsp_arg3	Long response, it is rsp_arg[103:72]
0x1C			**RAR4**	response command argument4 register
[31:24]			RSVD	
[23:0]	rw	24'h0	rsp_arg4	Long response, it is rsp_arg[127:104]
0x20			**TOR**	timeout count register
[31:0]	rw	32'h1000	timeout_cnt	Used to determine how much time waiting response or data bus busy is timeout, and decreased under card clock. Set to 400000 for 1s timeout if interface clock is 400KHz.
0x24			**DCR**	data control register
[31:27]			RSVD	
[26:16]	rw	11'h1ff	block_size	Data block size is block_size+1 (max 2048 bytes) 0: 1 byte 0x1ff: 512 bytes
[15:13]			RSVD	
[12:11]	rw	2'h0	wire_mode	Wide data bus mode 00: 1 wire bus 01: 4 wires wide bus 1X: reserved

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表 14-1: SDMMC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[10]	rw	1'h0	stream_mode	Data transfer mode 0: block 1: stream
[9]	rw	1'h0	r_wn	Write or read 0: write data into card 1: read data from card
[8]	rw	1'h0	tran_data_en	Transfer data enable 0: disable transfer data. After disable data transfer, stop command should be sent to card 1: enable data transfer
[7:1]			RSVD	
[0]	rw	1'h0	data_start	Start transfer data set 1 to let the controller begin to transfer data (in fact, go into wait write or wait read state). After begin to transfer, this bit will be back to 0.
0x28			**DLR**	data length register
[31:16]	r	16'h0	block_tran_num	The number of blocks which have been transferred successfully 1 = 1 block transferred It is cleared when start transfer data bit is set.
[15:0]	rw	16'h1ff	data_len	Data length value. The number of data bytes is data_len+1. The number of data bytes should be a multiple of data block size. 0 is 1 byte. 0x1ff is 512 bytes. Max is 63.5KB.
0x2C			**IER**	command and data interrupt mask register
[31:18]			RSVD	
[17]	rw	1'h1	cache_err_mask	cache error mask for interrupt
[16]	rw	1'h0	sdio_mask	Detect SDIO interrupt(data[1]) mask for interrupt
[15]			RSVD	
[14]	rw	1'h0	card_remove_mask	Detect card remove mask for interrupt
[13]	rw	1'h0	card_insert_mask	Detect card insert mask for interrupt
[12]	rw	1'h0	cmd_sent_mask	Command sent mask for interrupt
[11]			RSVD	
[10]	rw	1'h1	fifo_overrun_mask	FIFO overrun bit mask for interrupt
[9]	rw	1'h1	fifo_underrun_mask	FIFO underrun bit mask for interrupt
[8]	rw	1'h0	startbit_error_mask	Wide bus start bits error bit mask for interrupt
[7]	rw	1'h1	data_timeout_mask	Data timeout bit mask for interrupt
[6]	rw	1'h1	data_crc_mask	Data CRC error bit mask for interrupt
[5]	rw	1'h1	data_done_mask	Data transfer done bit mask for interrupt
[4]			RSVD	
[3]	rw	1'h1	cmd_timeout_mask	Command timeout bit mask for interrupt
[2]	rw	1'h1	cmd_rsp_crc_mask	Command CRC error bit mask for interrupt
[1]	rw	1'h1	cmd_done_mask	Command done bit mask for interrupt
[0]			RSVD	
0x30			**CLKCR**	clock control register
[31:21]			RSVD	
[20:8]	rw	13'h80	div	Divide card clock counter. 0 is illegal. sd_clock = hclk/(div + 1) If hclk is 240M and div is 599, 400KHz SD clock will be generated.
[7:4]			RSVD	

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表 14-1: SDMMC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[3:2]	rw	2'h0	clk_tune_sel	select clock delay for rx sample 0: no delay 1: delay level 1 (~1.5ns typical) 2: delay level 2 (~3ns typical) 3: delay level 3 (~5ns typical)
[1]	rw	1'h0	void_fifo_error	Void FIFO error 0: close the function 1: open the function If open it, when FIFO will be overrun or underrun soon, the SD_CLK and the clock enable of this module will be closed, and wait to host to read or write FIFO. Note: this function needs to be supported by card.
[0]	rw	1'h1	stop_clk	Disable SD card clock 1: stop SD card clock 0: SD card clock generated
0x3C			**CDR**	card interface control and card detect register
[31:19]	rw	13'h0	otiming	define output timing
[18:6]	rw	13'h0	itiming	define input timing
[5]	rw	1'h0	cmd_od	Open Drain mode for cmd line (for eMMC identification mode) 0: cmd line is push-pull 1: cmd line is open-drain
[4]	rw	1'h1	cd_hvalid	Card detect high level valid 0: detect low level means card exist 1: detect high level means card exist (default)
[3]	rw	1'h1	en_cd	Enable card detect Only when the bit is valid, controller does card detect. If use sd_data[3] to do card detect, the bit should be cleared when transfer valid data.
[2]	rw	1'h0	otiming_sel	select output timing (according to otiming config)
[1]	rw	1'h0	itiming_sel	select input sample timing (according to itiming config)
[0]	rw	1'h1	sd_data3_cd	Use sd_data[3] to do card detect 0: use special pin to do card detect / write protect. (Currently not supported) 1: use sd_data[3] to do card detect (default)
0x40			**DBGR1**	card debug port1 register
[31]			RSVD	
[30:16]	r	15'h1	data_st	data state for debug only
[15:0]	r	16'h1	cmd_st	command state for debug only
0x44			**DBGR2**	card debug port2 register
[31:30]	rw	2'h0	dbg_sel	for debug only
[29:26]			RSVD	
[25:16]	r	10'h0	valid_data_cou	for debug only
[15:14]			RSVD	
[13:0]	r	14'h0	host_word_counter	for debug only
0x48			**CEATA**	CE-ATA/SDIO mode register
[31:4]			RSVD	
[3]	rw	1'h0	sdio_4wires_multi_irq	Select the sdio host 4 wires interrupt on multi-block support 0: host not support 4 wires interrupt on multi-block data transfers 1: host support 4 wires interrupt on multi-block data transfers

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表 14-1: SDMMC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[2]	rw	1'h0	sdio_4wires_irq	Select the sdio host 4 wires interrupt support 0: host not support 4 wires interrupt on single-block data transfers 1: host support 4 wires interrupt on single-block data transfers
[1]	rw	1'h0	enable_sdio_irq	Select the sdio card mode, default is sd card 0: sd card mode , no sdio card interrupt 1: sdio card mode , enable sdio card interrupt
[0]	rw	1'h0	ata_mode	Select the card type, default is sd card 0: sd card mode 1: CE-ATA device mode
0x54			**DSR**	data status register
[31:8]			RSVD	
[7:0]	r	8'h0	sd_data_i_ll	The status of each sd data pad status
0x58			**CDCR**	clock duty cycle register
[31:1]			RSVD	
[0]	rw	1'h1	clk_config	1: the sd clock is 50% duty cycle 0: the high level of the sd clock is 1 hclk cycle
0x5C			**CASR**	cache status register
[31:4]			RSVD	
[3]	rw1s	1'h0	cache_flush	Set 1 to flush cache. Should set when cache not busy.
[2]	r	1'h0	cache_busy	Indicates cache is working
[1]	rw1c	1'h0	sd_busy	Read 1 indicates sd is ready for normal access. Ahb access will be hold during sd_busy asserted. After sd normal access done, write 1 to clear, and ahb access will continue
[0]	rw1s	1'h0	sd_req	Set 1 to request sd normal access. sd_req will be cleared automatically after sd_busy asserted
0x60			**CACR**	cache control register
[31]	rw	1'h1	cache_en	enable cache 1: ahb read will return cached data 0: ahb read always return dummy data with no error response
[30]	rw	1'h1	cache_to_en	enable ahb read timeout recover
[29]	rw	1'h0	cache_force_read	force cache read done 1: start new fetch for miss access only after cache read done 0: start new fetch for miss access even when cache is still filling (read will be breaked by cmd12)
[28]	rw	1'h1	cache_sdsc	select card version 1: card size <=2GB, address of cmd18 is in byte 0: card size >2GB, address of cmd18 is in block
[27]	rw	1'h0	cache_nocrc	1: return ahb data without crc check 0: return ahb data after block crc pass
[26]	rw	1'h0	cache_hresp	1: generate ahb error response when error occur 0: no ahb error response generated. Could check cache_err interrupt
[25:24]			RSVD	
[23:20]	rw	4'h8	cache_pref_block	cache prefetch depth is cache_pref_block blocks. Should be no less than cache_block
[19]			RSVD	
[18:16]	rw	3'h4	cache_block	cache depth is cache_block blocks
[15]	rw	1'h0	stop_long_rsp	Stop response is 136-bit, long response
[14]	rw	1'h1	stop_has_rsp	Stop command have a response
[13:8]	rw	6'h0c	stop_index	Command index for stop. CMD12 by default

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表 14-1: SDMMC 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7]	rw	1'h0	read_long_rsp	Read response is 136-bit, long response
[6]	rw	1'h1	read_has_rsp	Read command have a response
[5:0]	rw	6'h12	read_index	Command index for cache read. CMD18 by default
0x64			**CACNT**	cache counter register
[31:16]	rw	16'hffff	cache_tor	timeout count register for ahb read
[15:8]	rw	8'h0	cache_ndc	data-cmd interval counter in hclk cycles
[7:0]	rw	8'h20	cache_ncc	cmd-cmd interval counter in hclk cycles
0x68			**CAOFF**	cache offset register
[31:0]	rw	32'h0	cache_offset	offset to map ahb address to sd address for ahb access
0x200			**FIFO**	FIFO entry
[31:0]	rw	32'h0	data	Entry to access internal FIFO. Access should be word-aligned, ranging from 0x200 to 0x3fc. Inside the range, write to any address will push the data into the FIFO, and read any address will pop a word from the FIFO.

14.2 MPI

芯片共有 3 个 MPI。MPI1 的输入输出连接至 IO(SA)，用于访问芯片内合封 (SiP) 的 8 线 pSRAM。MPI2 的输入输出连接至 IO(SB)，用于访问芯片内合封 (SiP) 的 8 线 pSRAM 或 NOR Flash。MPI3 的输入输出连接至 IO(PA)，用于访问芯片外接的 NOR/NAND Flash。

MPI (Memory Peripheral Interface) 控制器是一个专用的 memory 通信接口，支持多种片外存储颗粒，包括：

- SPI NOR Flash，支持 1 线/2 线/4 线，支持 DTR 模式
- SPI NAND Flash，支持 1 线/2 线/4 线
- pSRAM，支持 x8 和 x16 数据位宽，支持 Xccela 标准接口，兼容 Legacy 接口
- HyperRAM，支持 x8 和 x16 数据位宽，支持 HyperBus 标准接口

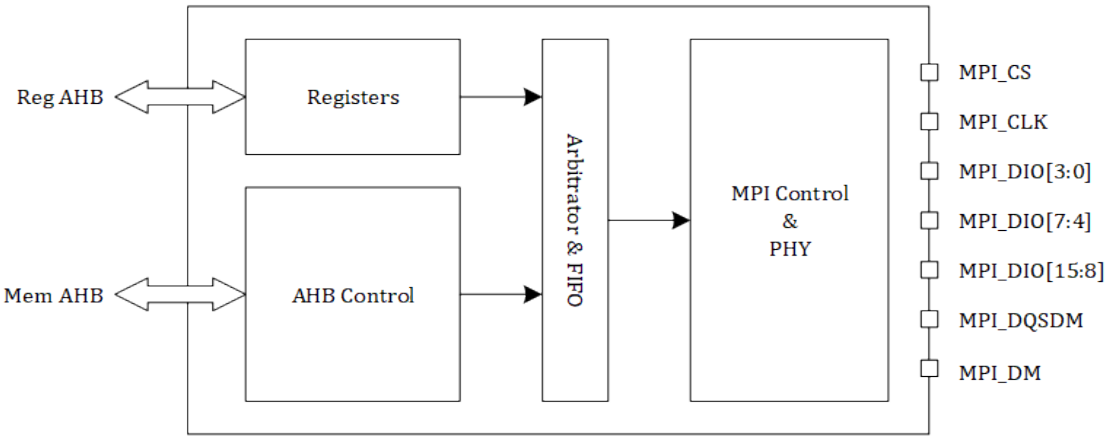


图 14-2: MPI 控制器框图

MPI 控制器支持两种操作模式：（1）寄存器模式和（2）地址映射模式。两种模式的切换由硬件自动完成，可动态穿插执行。且无论哪种模式，都支持高度可定制的接口时序，以兼容各种存储颗粒。

寄存器模式

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- 通过寄存器操作，发送一个命令时序。也可以将该命令设置为状态查询命令反复发送，直到读回的数据满足某个预设状态
- 支持发送包含两个命令时序的序列，其中第二个命令可设置为状态查询命令反复发送，直到读回的数据满足某个预设状态
- 支持 DMA 通道，通过寄存器 FIFO 接口完成数据搬运

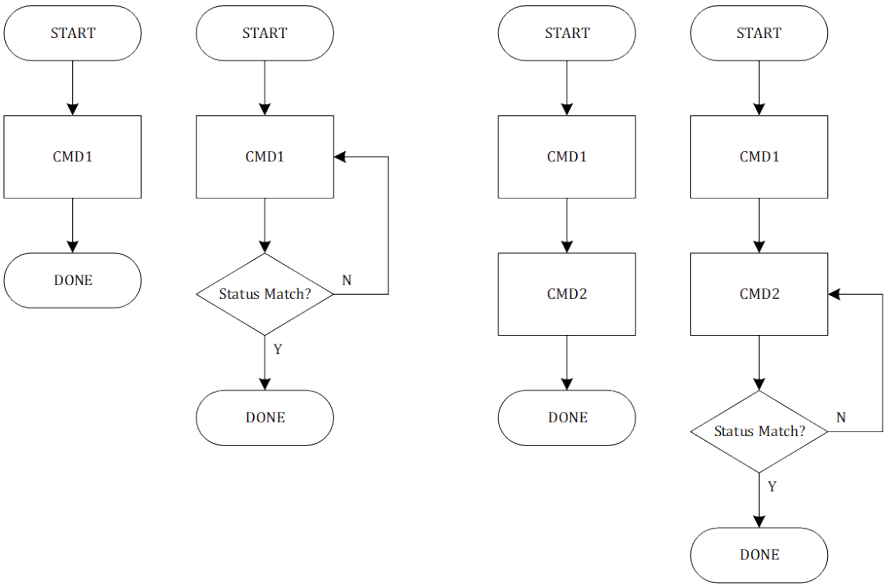


图 14-3: 寄存器模式单个和多个命令时序的序列

地址映射模式

- 外部 memory 映射为 AHB 地址空间，自动将 AHB 总线读写转换为预设的 Memory 接口时序，实现 XIP 功能
- 支持 Byte (8-bit)、Half-word (16-bit) 和 Word (32-bit) AHB 访问
- 高效转换 AHB Wrap 操作，不依赖于颗粒是否支持 Wrap
- 支持 XIP 实时（On-The-Fly）解密，模式为 AES128-CTR 或者 AES256-CTR
- 支持连续读写功能，如果当前一笔 AHB 的读写地址与前一笔连续，则直接开始数据传输，省略命令和地址部分。该功能可大幅提升大块数据搬运时的有效带宽
- 针对 pSRAM 和 HyperRAM 的内部动态刷新特性，自动处理颗粒最长 CS 拉低时间、最近 CS 访问间隔、最大 burst 数据长度等限制，无需软件处理

14.2.1 MPI 寄存器

MPI1 的基地址是 0x50041000。

MPI2 的基地址是 0x50042000。

MPI3 的基地址是 0x50042000

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表 14-2: MPI 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**CR**	Control Register
[31]	w1t	1'h0	ABORT	Write 1 to abort internal state machine. For debug purpose only
[30:26]			RSVD	
[25]	rw	1'h0	AHBDIS	Hold hreadyout low if AHB access
[24]	rw	1'h0	DFM	Dual Flash Mode Reserved-Do not modify
[23]	rw	1'b0	MX16	Mode X16 Reserved-Do not modify
[22]	rw	1'b0	PREFE	Prefetch enable. If enabled, MPI will prefetch at consequtive address following a read transaction. Recommend to use when reading large data in a burst manner. 0: prefetch disabled 1: prefetch enabled
[21]	rw	1'b0	OPIE	OPI interface enable 0: x8 mode disabled 1: x8 mode enabled
[20]	rw	1'b0	HWIFE	Hardware interface enable Reserved-Do not modify
[19]	rw	1'b0	SMM	Status match mode 0: AND mode 1: OR mode
[18]	rw	1'b0	SME2	Status match enable. If enabled, CMD2 will be issued repeatedly until the data match the value in SMR and SMKR 0: disabled 1: enabled
[17]	rw	1'b0	SME1	Status match enable. If enabled, CMD1 will be issued repeatedly until the data match the value in SMR and SMKR 0: disabled 1: enabled (either SME1 or SME2 can be enabled, and SME1 has high priority)
[16]	rw	1'b0	CMD2E	Enable CMD2 0: disabled 1: CMD2 is enabled and will be issued after CMD1 with an interval of TI2
[15:14]			RSVD	
[13]	rw	1'h0	RBXIE	Row boundary crossing interrupt enable
[12]	rw	1'h0	CSVIE	CS max violation interrupt enable
[11]	rw	1'h0	SMIE	Status match interrupt enable
[10]			RSVD	
[9]			RSVD	
[8]	rw	1'h0	TCIE	Transfer complete interrupt enable
[7]	rw	1'h0	CTRM	AES-CTR mode 0: AES-128 1: AES-256
[6]	rw	1'h0	CTRE	AES-CTR on-the-fly decryption enable 0: disabled 1: enabled, data read from memory will be decrypted on the fly by MPI controller
[5]	rw	1'h0	DMAE	DMA enable 0: disabled 1: enable DMA to read or write DR register
[4]	rw	1'h0	HOLD	The value of HOLD when HOLDE is set
[3]	rw	1'h0	HOLDE	Enable HOLD function on IO3. Use this only in SPI or Dual SPI mode
[2]	rw	1'h0	WP	The value of WP when WPE is set

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表 14-2: MPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[1]	rw	1'h0	WPE	Enable WP function on IO2. Use this only in SPI or Dual SPI mode
[0]	rw	1'h0	EN	Enable MPI
0x04			**DR**	Data Register
[31:0]	rw	32'h0	DATA	The entry of internal data FIFO
0x08			**DCR**	Device Control Register
[31]	rw	1'h0	FIXLAT	Indicate PSRAM is fixed latency or variable latency. It must be compatible to the configuration in PSRAM registers. Recommend always set to 1. 0: variable latency 1: fixed latency
[30:26]	rw	5'h0	TRCMIN	Write/Read cycle minimum time in internal MCLK cycles. Please see MCLK frequency in PSCLR description. For example, if PSRAM clock is 120MHz (i.e. internal MCLK is 240MHz) and TRCMIN = n, then tRC time = (n+1) * 1000/240 ns which must meet minimum tRC requirement for PSRAM
[25:22]	rw	4'h2	CSHMIN	Minimum CS high deselect time in MCLK cycles. For example, if PSRAM clock is 120MHz (i.e. internal MCLK is 240MHz) and CSHMIN = n, then CS High time = (n+1) * 1000/240 ns which must meet minimum tCPH requirement for PSRAM
[21:18]	rw	4'h0	CSLMIN	Minimum CS low active time in MCLK cycles. For example, if PSRAM clock is 120MHz (i.e. internal MCLK is 240MHz) and CSLMIN = n, then CS Low time = (n+1) * 1000/240 ns which must meet the minimum tCEM requirement for PSRAM
[17:6]	rw	12'h0	CSLMAX	Maximum CS low active time in MCLK cycles For example, if PSRAM clock is 120MHz (i.e. internal MCLK is 240MHz) and CSLMAX = n, then CS Low time = (n+1) * 1000/240 ns which must meet the maximum tCEM requirement for PSRAM
[5]	rw	1'h0	XLEGACY	Xccela legacy protocol. Set to 1 for AP 32Mb PSRAM only, othersize always set to 0.
[4]	rw	1'h0	HYPER	HyperBus protocol. Set to 1 for HyperRAM.
[3]	rw	1'h0	DQSE	DQS enable. Setting to 1 indicates device provides DQS signal for Rx data latching
[2:0]	rw	3'h0	RBSIZE	Row boundary size. 0: no row boundary 1: $2^{(1+3)}$ = 16 bytes 2: $2^{(2+3)}$ = 32 bytes ... n: $2^{(n+3)}$ bytes
0x0C			**PSCLR**	Prescaler Register
[31:8]			RSVD	

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表 14-2: MPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7:0]	rw	8'h4	DIV	Prescaler divider. 0: MCLK = FCLK/1 1: MCLK = FCLK/1 2: MCLK = FCLK/2 n: MCLK = FCLK/n Note: FLASH clock = MCLK. E.g. FCLK=192M and DIV=2, then FLASH clock = MCLK = 192/2 = 96MHz PSRAM clock = MCLK/2. E.g. FCLK=240M and DIV=1, then PSRAM clock = MCLK/2 = 240/2 = 120MHz
0x10			**SR**	Status Register
[31]	r	1'h0	BUSY	For debug purpose only
[30:6]			RSVD	
[5]	r	1'h0	RBXF	Row boundary crossing flag
[4]	r	1'h0	CSVF	CS max violation flag
[3]	r	1'h0	SMF	Status match flag in Polling Mode
[2]			RSVD	
[1]			RSVD	
[0]	r	1'h0	TCF	Transfer complete flag
0x14			**SCR**	Status Clear Register
[31:6]			RSVD	
[5]	w1c	1'h0	RBXFC	Write 1 to clear RBXF
[4]	w1c	1'h0	CSVFC	Write 1 to clear CSVF
[3]	w1c	1'h0	SMFC	Write 1 to clear SMF
[2]			RSVD	
[1]			RSVD	
[0]	w1c	1'h0	TCFC	Write 1 to clear TCF
0x18			**CMDR1**	Command Register
[31:8]			RSVD	
[7:0]	rw	8'h0	CMD	Command. Write to this register will trigger the sequence specified in CCR1
0x1C			**AR1**	Address Register
[31:0]	rw	32'h0	ADDR	Address
0x20			**ABR1**	Alternate Byte Register
[31:0]	rw	32'h0	ABYTE	Alternate byte
0x24			**DLR1**	Data Length Register
[31:20]			RSVD	
[19:0]	rw	20'h0	DLEN	Data length 0: one byte 1: two bytes ... n: (n+1) bytes
0x28			**CCR1**	Communication Configuration Register
[31:22]			RSVD	
[21]	rw	1'b0	FMODE	Function Mode 0: read mode 1: write mode

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表 14-2: MPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[20:18]	rw	3'h0	DMODE	Data Mode 0: no data phase 1: single line 2: dual lines 3: quad lines 4/5/6: reserved 7: quad lines DDR
[17:13]	rw	5'h0	DCYC	Number of dummy cycles 0: no dummy cycle 1: one dummy cycle 2: two dummy cycles
[12:11]	rw	2'h0	ABSIZE	Alternate byte size 0: one byte 1: two bytes 2: three bytes 3: four bytes
[10:8]	rw	3'h0	ABMODE	Alternate byte mode 0: no alternate byte 1: single line 2: dual lines 3: quad lines 4/5/6: reserved 7: quad lines DDR
[7:6]	rw	2'h0	ADSIZE	Address size 0: one byte 1: two bytes 2: three bytes 3: four bytes
[5:3]	rw	3'h0	ADMODE	Address mode 0: no address phase 1: single line 2: dual line 3: quad line 4/5/6: reserved 7: quad line DDR
[2:0]	rw	3'h0	IMODE	Instruction mode 0: no instruction phase 1: single line 2: dual lines 3: quad lines 4/5/6 - reserved 7 - quad lines DDR
0x2C			**CMDR2**	Command Register
[31:8]			RSVD	
[7:0]	rw	8'h0	CMD	Command 2. If CMD2E is enabled, the CMD2 sequence will be issued after CMD1 as specified in CCR2 Note: CMD2 sequence cannot be issue individually
0x30			**AR2**	Address Register
[31:0]	rw	32'h0	ADDR	Address byte in CMD2 sequence

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表 14-2: MPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x34			**ABR2**	Alternate Byte Register
[31:0]	rw	32'h0	ABYTE	Alternate byte in CMD2 sequence
0x38			**DLR2**	Data Length Register
[31:20]			RSVD	
[19:0]	rw	20'h0	DLEN	Data length in CMD2 sequence
0x3C			**CCR2**	Communication Configuration Register
[31:22]			RSVD	
[21]	rw	1'b0	FMODE	
[20:18]	rw	3'h0	DMODE	
[17:13]	rw	5'h0	DCYC	
[12:11]	rw	2'h0	ABSIZE	
[10:8]	rw	3'h0	ABMODE	
[7:6]	rw	2'h0	ADSIZE	
[5:3]	rw	3'h0	ADMODE	
[2:0]	rw	3'h0	IMODE	This register specifies the format of CMD2 sequence. Refer to CCR1 description
0x40			**HCMDR**	AHB Command Register
[31:16]			RSVD	
[15:8]	rw	8'h02	WCMD	AHB write command. During XIP, the AHB write transaction will be translated into this Write Command on memory interface
[7:0]	rw	8'h0b	RCMD	AHB read command. During XIP, the AHB read transaction will be translated into this Read Command on memory interface
0x44			**HRABR**	AHB Read Alternate Byte Register
[31:0]	rw	32'h0	ABYTE	
0x48			**HRCCR**	AHB Read Communication Configuration Register
[31:21]			RSVD	
[20:18]	rw	3'h0	DMODE	
[17:13]	rw	5'h0	DCYC	
[12:11]	rw	2'h0	ABSIZE	
[10:8]	rw	3'h0	ABMODE	
[7:6]	rw	2'h0	ADSIZE	
[5:3]	rw	3'h0	ADMODE	
[2:0]	rw	3'h0	IMODE	This register specifies the format of AHB read command sequence. Refer to CCR1 description
0x4C			**HWABR**	AHB Write Alternate Byte Register
[31:0]	rw	32'h0	ABYTE	
0x50			**HWCCR**	AHB Write Communication Configuration Register
[31:21]			RSVD	
[20:18]	rw	3'h0	DMODE	
[17:13]	rw	5'h0	DCYC	
[12:11]	rw	2'h0	ABSIZE	
[10:8]	rw	3'h0	ABMODE	
[7:6]	rw	2'h0	ADSIZE	
[5:3]	rw	3'h0	ADMODE	
[2:0]	rw	3'h0	IMODE	This register specifies the format of AHB write command sequence. Refer to CCR1 description
0x54			**FIFOCR**	FIFO Control Register
[31:15]			RSVD	

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表 14-2: MPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[14:10]	rw	5'h8	TXSLOTS	When DMA enabled, asserts DMA reqeust if TXFIFO vacant slots is greater than or equal to TXSLOTS. Note: this field should be set in accordance to the burst length in DMA. For example, if DMA employs BURST8 transction, then this filed is set to 8
[9]	r	1'h0	TXF	Tx FIFO full flag
[8]	w1c	1'h0	TXCLR	write 1 to clear Tx FIFO
[7:2]			RSVD	
[1]	r	1'h1	RXE	Rx FIFO empty
[0]	w1c	1'h0	RXCLR	write 1 to clear Rx FIFO
0x58			**MISCR**	Miscelaneous Register
[31:28]	rw	4'h0	DBGSEL	
[27]			RSVD	
[26]	rw	1'h0	DTRPRE	Enable pre-sampling for DTR Reserved-Do not modify
[25]	rw	1'h1	SCKINV	Invert output clock. This bit is used to align (coarse tune) the output clock to the center of output data.
[24]	rw	1'h0	RXCLKINV	Invert internal Rx clock to add half-cycle delay (coarse tune) when sampling data. It is usually used for FLASH device w/ higher frequency.
[23:16]	rw	8'h0	DQSDLY	Delay the input DQS signal to the appropriate sampling position. For device w/ DQS signal only. Note: effective 7-bit
[15:8]	rw	8'h0	SCKDLY	Add delay on output clock to fine tune the clock position. Note: effective 7-bit
[7:0]	rw	8'h0	RXCLKDLY	Add delay on internal Rx clock to fine tune the sampling position. Note: effective 5-bit
0x5C			**CTRSAR**	CTR Starting Address Register
[31:10]	rw	22'h0	SA	Starting address of the AES decryption area. Since the lowest 10 bits are zero, the address is always 1KB aligned. Together with CTREAR, the total area is [CTRSAR, CTREAR) For example, CTRSAR = 32'h0, CTREAR = 32'h200000, then the on-the-fly decryption area is 0x0 - 0x1FFFFF
[9:0]			RSVD	
0x60			**CTREAR**	CTR Ending Address Register
[31:10]	rw	22'h0	EA	Ending address of the AES decryption area
[9:0]			RSVD	
0x64			**NONCEA**	Nonce A Register
[31:0]	rw	32'h0	NONCEA	Used for on-the-fly decryption
0x68			**NONCEB**	Nonce B Register
[31:0]	rw	32'h0	NONCEB	Used for on-the-fly decryption
0x6C			**AASAR**	Address Aliasing Start Address Register
[31:10]	rw	22'h0	SA	Starting address of the address aliasing area. Always 1KB aligned.Together with AAEAR, the aliasing area is [AASAR, AAEAR). If the address falls into this area, an offset AAOAR is added and the aliased address will be used to access external memory
[9:0]			RSVD	
0x70			**AAEAR**	Address Aliasing Ending Address Register
[31:10]	rw	22'h0	EA	Ending address of the address aliasing area
[9:0]			RSVD	
0x74			**AAOAR**	Address Aliasing Offset Address Register
[31:10]	rw	22'h0	OA	The offset to be added to the original address
[9:0]			RSVD	

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表 14-2: MPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
0x78			**CIR**	Command Interval Register
[31:16]	rw	16'h0	INTERVAL2	The interval between CMD1 and CMD2 (or between CMD2 itself) if CMD2E is enabled. The unit is in MCLK cycles
[15:0]	rw	16'h0	INTERVAL1	The interval between CMD1 itself. The unit is in MCLK cycles
0x7C			**SMR**	Status Match Register
[31:0]	rw	32'h0	STATUS	If status match is enabled, this register is compared with the data read from external memory. Together with SMKR, only the bits with mask=1 will be considered to compare in AND or OR mode as configured in SMM field.
0x80			**SMKR**	Status Mask Register
[31:0]	rw	32'h0	MASK	Status mask 0: the corresponding bit is not considered to compare 1: the corresponding bit is considered to compare
0x84			**TIMR**	Timer Register
[31:16]			RSVD	
[15:0]	rw	16'h0	TIMEOUT	After the transaction is complete, CS remains low for multiple cycles of MCLK as specified by this register. For example if TIMEOUT=n, CS remains active for n cycles, during which if a new transaction occurs and the address is consecutive, the memory access can be resumed w/o sending the command and address again.
0x88			**WDTR**	WDT Register
[31]	r	1'h0	TOF	Timeout flag. Self cleared when HREADYOUT becomes ready
[30:17]			RSVD	
[16]	rw	1'b0	EN	WDT enable. This watchdog is on AHB side such that bus access will not hang in exceptional cases
[15:0]	rw	16'hffff	TIMEOUT	Set timeout value in number of clk_wdt cycles
0x8C			**PRSAR**	Prefetch Starting Address Register
[31:10]	rw	22'h0	SA	Starting address of the prefetch area If prefetch is enabled and the read address falls into [PRSAR, PREAR), controller will prefetch the following data
[9:0]			RSVD	
0x90			**PREAR**	Prefetch Ending Address Register
[31:10]	rw	22'h0	EA	Ending address of the prefetch area
[9:0]			RSVD	
0x94			**CALCR**	Calibration Clock Register
[31]	rw	1'h0	EN	calibration enable
[30:9]			RSVD	
[8]	r	1'h0	DONE	calibration done flag
[7:0]	r	8'h0	DELAY	calibration delay result
0x9C			**APM32CR**	APM32 Control Register
[31:8]			RSVD	
[7:4]	rw	4'h4	TCPHW	For special use by AP 32Mb PSRAM. Reserved-Do not modify
[3:0]	rw	4'h2	TCPHR	For special use by AP 32Mb PSRAM. Reserved-Do not modify
0xA0			**CR2**	Control Register 2
[31:8]			RSVD	

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表 14-2: MPI 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[7:0]	rw	8'h0	LOOP	Repeat CMD1->CMD2 sequence for n times. This filed is only valid when CMD2E=1 and SME2=0. For example if LOOP=0, then the sequence is CMD1 -> CMD2. If LOOP=2, then the sequence is (CMD1->CMD2) -> (CMD1->CMD2) -> (CMD1->CMD2)

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15 调试接口

15.1 简介

芯片支持 SWD 与 UART 两种调试接口。这两种调试接口都可以对芯片内所有 CPU 进行调试，完成暂停，获取状态，单步等操作，也可以访问总线地址，完成存储器和寄存器的读写操作。UART 在进行调试的同时还能够输出日志信息。调试接口可以通过烧录 EFUSE 禁用，禁用级别可配置为通过密钥临时开启，或永久封禁。

15.2 调试结构图

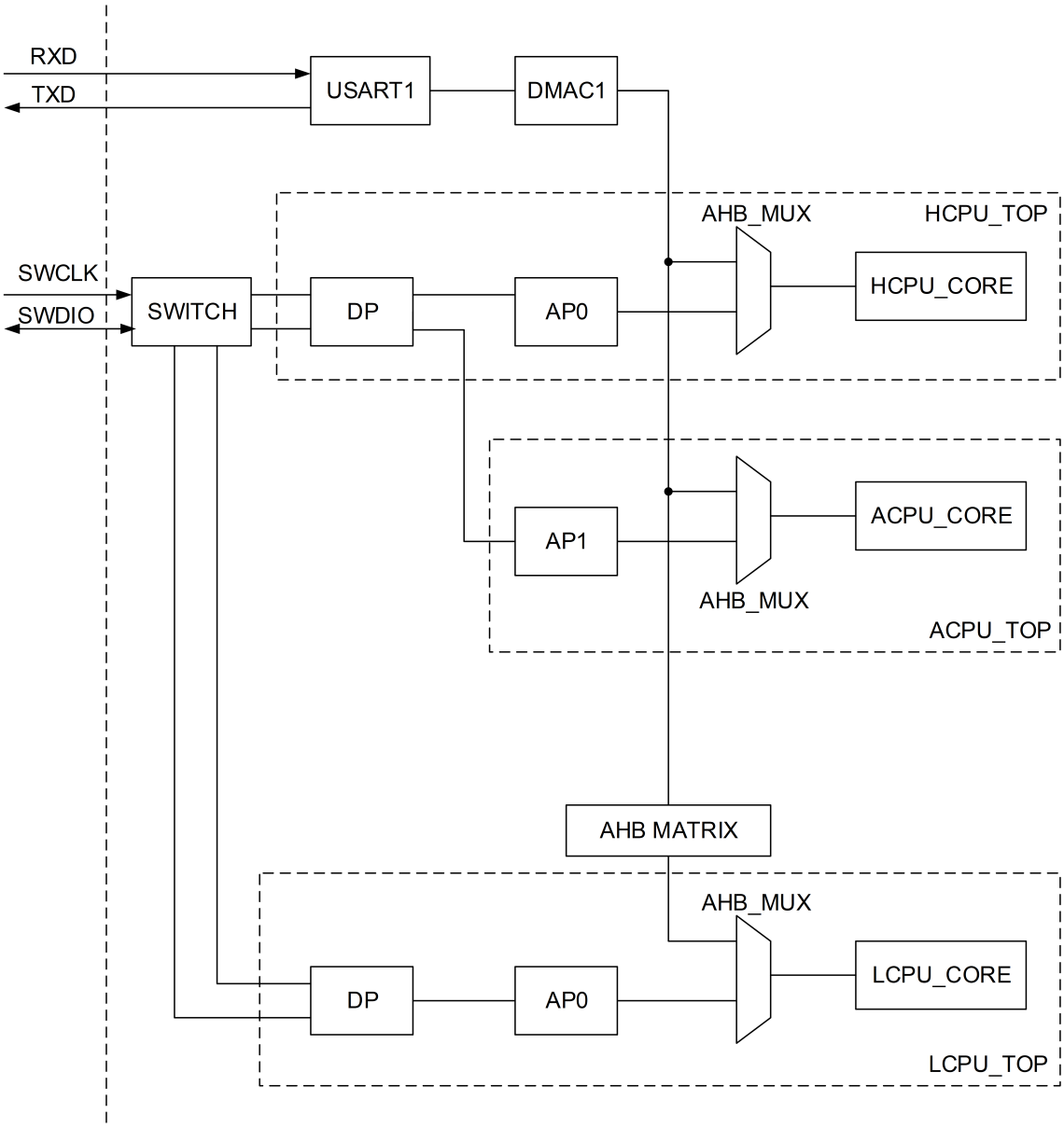


图 15-1: 调试结构图

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15.3 SWD 调试

15.3.1 主要特性

- SWD 可同时调试 HCPU 与 ACPU，通过 AP 切换
- 支持 HCPU SWO 输出
- 支持通过总线地址访问各存储器及寄存器
- 可永久禁用，或通过密钥临时开启

15.3.2 调试 HCPU

PA44 和 PA43 默认是 SWD 的 SWCLK 和 SWDIO(需启动时 PA01 为低电平)。HPSYS 没有进入 deepsleep/standby/hibernate 模式时，PC 通过调试器连接到芯片的 SWD 端口，可以搜索到 HCPU 并连接。

PC 通过 SWD 调试器可以控制 HCPU 的运行，读写 HCPU 以及各模块的寄存器，读写存储器内容。

HCPU 支持 ITM，用于软件日志打印，系统事件记录，时间戳记录等，如需使用应将 IO(PA20) 切换为 SWO 功能。

如果芯片启用了安全方案，SWD 可能默认无法连通，需首先通过密钥激活 SWD 功能，再进行连接。

15.3.3 调试 ACPU

ACPU 时钟使能，并且 reset 释放后，PC 通过 SWD 调试器可以检测到 ACPU 并连接。

HCPU 与 ACPU 通过 SWD 的不同 AP 区分，因此同一个调试器通过切换 AP 可以同时调试 HCPU 与 ACPU。

PC 通过 SWD 调试器可以控制 ACPU 的运行，读写 ACPU 以及各模块的寄存器，读写存储器内容。

ACPU 不支持 ITM 与 MTB。

HPSYS 处于 deepsleep/standby/hibernate 时，无法调试 ACPU。

15.3.4 调试 LCPU

SWD 默认连接到 HCPU 上。如果需要通过 SWD 调试 LCPU，应配置 HPSYS_CFG → SWCR 为 1，将 SWD 通路切换至 LCPU。

SWD 通路切换至 LCPU 后，如果 LCPU 时钟使能，并且 reset 释放，PC 即可通过 SWD 调试器检测到 LCPU 并连接。

PC 通过 SWD 调试器可以控制 LCPU 的运行，读写 LCPU 以及各模块的寄存器，读写存储器内容。

LCPU 不支持 ITM 与 MTB。

LPSYS 处于 deepsleep/standby/hibernate 模式时，无法调试 LCPU。

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15.4 UART 调试

芯片在 USART1 模块中集成了 UART 调试接口，为用户提供便捷高效的调试手段。用户仅需使用 UART 通信，即可进行 CPU 调试，完成暂停，获取状态，单步等操作；也可访问总线地址，完成存储器和寄存器的读写操作。USART1 在支持 UART 调试功能的同时，仍可进行通常的 UART 收发 (需上位机及驱动支持)。用户可通过烧写 EFUSE 永久禁用 UART 调试接口，而不影响 USART1 的正常功能。

15.4.1 主要特性

- 采用标准 UART 接口，仅需连接 TX, RX 和 GND
- 自定义调试帧
- 连接后波特率可配 (默认波特率 1M)
- 兼容 CPU 的各项调试功能
- 支持通过总线地址访问各存储器及寄存器
- 支持块数据传输，提高访问效率
- CPU 异常时不影响总线地址访问
- 可与普通 UART 功能共存
- 可永久禁用，或通过密钥临时开启

15.4.2 调试方法

上位机向 USART1 的接收端口 (PA18) 发送请求帧，并从 USART1 的发送端口 (PA19) 接收应答帧。请求帧与应答帧均依照 UART 协议传输，并且符合自定义调试帧格式。

请求帧共有 4 种格式，分别代表进入调试模式，退出调试模式，读数据，写数据。

每一种请求帧均有一种应答帧相对应，分别为已进入调试模式，已退出调试模式，读数据完成，写数据完成。

上位机发送完请求帧后，应等待应答帧返回，再发送下一个请求帧。如果在一定时间内 (如 100ms) 仍未收到应答帧返回，可认为请求超时，并可尝试重新发送请求帧。

上位机需首先下发进入调试模式的请求帧，并收到已进入调试模式的应答帧后，才能开始进行数据读写。

读数据时，需下发包含数据起始地址与数据长度的读数据请求帧，等待芯片返回读数据完成应答帧。数据内容包含在读数据完成应答帧内。

写数据时，需下发包含数据起始地址，数据长度与数据内容的写数据请求帧，等待芯片返回写数据完成应答帧。

调试完成后，可下发退出调试模式的请求帧，并等待已退出调试模式的应答帧。

15.4.3 自定义调试帧

自定义调试帧用于区分调试数据与正常传输的数据。

自定义调试帧格式如下，主要包括帧头 Header 和帧数据 Payload 两部分，依照从左到右，从低字节到高字节的顺序传输。长度 Length 共 2 字节，指示帧数据 Payload 的字节数。帧数据 Payload 的长度可变，传输顺序从最低字节开始。

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表 15-1: 自定义调试帧格式

Header (6 bytes)						Payload (Length bytes)			
0x7E	0x79	Length (Lower byte)	Length (higher byte)	0x10	0x00	Byte0	Byte1	···	Byte Length-1

帧数据 Payload 可进一步区分不同类型的帧。传输时依照从左到右，从低字节到高字节的顺序。

表 15-2: 进入调试模式 (请求帧)

Payload (8 bytes)							
0x41	0x54	0x53	0x46	0x33	0x32	0x05	0x21

表 15-3: 已进入调试模式 (应答帧)

Payload (2 bytes)	
0xD1	0x06

表 15-4: 退出调试模式 (请求帧)

Payload (8 bytes)							
0x41	0x54	0x53	0x46	0x33	0x32	0x18	0x21

表 15-5: 已退出调试模式 (应答帧)

Payload (2 bytes)	
0xD0	0x06

读数据 (请求帧)

Addr 表示读数据的起始地址，需 4 字节对齐。WordCnt 表示读数据的 word 数量。读取的字节数为 4 × WordCnt。

表 15-6: 读数据 (请求帧)

Payload (8 bytes)			
0x40	0x72	Addr (4 bytes)	WordCnt (2 bytes)

读数据完成 (应答帧)

表 15-7: 读数据完成 (应答帧)

Payload (2+4×WordCnt bytes)		
0xD2	Data (4×WordCnt bytes)	0x06

写数据 (请求帧)

Addr 表示写数据的起始地址，需 4 字节对齐。WordCnt 表示写数据的 word 数量。写入的字节数为 4 × WordCnt。

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表 15-8: 写数据 (请求帧)

Payload (8+4×WordCnt bytes)				
0x40	0x77	Addr (4 bytes)	WordCnt (2 bytes)	Data (4×WordCnt bytes)

写数据完成 (应答帧)

表 15-9: 写数据完成 (应答帧)

Payload (2 bytes)	
0xD3	0x06

15.4.4 调试示例

下面以一次完整的数据读写调试为例，列举调试过程中通过 UART 顺序传输的具体数据。下行代表上位机发送给芯片的请求帧。上行代表芯片返回给上位机的应答帧。假设地址 0x20000000 处已有数据 0x12345678。

表 15-10: UART 调试示例

方向	数据
下行	7E 79 08 00 10 00 41 54 53 46 33 32 05 21 (进入调试模式)
上行	7E 79 02 00 10 00 D1 06 (已进入调试模式)
下行	7E 79 0C 00 10 00 40 77 04 00 00 20 01 00 DD CC BB AA (写数据, 0xAABBCCDD 写入 0x20000004)
上行	7E 79 02 00 10 00 D3 06 (写数据完成)
下行	7E 79 08 00 10 00 40 72 00 00 00 20 02 00 (读数据, 从 0x20000000 开始 2 个 word)
上行	7E 79 0A 00 10 00 D2 78 56 34 12 DD CC BB AA 06 (读数据完成)
下行	7E 79 08 00 10 00 41 54 53 46 33 32 18 21 (退出调试模式)
上行	7E 79 02 00 10 00 D0 06 (已退出调试模式)

15.4.5 地址映射

UART 调试接口基于总线地址读写数据，但地址映射与 HCPU 略有差异。UART 调试接口另包含若干专用寄存器。具体见下表。

表 15-11: UART 调试接口地址映射

调试接口地址空间	HCPU 地址空间	ACPU 地址空间	ACPU 地址空间
HPSYS_ROM	0xA0000000 起	0x0 起	/
HCPU 系统寄存器	0xF0000000 起	0xE0000000 起	/
ACPU 系统寄存器	0xF8000000 起	/	0xE0000000 起
MPI	0x60000000 起	0x10000000 或 0x60000000 起	0x60000000 起
其它存储器	相同		
其它模块寄存器	相同		
(专用)boot mode	0xFFA57200	/	/
(专用)HCPU 系统复位	0xFFA57201	/	/
(专用) 芯片复位	0xFFA57203	/	/

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15.4.6 调试 HCPU

可通过对 HCPU 系统寄存器的读写访问实现调试 HCPU。具体寄存器的操作方法请参考 ARM 公司相关文档。

UART 调试接口可通过地址空间 0xF0000000~0xF00FFFFF 访问 HCPU 系统寄存器，实现对 HCPU 的调试功能，包括但不限于暂停，获取状态，单步，系统复位等操作。

15.4.7 调试 ACPU

UART 调试接口可通过地址空间 0xF8000000~0xF80FFFFF 访问 ACPU 系统寄存器，实现对 ACPU 的调试功能，包括但不限于暂停，获取状态，单步，系统复位等操作。

15.4.8 调试 LCPU

UART 调试接口可通过地址空间 0x30000000~0x300FFFFF 访问 LCPU 系统寄存器，实现对 LCPU 的调试功能，包括但不限于暂停，获取状态，单步，系统复位等操作。

15.4.9 USART1 行为

USART1 模块在芯片启动后默认开启，并在接收端 (PA18) 持续监测自定义调试帧序列，当发现合法的自定义调试帧时，自动执行相应操作，并通过发射端 (PA19) 返回响应。USART1 模块默认为 1M 波特率，8 位数据，1 位停止位，无校验。

USART1 在进行调试数据读写时，会自动调用 DMAC1 的专用通道进行总线数据读写，不影响 DMAC1 其它通道的功能，但会占用一定的总线带宽。

15.4.10 调试接口失效

出现如下情况时，调试接口可能无法连接或读写失败：

- 波特率错误。芯片上电后默认波特率是 1M，但如果固件修改了 USART1 的波特率，就需要按照修改后的波特率连接调试接口。
- USART1 的端口映射到了其它 IO。
- DMAC1 时钟被关闭，或被复位。
- DMAC1 总线卡死。MPI 未初始化时，DMAC1 或 UART 调试接口访问了该 MPI 的存储器空间 (如 Nor Flash 或 PSRAM)，有可能造成总线卡死。
- HPSYS 进入低功耗模式。HPSYS 处于 deepsleep 或 standby 模式，或芯片处于 hibernate 模式时，UART 调试接口无法工作。
- 调试接口通过 EFUSE 控制位被禁用。

15.4.11 调试数据与普通数据共存

使用调试接口的同时，USART1 仍能进行通用 UART 数据的收发，但需遵守如下规则避免冲突。

CPU 使用 USART1 发送数据前必须读取 USART1 的数据锁寄存器 EXR_BUSY。如果读出为 1，说明已上锁 (调试接口正在工作)，需等待一段时间后重新尝试。如果读出为 0，数据锁会自动置 1，此时可以开始正常发送数据，数据发送结束后需向 EXR_BUSY 写 1 进行解锁。

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UART 调试接口发送调试数据前也会自动判断 EXR_BUSY，如果 EXR_BUSY 为 1 则会等到 CPU 解锁后再启动发送，否则直接发送数据并自动上锁，直到发送完成后自动解锁。

USART1 接收到的所有数据都可被 CPU 读取，包括请求帧与通用数据。固件需通过自定义调试帧的格式区分不同的数据。

15.5 调试 IO

SWD 调试默认占用 PA43 和 PA44，硬件默认映射为 SWCLK(FSEL=1) 和 SWDIO(FSEL=1)。如果需要使用 SWO 功能，还需额外将 PA20 切换为 SWO(FSEL=1)，否则 PA20 可以作为通用 IO 使用。如果不使用 SWD 调试功能，PA43 和 PA44 也可以作为通用 IO 使用。

DBGUART 调试默认占用 PA18 和 PA19。如果不使用 DBGUART 下载或调试，PA18 和 PA19 也可以作为通用 IO 使用，但需注意如果启动时 PA01 为低电平，PA19 会输出启动信息。

芯片启动时如果 PA01 上拉至高电平，PA18 和 PA19 会由硬件自动切换至 SWD 功能，分别为 SWCLK(FSEL=2) 和 SWDIO(FSEL=2)，而 PA43 和 PA44 的 SWD 功能自动失效，但功能选择仍在 SWD 上 (FSEL=1)，可由软件切换至其它功能使用。此时 PA19 不会输出启动信息。

表 15-12: 调试 IO 列表

	默认上下拉	启动时 PA01 为低电平		启动时 PA01 为高电平		备注
		默认功能	默认 FSEL	默认功能	默认 FSEL	
PA18	上拉	USART1_RXD	1	SWD_CLK	2	
PA19	上拉	USART1_TXD	1	SWD_SDIO	2	USART1_TXD 会输出启动信息
PA43	下拉	SWD_CLK	1	无	1	
PA44	下拉	SWD_SDIO	1	无	1	
PA20	下拉	GPIO	0	GPIO	0	可切换至 SWO(FSEL=1)

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16 烧录与启动

16.1 烧录

16.1.1 BOOT MODE

BOOT MODE 是芯片启动以后等待程序烧录的模式。进入 BOOT MODE 以后，芯片会停留在等待烧录的状态，不会加载用户的程序代码，因此在 BOOT MODE 进行程序烧录可以避免用户程序的影响。

满足以下任一条件，芯片会进入 BOOT MODE：

1. 启动时 PA00 为高电平。PA00 默认在芯片内存在下拉电阻。当需要进入 BOOT MODE 时，可对 PA00 施加强上拉 (上拉电阻 7.5k 欧姆或更低)，使得 PA00 的电平变高，随后使芯片上电或重启。BOOTROM 运行时读取 PA00 的电平，如果为高就会进入 BOOT MODE。程序烧录完成后，如果要进入常规启动流程，应先去除 PA00 的上拉再重启。程序从 BOOTROM 跳出后 PA00 即可作为普通 IO 使用。
2. 启动时 BOOT 寄存器为 1。BOOT 寄存器是 HPSYS_CFG 的 BMR.BOOT_MODE，可由软件写入，也可通过 DBGUART 写入。当需要进入 BOOT MODE 时，可先将该寄存器置 1 再重启芯片。重启后该寄存器值不会改变，BOOTROM 运行时读取 BOOT 寄存器的值，如果为 1 就会进入 BOOT MODE。程序烧录完成后，如果要进入常规启动流程，应先将 BOOT 寄存器置 0 再重启。
3. 启动时 PA01 为低电平，芯片通过 DBGUART 连接到上位机烧录工具，并且工具开启 BOOT 开关。PA01 默认在芯片内存在下拉电阻。启动时 PA01 的电平用于切换 PA18 与 PA19 的功能。如果启动时 PA01 为低电平，PA18 与 PA19 默认就是 DBGUART 的 RXD 与 TXD 信号。BOOTROM 会通过 PA19 输出启动信息并等待 100ms。在这段时间内上位机烧录工具接收到启动信息后会通过 PA18 发送 DBGUART 调试指令，将 BOOT 寄存器置为 1。等待时间结束后 BOOTROM 程序读取 BOOT 寄存器，为 1 则进入 BOOT MODE。如果启动时 PA01 为高电平，PA18 与 PA19 切换为 SWD 功能，PA19 不会输出启动信息，也无法通过 DBGUART 连接到上位机烧录工具。程序烧录完成后，如果要进入常规启动流程，应先将 BOOT 寄存器置 0，再禁用上位机烧录功能，随后重启芯片 (这几步均可由上位机自动完成)。

上述条件 3 与条件 2 都是通过将 BOOT 寄存器置 1 使 BOOTROM 进入 BOOT MODE，区别在于条件 2 是先将 BOOT 寄存器置位再重启进入 BOOT MODE，而条件 3 是直接重启，随后由上位机通过 DBGUART 将 BOOT 寄存器置位，进入 BOOT MODE。

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表 16-1: BOOT MODE 进入条件

PA00	BOOT 寄存器	PA01	上位机 BOOT 开关	启动分支
0	0	1	任意	常规启动，PA19 不输出启动信息
		0	关闭	常规启动，PA19 输出启动信息
		0	开启	BOOT MODE，PA19 输出启动信息，支持 DBGUART/SWD/UART/USB 烧录
任何一项为 1		0	任意	
		1	任意	BOOT MODE，PA19 不输出启动信息，支持 SWD/USB 烧录

进入 BOOT MODE 以后，芯片支持通过 SWD 或 DBGUART 调试接口直接烧录，也支持通过 UART 或 USB 进行烧录。为支持 USB 烧录，BOOTROM 会将 PA35(USB_DP) 的默认下拉电阻切换为上拉电阻，但不会产生输出。如果用户将 PA35 作为普通 IO 使用，应注意该 IO 电平可能发生改变。

如果芯片启动后未满足条件进入 BOOT MODE，则会进入常规启动分支。常规启动时，如果 BOOTROM 未能在启动存储器中检测到有效的程序镜像，仍会跳转至 BOOT MODE 等待烧录。因此出厂后未烧录过的空芯片也会自动进入 BOOT MODE。

16.1.2 BOOT 启动信息

芯片启动过程中，BOOTROM 会通过 DBGUART 输出启动信息"SFBL" 以及芯片 UID，输出 IO 为 PA19，波特率为 1M。随后 BOOTROM 会等待 100ms，等待时间结束后读取 BOOT 寄存器，判断是否进入 BOOT MODE。这 100ms 是预留给上位机烧录工具的反馈时间，上位机烧录工具应当在这 100ms 以内完成对 BOOT 寄存器的置位。如果启用了安全调试，上位机在置位 BOOT 寄存器之前还应先完成密钥解锁。

如果启动时 PA01 为高电平，PA18 与 PA19 自动切换为 SWD 功能，这种配置下 PA19 不会在启动时产生" 脏数据"，因此也可以作为普通 IO 使用。此时 PA18 和 PA19 由硬件自动切换为 SWCLK(FSEL=2) 和 SWDIO(FSEL=2)，而 PA43 和 PA44 的 SWD 功能自动失效，但功能选择仍在 SWD 上 (FSEL=1)，可由软件切换至其它功能使用。具体实现时，可以在芯片外部对 PA01 施加强上拉 (上拉电阻 7.5k 欧姆或更低) 使 PA01 变为高电平。

16.1.3 DBGUART 烧录

DBGUART 是 USART1 的专属调试功能。芯片上电后 USART1 默认使能，波特率为 1M，RXD 和 TXD 分别映射到 IO PA18 和 PA19(需启动时 PA01 为低电平)。BOOTROM 启动时会通过 USART1 输出启动信息。上位机接收到启动信息后，可通过 USART1 向芯片传输特定指令序列，使能 DBGUART 调试功能。DBGUART 调试功能使能后，上位机可通过 USART1 向芯片传输特定指令序列，实现读写寄存器和存储器，调试 CPU 等行为。DBGUART 烧录过程不依赖 BOOTROM 软件。

DBGUART 烧录由上位机控制，主要流程包括：

1. 使能 DBGUART 调试；
2. 暂停 HCPU 运行；

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3. 将烧录引导程序写入 SRAM；
4. 控制 HCPU 跳转到烧录引导程序中运行；
5. 将待烧录的镜像文件传输至芯片，通过烧录引导程序烧写到指定的存储器中；
6. 烧录结束后，将 BOOT 寄存器清 0，并重启。

如果启用了安全调试，DBGUART 调试功能需通过密钥激活后才能使用。激活方法是上位机向 USART1 发送一串密钥序列。

如果不需要使用 DBGUART 调试功能，PA18 和 PA19 可以作为普通 IO 使用。其中 PA19 默认会输出启动信息，可将 PA01 上拉避免产生输出。

16.1.4 SWD 烧录

芯片上电后，PA43 和 PA44 默认映射为 SWD 的 SWCLK 和 SWDIO(需启动时 PA01 为低电平)。上位机可通过 SWD 连接到芯片，实现读写寄存器和存储器，调试 CPU 等行为。SWD 烧录过程不依赖 BOOTROM 软件。

SWD 烧录由上位机控制，主要流程包括：

1. 建立 SWD 连接；
2. 暂停 HCPU 运行；
3. 将烧录引导程序写入 SRAM；
4. 控制 HCPU 跳转到烧录引导程序中运行；
5. 将待烧录的镜像文件传输至芯片，通过烧录引导程序烧写到指定的存储器中；
6. 烧录结束后，将 BOOT 寄存器清 0，并重启。

如果启用了安全调试，SWD 默认将无法调试，需首先通过密钥激活 SWD 功能，再进行连接。激活方法是上位机通过 SWD 向特定地址写入一串密钥序列。

16.1.5 UART 烧录

UART 烧录是由 BOOTROM 程序通过 USART1 接收数据并进行下载烧录的过程。

芯片上电后，USART1 默认使能，波特率为 1M，RXD 和 TXD 分别映射到 IO PA18 和 PA19(需启动时 PA01 为低电平)。进入 BOOT MODE 以后，BOOTROM 程序开始监测 USART1 接收到的数据，如果符合特定指令序列则进入 UART 烧录流程。

UART 烧录由上位机和 BOOTROM 共同完成，主要流程包括：

1. 上位机向 BOOTROM 发送特定指令序列，启动 UART 烧录；
2. 上位机向 BOOTROM 传输烧录引导程序，由 BOOTROM 写入 SRAM；
3. BOOTROM 控制 HCPU 跳转到烧录引导程序中运行；
4. 上位机向 BOOTROM 传输待烧录的镜像文件，通过烧录引导程序烧写到指定的存储器中；
5. 烧录结束后，BOOTROM 将 BOOT 寄存器清 0，并重启。

UART 烧录与 DBGUART 烧录的区别是，UART 烧录依赖 BOOTROM 中的软件处理 UART 接收到的指令与数据，调试器被禁用后仍可进行 UART 烧录，而 DBGUART 烧录是通过调试器接口直接传输程序并控制 CPU 跳转到 SRAM 中运行，不需要 BOOTROM 软件参与。

如果启用了安全启动流程，BOOTROM 会对烧录引导程序进行安全校验，只有校验通过才跳转运行。

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16.1.6 USB 烧录

USB 烧录是由 BOOTROM 程序通过 USBC1 接收数据并进行下载烧录的过程。

芯片进入 BOOT MODE 以后，BOOTROM 程序将 PA35 和 PA36 映射为 USBC1 的 DP 和 DM，初始化 USBC1 并开启 USB-CDC。上位机连接到芯片的 USB 后，识别出 UART 串口，即可进入 USB 烧录流程。USB 烧录流程与 UART 烧录流程类似，区别仅在于通信是通过 USBC1 映射出的串口，而不是 USART1。

如果启用了安全启动流程，BOOTROM 会对烧录引导程序进行安全校验，只有校验通过才跳转运行。

16.1.7 运行中重烧录

芯片正在运行用户程序时也支持重新烧录，而不需要将 BOOT PIN 拉高并重启。运行中烧录的前提条件是：

- 芯片未处于 hibernate 模式，且 HPSYS 未处于 deepsleep/standby 模式；
- 上位机通过 DBGUART/SWD 连接到芯片。

运行中烧录的流程是：

1. 上位机通过调试器触发 HCPU 复位并 halt；
2. HCPU 复位后自动 halt，上位机开始烧录程序；
3. 烧录完成后，上位机通过调试器触发芯片重启。

16.1.8 烧录的存储器选择

用户烧录芯片时已知芯片型号，存储器配置也为已知信息，因此不论使用哪种烧录方式，仅需在烧录时选择正确的配置脚本即可将程序烧写进相应的存储器。该环节主要的注意点就是烧录配置的选择，如果选择错误则会烧录失败。

16.2 常规启动

16.2.1 启动介质

芯片启动后如果不满足进入 BOOT MODE 的条件，会进入常规启动分支。

芯片支持多种启动介质，包括：

- 通过 MPI1/2 访问的合封 NOR Flash，连接至 IO(SA)；
- 通过 MPI3 访问的外部 NOR Flash；
- 通过 MPI3 访问的外部 NAND Flash；
- 通过 SDMMC1 访问的外部 SD-NAND/SD 卡；
- 通过 SDMMC1 访问的外部 eMMC。

进入常规启动分支后，BOOTROM 程序首先读取 EFUSE 中的 2-bit PKGID 判断启动介质。PKGID 与芯片型号有关，芯片出厂时已烧录完毕。

如果 PKGID 为 00, 01 或 10，BOOTROM 判断为合封启动介质。BOOTROM 自动从合封存储器启动。

如果 PKGID 为 11，BOOTROM 读取 Bootstrap PIN 的电平，判断外置启动介质。Bootstrap PIN 复用了芯片的两

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个通用 IO，其中 PA13 功能是 MPI3 的 D1 或 SDMMC1 的 D3，PA17 功能是 MPI3 的 D3 或 SDMMC1 的 D1。这两个 IO 在芯片内部默认下拉。如果需从外部 NOR FLASH 启动，PA13 与 PA17 外部不上拉。如果需从外部 NAND FLASH 启动，PA17 外部需增加 7.5k 欧姆的上拉电阻。如果需从外部 SD-NAND 启动，PA13 外部需增加 7.5k 欧姆的上拉电阻。如果需从外部 eMMC 启动，PA13 与 PA17 外部都需增加 7.5k 欧姆的上拉电阻。

表 16-2: 通过 Bootstrap PIN 区分外置启动介质

PA13	PA17	启动存储器	接口模块
0	0	外置 NOR	MPI3
0	1	外置 NAND	MPI3
1	0	外置 SD-NAND/SD 卡	SDMMC1
1	1	外置 eMMC	SDMMC1

BOOTROM 根据不同的外置启动介质，配置相应 PINMUX 并初始化 MPI3 或 SDMMC1 模块。

如果启动存储器是外置 NOR，BOOTROM 以 24M 单线模式尝试读取 NOR FLASH 中的 FTAB，并进行后续操作。

如果启动存储器是外置 NAND，BOOTROM 通过 MPI3 以 24M 单线模式将 NAND 上的二级 bootloader 搬运到 SRAM 执行。

如果启动存储器是外置 SD-NAND 或 eMMC，BOOTROM 通过 SDMMC1 以 24M 单线模式将 SD-NAND 或 eMMC 上的二级 bootloader 搬运到 SRAM 执行。

在二级 bootloader 中，PSRAM 被初始化，并加载应用程序。应用程序可直接在 NOR Flash 上运行，也可被搬运到 SRAM 或 PSRAM 上运行。

如果启动过程中初始化或搬运程序失败，BOOTROM 进入 BOOT MODE 运行。

如果启用了安全启动流程，BOOTROM 在搬运二级 bootloader 之后会进行安全校验，只有校验通过才跳转执行。

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17 蓝牙

17.1 蓝牙简介

支持蓝牙协议 v6.3 并向下兼容协议 v4.2、v4.1、4.0。

主要的功能如下：

- 低功耗蓝牙模式：
  - 支持速率（1M/2M）；
  - 支持所有的包格式（广播包/拓展广播包/数据包等）；
  - 支持数据的加解密；
  - 支持数据流的处理（冗余校验、白化）；
  - 支持两种跳频模式；
  - BLE 最大发射功率 19dBm，
- 经典蓝牙模式：
  - 支持 BR，EDR2，EDR3；
  - 支持 ACL、CSB、SCO 以及 eSCO 的所有包类型；
  - 支持数据加解密（E0 加密以及 AES-CCM 加密）；
  - 支持数据流的处理（HEC、CRC、Whitening、FEC2/3、FEC1/3）；
  - 支持音频数据的编解码处理（CVSD 以及 a/μ-Law）；
  - 支持自适应跳频；
  - BR 最大发射功率 17dBm，EDR2/EDR3 最大发射功率 13dBm
- 以及：
  - 支持 AMBA AHB 总线的访问；
  - 支持 WIFI 的共存机制。
  - 单 ble 的场景下:
    - SF32LB573/SF32LB575/SF32LB577 等锂电池供电系列最大链接数是 4 条
    - SF32LB57A/SF32LB57B/SF32LB57D 等常规供电系列最大链接数是 8 条
  - 单经典蓝牙的场景下:
    - SF32LB573/SF32LB575/SF32LB577 等锂电池供电系列最大链接数是 2 条
    - SF32LB57A/SF32LB57B/SF32LB57D 等常规供电系列最大链接数是 7 条

17.2 蓝牙共存接口

17.2.1 简介

蓝牙共存接口可用于实现 WIFI 共存。共存接口共有 4 根信号线，包括 3 根输出信号 BT_ACTIVE, BT_PRIORITY, BT_COLLISION 和 1 根输入信号 WLAN_ACTIVE，支持多种配置模式，可兼容常见的单线，2 线，3 线和 4 线共存接口，支持外部仲裁或内部仲裁方案。输出信号用于表示蓝牙工作状态，输入信号可以控制蓝牙的收发行为。

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输入与输出信号可直接连接到芯片 IO，也可触发 PTC 事件。

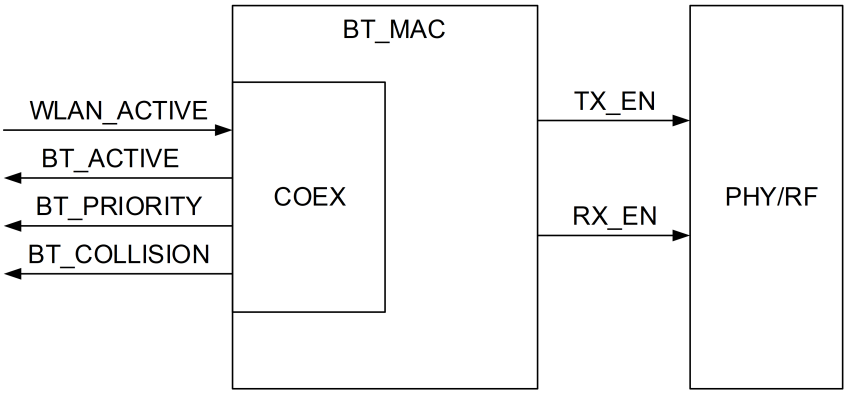


图 17-1: 蓝牙共存示意图

17.2.2 主要特性

- 4 线接口，可兼容单线，2 线，3 线和 4 线方案
- 蓝牙工作状态输出，极性可配置，并可合并优先级输出
- 蓝牙工作优先级输出，各场景优先级可配，并可调整阈值
- 蓝牙频点冲突输出，可配置冲突频点
- WIFI 工作状态输入，极性可配置，可屏蔽蓝牙收发

17.2.3 输出信号 BT_ACTIVE

BT_ACTIVE 用于表示蓝牙是否正在工作，极性可配置。该信号可以通过 BT_MAC 的状态机产生，也可以通过寄存器配置成指定电平。BT_ACTIVE 可以表示蓝牙一次完整的事件单元，比如一次 BLE 广播的 3 个信道轮询，或者一次 BT 的 sniff 交互等；也可以表示蓝牙的单次发送，或者单次接收。从 BT_ACTIVE 生效到蓝牙开始收发包的时间间隔 TRF 通常为数十 us。BT_ACTIVE 还可合并 BT_PRIORITY 的功能，即仅当 BT_PRIORITY 为高优先级时才输出正在工作的状态。BT_ACTIVE 信号通常用于向外部仲裁器发送蓝牙传输请求，也可直接用于控制外部射频开关。

配置 BT_ACTIVE 的流程是：

1. 通过 BT_MAC 的寄存器 BTCOEXIFCNTL2.PTA_ACTPOL 配置 BT_ACTIVE 的输出极性，默认为 0，即高电平表示蓝牙工作。极性取反时低电平表示蓝牙工作；
2. 通过 BTCOEXIFCNTL2.PTA_ACTSEL 寄存器选择 BT_ACTIVE 的覆盖范围，默认为 0，覆盖蓝牙一次完整的事件单元。如果改为 1，则只覆盖蓝牙发送，为 2 时只覆盖蓝牙接收；
3. 如果需要 BT_ACTIVE 合并 BT_PRIORITY 的功能，将 BTCOEXIFCNTL2.PTA_ACTMODE 寄存器置 1。默认极性时，高电平表示蓝牙工作并且优先级为高。极性取反时低电平表示蓝牙工作并且优先级为高。

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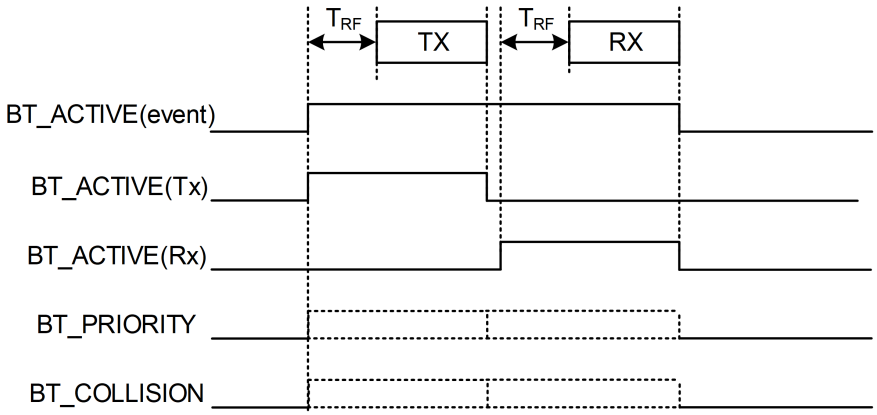


图 17-2: 输出信号示意图

17.2.4 输出信号 BT_PRIORITY

BT_PRIORITY 用于表示蓝牙工作的优先级，高/低电平分别表示高/低优先级。该信号可以通过 BT_MAC 的状态机产生，也可以通过寄存器配置成指定电平。蓝牙 MAC 可以设定在不同场景 (如广播，建立连接，维持连接，通话，重传等) 收发行为对应的优先级，并可以配置统一的优先级阈值，当蓝牙收发行为对应的优先级不低于优先级阈值时，BT_PRIORITY 拉高，否则 BT_PRIORITY 为低。从 BT_PRIORITY 生效到蓝牙射频开启收发的时间间隔等于 TRF。BT_PRIORITY 还可合并 BT_COLLISION 的功能，即仅当共存频点冲突时才输出高优先级。

配置输出信号 BT_PRIORITY 的流程是：

1. 通过 BTMPRIO0/1/2 和 BLEMPRIO0/1/2 寄存器设置 BT 和 BLE 各种蓝牙场景的优先级。芯片上电以后各场景的优先级已经分配了默认的初始值，可以根据需求进一步调整；
2. 通过 BTCOEXIFCNTL1.WLCPTXTHR 寄存器配置优先级阈值，当 BT 和 BLE 优先级大于或等于优先级阈值时，才产生有效输出；
3. 如果需要 BT_PRIORITY 合并 BT_COLLISION 的功能，即仅当频点冲突时才产生有效输出，需将 BTCOEXIFCNTL2.PTA_PRIOMODE 寄存器置为 1。

17.2.5 输出信号 BT_COLLISION

BT_COLLISION 用于表示蓝牙是否存在共存频点冲突，高电平表示发生冲突，低电平表示无冲突。该信号可以通过 BT_MAC 的状态机产生，也可以通过寄存器配置成指定电平。如果要使用这个功能，需在 BT_MAC 寄存器中预先标记出可能发生冲突的频点。当蓝牙跳频到标记的频点上进行收发时，BT_COLLISION 输出高电平，否则输出低电平。从 BT_COLLISION 生效到蓝牙射频开启收发的时间间隔等于 T_{RF}。

使用该功能时，需通过 COEXCHN0/1/2 寄存器配置 2402MHz 到 2480MHz 中的每个频点是否会产生共存冲突。会产生冲突的频点对应寄存器比特应当置 1，否则置 0。

17.2.6 输入信号 WLAN_ACTIVE

WLAN_ACTIVE 用于表示外部 WIFI 的工作状态，可作为允许蓝牙工作的使能信号使用，有效电平可配置。WLAN_ACTIVE 的影响可以配置为下列行为中的一种：

1. 不影响蓝牙收发；

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2. 禁止蓝牙低于优先级阈值的发送；
3. 禁止蓝牙低于优先级阈值的接收；
4. 禁止蓝牙低于优先级阈值的接收和发送；
5. 禁止蓝牙所有发送；
6. 禁止蓝牙所有接收；
7. 禁止蓝牙所有接收和发送；

下图是 WLAN_ACTIVE 影响蓝牙收发的一个示例。当 WLAN_ACTIVE 有效时，蓝牙的发送与接收都被立即禁止，但当优先级为高时不受影响。

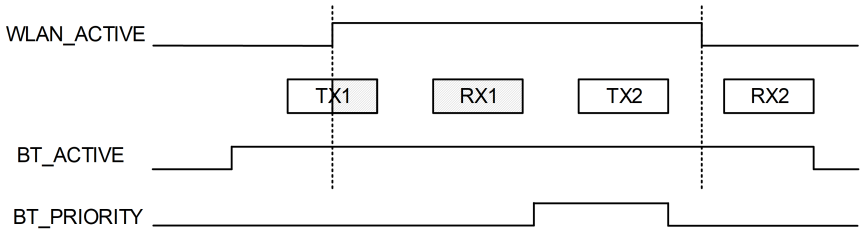


图 17-3: WLAN_ACTIVE 影响示例

配置输入信号 WLAN_ACTIVE 的流程是：

1. 通过 BTCOEXIFCNTL2.PTA_WLANPOL 寄存器配置 WLAN_ACTIVE 的有效电平，默认值 0 表示高电平有效；
2. 如果需要在 WLAN_ACTIVE 为有效电平时禁用蓝牙发射，将 BTCOEXIFCNTL2.PTA_MASKTX 和 ABORTTX 寄存器写 1；如果需要在 WLAN_ACTIVE 为有效电平时禁用蓝牙接收，将 BTCOEXIFCNTL2.PTA_MASKRX 和 ABORTRX 寄存器写 1；
3. 如果只想禁用蓝牙低优先级行为，将 BTCOEXIFCNTL2.PTA_PRIOMODE 寄存器置为 1。

17.2.7 配置共存接口的流程

1. 配置所需输出信号与输入信号；
2. 配置 PINMUX，将所需的输入和输出信号映射到指定 IO 上；
3. 使能共存接口，将 BT_MAC 的寄存器 BTCOEXIFCNTL0.WLANCOEX_EN 和 BLECOEXIFCNTL0.WLANCOEX_EN 置 1。

17.2.8 IO 映射

IO 映射有两种方式。

第一种方式，共存的输入输出信号可映射到任意 IO(PA)，但其中输出信号 (如 BT_ACTIVE) 仅支持高电平有效，输入信号极性可配置。此方式下 HPSYS 可以进入 deepsleep 模式，但不能进入 standby 或 hibernate 模式。将共存信号映射到某个 IO(PA) 时，需首先将 IO 映射为 PA_TIM 功能，再进一步在 HPSYS_CFG 寄存器中指定其功能，并将 LPSYS_CFG->DBGR.BITEN_L 设置为 0xff。例如若要让 PA01 作为 BT_ACTIVE 使用，不仅需设置 HPSYS_PINMUX 寄存器的 PAD_PA01.FSEL 为 5(对应 PA_TIM)，也需要设置 HPSYS_CFG 寄存器的 PTA_PINR.BT_ACTIVE 为 1(对应 PA01)。应注意若将多个功能指定到同一个 IO 会引起功能错误，比如上例中应确保 HPSYS_CFG 中其它的所有 PA_TIM 功能配置寄存器 (如 PTA_PINR.BT_COLLISION, GPTIM1_PINR.CH1_PIN 等) 未配置为 1(对应 PA01)。

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第二种方式配置更为复杂，共存的输入输出信号仅可映射到 PA00~PA03，优点是电平极性可配置。此方式下 HPSYS 可以进入 deepsleep 或 standby 模式，但不能进入 hibernate 模式。此方式配置 IO 时，需先将对应 HPSYS_PINMUX 中对应 IO 设置为高阻 (GPIO 模式关闭输出且 PE=0)，将 LPSYS_PINMUX 中对应 IO 设置为 PB_TIM 功能，并进一步在 LPSYS_CFG 寄存器中指定其 PTA 功能。例如若要让 PA01 作为 BT_ACTIVE 使用，需设置 HPSYS_PINMUX 寄存器的 PAD_PA01.FSEL/PE 为 0，并设置 LPSYS_PINMUX 寄存器的 PAD_PB01.FSEL 为 2(对应 PB_TIM)，以及 LPSYS_CFG 寄存器的 PTA_PINR.BT_ACTIVE 为 1(对应 PA01)。

17.2.9 外部仲裁的 3 线方案示例

本示例中蓝牙与 WIFI 共用一个天线，使用射频开关进行切换，控制信号来自于 WIFI 芯片。仲裁是由 WIFI 芯片完成，根据蓝牙输出的 BT_ACTIVE 和 BT_PRIORITY 信号决定是否将天线使用权交给蓝牙，并可在 WIFI 工作时通过 WLAN_ACTIVE 信号关闭蓝牙收发。

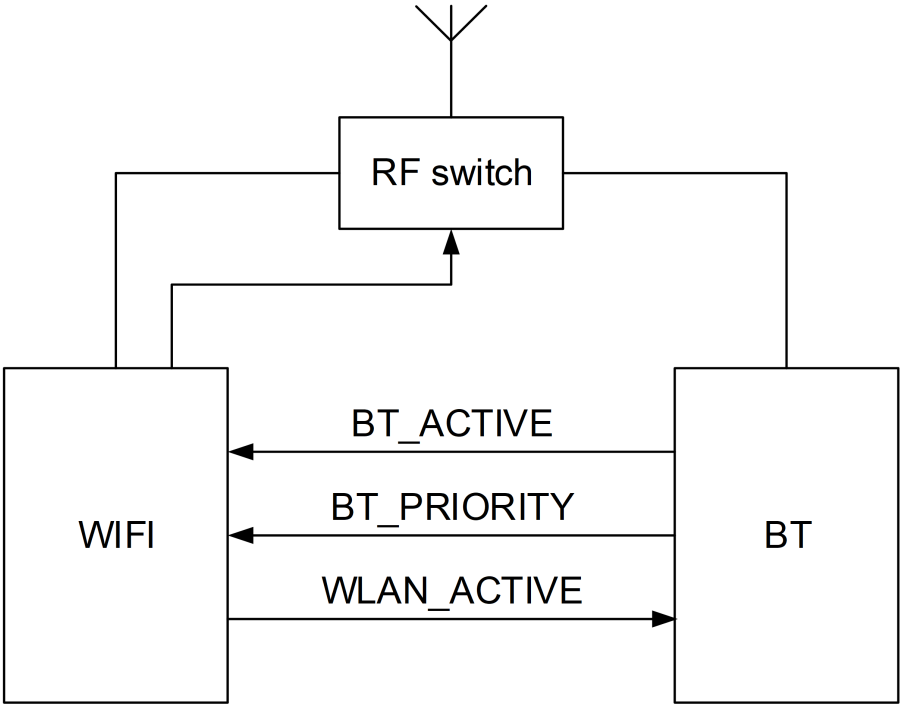


图 17-4: 外部仲裁的 3 线方案示例

17.2.10 内部仲裁的单线方案示例

本示例中蓝牙与 WIFI 共用一个天线，使用射频开关进行切换，控制信号来自于蓝牙。仲裁是由蓝牙完成，用 BT_ACTIVE 信号控制天线使用权，并通知 WIFI 芯片。如果需要让出部分时隙给 WIFI，可以打开 BT_ACTIVE 合并 BT_PRIORITY 的功能，并根据工作场景调节优先级阈值，空出一部分低优先级的时隙供 WIFI 使用。

如果 WIFI 能够输出表示工作状态的信号，该方案可以升级为 2 线模式。将 WIFI 的输出连接到 WLAN_ACTIVE 输入，蓝牙能够在 WIFI 需要工作时屏蔽低优先级的蓝牙收发，而当 WIFI 不工作时不受影响。

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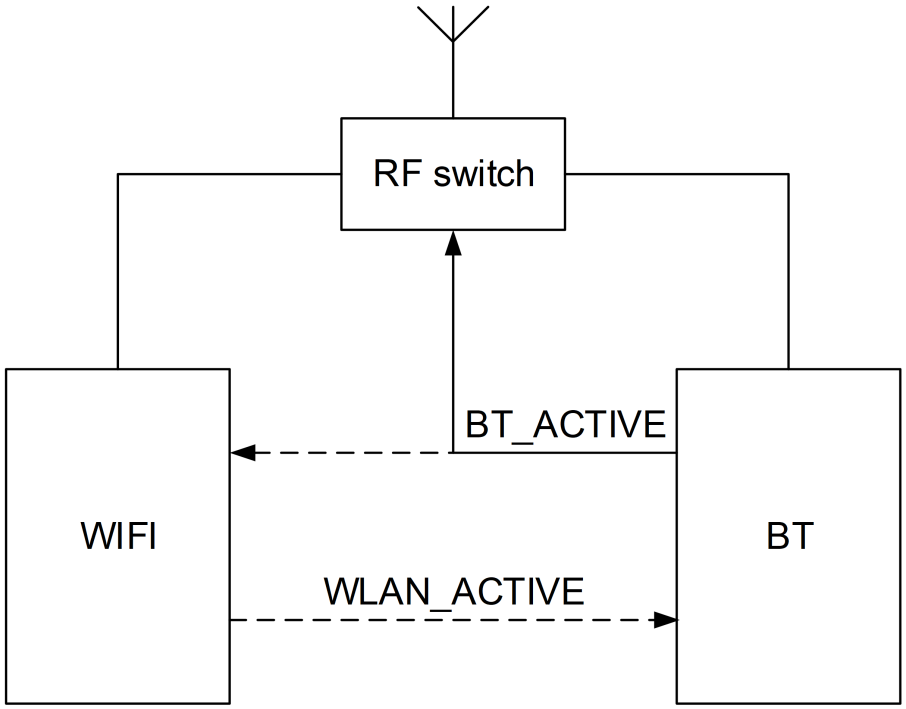


图 17-5: 内部仲裁的单线或 2 线方案示例

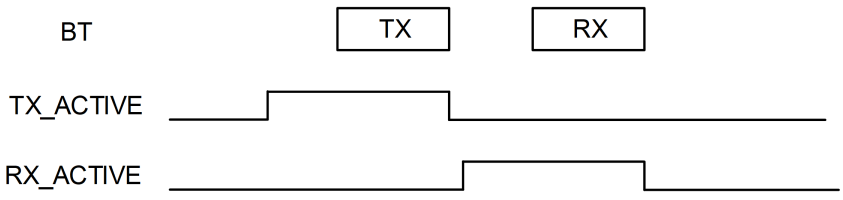
17.3 外接 PA(功率放大器) 和 LNA(低噪声放大器)

在芯片外部连接 PA(功率放大器) 和 LNA(低噪声放大器) 模块，可以进一步提高蓝牙的发射功率和灵敏度，实现数百米至数公里级别的蓝牙传输。

功率放大器和低噪声放大器通常由控制 IO 开启和关闭。功率放大器应在蓝牙发射时开启，在蓝牙接收时关闭。低噪声放大器应在蓝牙接收时开启，在蓝牙发射时关闭。因此芯片应根据蓝牙的收发行为，通过 IO 输出特定电平。

如果外部使用的是集成控制的模块，仅需一根控制信号，那么利用共存接口输出的 BT_ACTIVE 信号就可以同时控制外部功率放大器和低噪声放大器的工作。BT_ACTIVE 可以设置为高电平代表发送，也可设置为低电平代表发送。具体配置方法可参考蓝牙共存接口的输出信号 BT_ACTIVE 配置流程。

如果外部使用的是独立控制的模块，需要两根独立的控制信号分别控制功率放大器和低噪声放大器，那么可将代表蓝牙发射的 TX_ACTIVE 信号和代表蓝牙接收的 RX_ACTIVE 信号输出。



TX_ACTIVE 信号用于表示蓝牙处于发射状态，高电平有效，可通过特定 IO 输出。配置方法见下表。

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module	HPSYS_PINMUX	LPSYS_PINMUX	LPSYS_CFG			HPSYS_CFG		
register	PAD_PAxx	PAD_PBxx	DBGR		SYSCR	DBGR		
field	(xx 是 PA 编号，例如 PA03 时 xx=03)		SEL_L	BITEN_L	DBG_SWAP	SWAP	SEL_L	BITEN_L
PA01	0xf	0x6	0x0	0xf0	0x2	/	/	/
PA03	0xf	0x6	0x7	0xf0	0x2	/	/	/
PA03	0x9	0x0	0x0	0xff	0x2	0x0	0x9	0xff
PA05	0x9	0x0	0x7	0xff	0x2	0x0	0x9	0xff
PA07	0x9	0x0	0x0	0xff	0x0	0x0	0x9	0xff
PA09	0x9	0x0	0x7	0xff	0x0	0x0	0x9	0xff
PA37	0x9	0x0	0x0	0xff	0x2	0x1	0x9	0xff
PA40	0x9	0x0	0x7	0xff	0x2	0x1	0x9	0xff
PA42	0x9	0x0	0x0	0xff	0x0	0x1	0x9	0xff
PA44	0x9	0x0	0x7	0xff	0x0	0x1	0x9	0xff

RX_ACTIVE 信号用于表示蓝牙处于接收状态，高电平有效，可通过特定 IO 输出。配置方法见下表。

module	HPSYS_PINMUX	LPSYS_PINMUX	LPSYS_CFG			HPSYS_CFG		
register	PAD_PAxx	PAD_PBxx	DBGR		SYSCR	DBGR		
field	(xx 是 PA 编号，例如 PA02 时 xx=02)		SEL_L	BITEN_L	DBG_SWAP	SWAP	SEL_L	BITEN_L
PA00	0xf	0x6	0x0	0xf0	0x2	/	/	/
PA02	0xf	0x6	0x7	0xf0	0x2	/	/	/
PA02	0x9	0x0	0x0	0xff	0x2	0x0	0x9	0xff
PA04	0x9	0x0	0x7	0xff	0x2	0x0	0x9	0xff
PA06	0x9	0x0	0x0	0xff	0x0	0x0	0x9	0xff
PA08	0x9	0x0	0x7	0xff	0x0	0x0	0x9	0xff
PA31	0x9	0x0	0x0	0xff	0x2	0x1	0x9	0xff
PA39	0x9	0x0	0x7	0xff	0x2	0x1	0x9	0xff
PA4	0x9	0x0	0x0	0xff	0x0	0x1	0x9	0xff
PA43	0x9	0x0	0x7	0xff	0x0	0x1	0x9	0xff

TX_ACTIVE 与 RX_ACTIVE 同时使用时，应当选择同一套配置的两个 IO，例如 PA01 与 PA00，或 PA37 与 PA31 等，否则配置会冲突。

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18 PTM

18.1 PTM

18.1.1 简介

PTM(Parallel Task Machine) 是一个能够并行处理多个任务的小型处理器。PTM 内部包含 4 个独立运行的处理核，每个核能够从内置存储器 (TCM) 或系统总线获取自定义格式的指令并执行，实现总线地址读写、数据运算、判断、跳转、IO 读写、等待触发、延时等多种功能。利用一套简洁高效的自定义指令集，用户能够以周期级的精度控制每个核的运行，可满足 IO 读写的时序，也可实现对特定触发条件的快速响应。每个处理核可同时处理多达 16 路 IO 的输入输出，并内置带有 DMA 接口的读写 FIFO，便于构造自定义通信接口。处理核可访问 AHB 总线，从总线地址获取指令执行，或读写总线上的存储器和寄存器数据。处理核运行过程中可自定义产生中断与 CPU 交互。多个核之间也可基于事件通知机制协同工作。用户可基于 PTM 开发多种自定义功能，例如自定义接口协议，自定义 PWM，内存数据批量运算，多模块互联调度，自动传感器采集等。

18.1.2 主要特性

- 两级流水线，4 核并行处理
- 32 位自定义指令集，包括 4 条基础指令与 4 条访存指令
- 每个核在 TCM 上执行的指令数目为 2~64，从总线执行时无上限
- 基础指令具有严格的时序控制，1 个周期执行 1 条指令
- 运算包括与、或、异或、移位、有符号数加法、比特交换等
- 可基于条件判断并跳转，实现分支和循环
- 可等待事件触发或等待固定延时
- 每个核内置 2 个 32 位和 2 个 16 位通用寄存器
- 每个核内置支持 DMA 接口的 32 位 FIFO，深度为 4 或 8
- 16 个 IO 通道 CH0~CH15，可映射到每个核的 16 路 IO
- 每个核可基于 FIFO 输出或输入多达 16 路 IO，同时单独控制其中 2 个 IO 输出
- 16 个内部事件通知用于多核协同，其中 8 个可对应 CPU 中断
- 每个核可独立复位、启动、暂停以及单步调试

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18.1.3 结构图

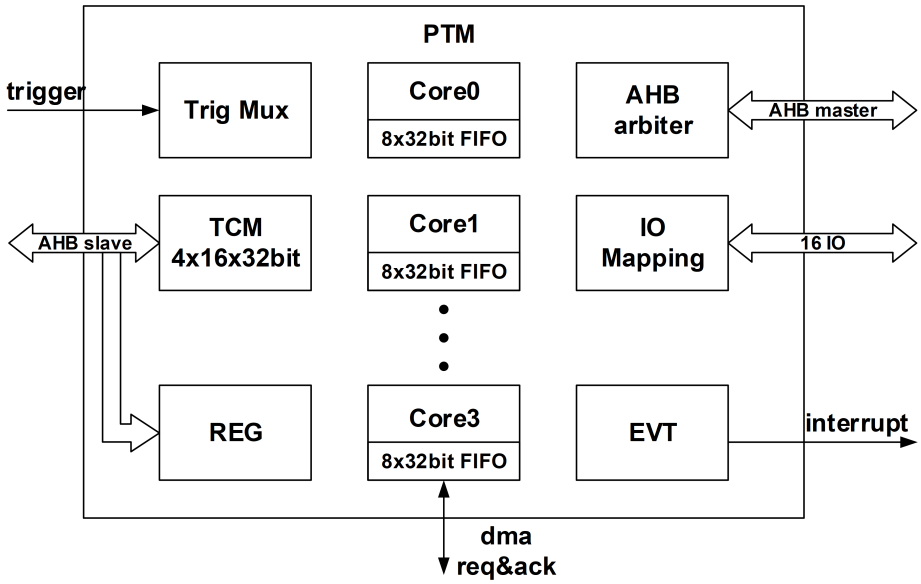


图 18-1: PTM 结构图

18.1.4 时钟频率

PTM 模块的工作时钟等于系统总线时钟 hclk。每个核的运行时钟可以基于该工作时钟整数倍分频，分频比为(CCRx.PSC+1)。例如 CCR0.PSC=0 时，Core0 的运行时钟频率等于 hclk；CCR7.PSC=15 时，Core7 的运行时钟频率等于 hclk/16。这是为了满足某些应用精确控制 IO 时序的要求，可使处理核运行在特定时钟频率上。

18.1.5 基本工作流程

PTM 包含 4 个处理核，每个核均能够独立执行指令，从而并行处理多个任务。

启动处理核之前，应当首先将指令存入其执行地址，随后将 CER.RSTx 置 1 复位核，之后完成该核的寄存器配置，并将 CER.ENx 置 1 启动处理核。

每个核启动后，固定从地址 0 开始取出第一条指令并执行，之后顺序执行地址 1, 地址 2... 等地址中的指令。

在指令执行过程中，如果遇到跳转指令，会判断条件是否满足，如果满足则跳转到目标地址，否则继续向后执行。

在指令执行过程中，如果遇到等待指令，会判断等待条件是否满足，如果满足则继续向后执行，否则会在下一个周期重新判断。

在指令执行过程中，如果执行地址不为 0，且等于预先定义的结束地址 (CCRx.END0 和 CCRx.END1) 中的任何一个，该条指令执行完成后不会继续向后执行，而是基于当前核的 CCRx.REP 进行判断：

- 如果 CCRx.REP 不为 0，跳转到 0 地址继续执行，并自动将 CCRx.REP 减 1(CCRx.REP=255 时不会减 1，可实现无限循环)。
- 如果 CCRx.REP 为 0，当前任务执行完成，处理核停止运行。如果 IER.EVTAUTOx 为 1，会自动产生事件通知 EVTx，且当 IER.EVTIEx 为 1 时可产生 CPU 中断。

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18.1.6 指令运行时序

处理核为两级流水线架构，取指令与指令执行可同步进行。

每一个运行时钟 (经过 CCR0.PSC 分频以后的时钟) 周期，处理核能够完成一条指令的执行，同时完成下一条指令的获取，除以下情况外：

- 指令并非位于 TCM，而是在总线地址上，此时取指令可能需要多个周期；
- 执行访存指令时，可能需要多个周期；
- 指令中指定了延时，在下一条指令执行之前会额外等待 N 个周期的延时；
- WAIT 指令中，等待条件不满足，会持续等待；
- 指令涉及写 IFIFO，但 IFIFO 已满且设置了 ICRx.IBLOCK=1，会等待 IFIFO 取出；
- 指令涉及读 OFIFO，但 OFIFO 为空且设置了 OCRx.OBLOCK=1，会等待 OFIFO 存入。

除了这些情况外，每条指令的执行时间为精确的 1 个运行时钟周期，因此可用于实现精确的时序控制。

18.1.7 流水线暂停

指令运行过程中，当满足下列任一条件时，流水线会暂停，直到所有条件均不再满足才会继续执行。

- 指令未取出。有两种场景会发生指令未准备好，需要等待的情况：处理核刚启动时，0 地址的第一条指令尚未取出；处理核从总线地址执行指令时，取指令需要多个时钟周期，超出了指令本身执行的时间。
- 指令访存未完成。访存指令对总线地址进行读写时，需要多个时钟周期，此时流水线暂停，直到总线访问结束。
- 指令中包含延时。流水线会依照指令中设定的延时周期数暂停。
- 指令内包含等待条件。在等待条件满足前，流水线会暂停。
- 指令执行中需要写 IFIFO，但 IFIFO 已满且设置了 ICRx.IBLOCK=1。
- 指令执行中需要读 OFIFO，但 OFIFO 为空且设置了 OCRx.OBLOCK=1。

18.1.8 TCM 指令数目限制

分配处理核的任务时需要遵照如下规则：

如果 CoreN 在 TCM 中的指令数目每超出 1 个 16 的倍数，其后顺序编号的一个核需被禁用。例如，如果 Core0 的 TCM 指令数目为 17，那么 Core1 将无法使用，其它 Core 可以使用。如果 Core0 的 TCM 指令数目为 64，那么其它所有核将无法使用。如果 Core3 的 TCM 指令数目为 17，那么 Core0 将无法使用，其它 Core 可以使用。

Core0 TCM 指令数目	Core 1	Core 2	Core 3
<=16	√	√	√
17~32	X	√	√
33~48	X	X	√
49~64	X	X	X

如下是具体的解释说明。

PTM 内置 TCM 存储器，可存放 64 条 32 位指令，每个指令空间分别以 TCM0~TCM63 指代。可以通过 PTM 的寄存器接口读写 TCM 内容，地址偏移为 0x200~0x2fc。

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每个核都可以通过地址 0~63 访问 TCM 空间，但访问 TCM 时附加了不同偏移。具体的映射规则是，CoreN 的 0 地址指向 TCM(16*N)，并依次递增直到 TCM63，再下一个地址又返回到 TCM0，如下表所示。例如，Core1 的 0 地址指向 TCM16，63 地址则指向 TCM15。

Addr	Core 0	Core 1	Core 2	Core 3
0	TCM0	TCM16	TCM32	TCM48
1	TCM1	TCM17	TCM33	TCM49
2	TCM2	TCM18	TCM34	TCM50
...	...	...	...	...
16	TCM16	TCM32	TCM48	TCM0
...	...	...	...	...
63	TCM63	TCM15	TCM31	TCM47

每个核启动时都从各自的 0 地址开始执行，但是不同核的 0 地址指向 TCM 的不同区域。如果每个核的指令数目都不超过 16 条，那么所有核都能够并行执行且不发生冲突。但假如某个核在 TCM 中需要执行的指令超出 16 条，那么其指令会顺序放置到其它核的 0 地址上，从而影响其它核的运行。

所幸基于简洁高效的自定义指令集，在 16 条指令以内已经足够完成简单的模块互联调度工作，并可实现若干常见的接口功能，例如 PWM，SPI，I2S，LED 等。如果指令数超过 16 条，每多 16 条指令也仅影响额外的一个核。如果指令数目较多且需多核同时运行，可以跳转到总线地址上执行指令。

18.1.9 从总线地址执行指令

从 0 地址启动以后，处理核可以通过 JMP 指令跳转到 X 或 Y 寄存器保存的总线地址，执行存放在该地址上的指令，并顺序执行在该地址之后储存的指令。在总线地址上执行指令的数量没有限制，可以实现更加复杂的功能，并可避免对其它核的影响。

在总线地址上执行时也支持偏移跳转，但需注意指令中的偏移地址增减 1 对应总线地址增减 4，因为每条指令占据 4 个字节的总线地址空间。

访问总线地址的周期数存在不确定性，因此在总线地址上执行时，每条指令的执行周期数也不确定。

处理核跳转到总线地址执行后，仍可通过 JMP 指令跳转回 TCM。每个核预先定义的结束地址 (CCRx.END0 和 CCRx.END1) 仅支持 TCM 地址 (1~63)，因此在结束前从总线地址跳转回 TCM 是较为常用的流程。

18.1.10 通用寄存器

每个核都包含 2 个 32 位和 2 个 16 位通用寄存器，可以参与指令执行，也可以由 CPU 通过访问寄存器直接赋值或读取。具体通用寄存器包括：

- 32 位通用寄存器 X。其高 16 位和低 16 位也可以分拆作为 XH 和 XL 两个通用寄存器使用。CPU 可通过 Xx 寄存器直接读写 X。X 通用寄存器也可以与 OFIFO 交互，参与 IO 指令的输出功能。
- 32 位通用寄存器 Y。其高 16 位和低 16 位也可以分拆作为 YH 和 YL 两个通用寄存器使用。CPU 可通过 Yx 寄存器直接读写 Y。Y 通用寄存器也可以与 IFIFO 交互，参与 IO 指令的输入功能。
- 16 位通用寄存器 A。CPU 可通过 Ax 寄存器直接读写 A。A 通用寄存器也可以参与 JMP 指令的自减条件，便于构建循环。

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- 16 位通用寄存器 B。CPU 可通过 Bx 寄存器直接读写 B。B 通用寄存器也可以参与 JMP 指令的自减条件，便于构建循环。

通用寄存器会被 CER.RSTx 复位成 0，因此程序执行前应当先进行复位，再初始化通用寄存器。

18.1.11 指令集

PTM 基于 32 位自定义指令集，共包含 8 条指令，全部都是 32 位，其中 4 条为基础指令，另外 4 条为访存指令。

基础指令包括：

- SET，运算并赋值。可获取通用寄存器、IO、OFIFO 等数据源的值，与 16 位立即数进行运算，再向通用寄存器、IO、IFIFO、EVT 等目标赋值。
- WAIT，等待条件满足并延时。可等待芯片各模块的事件触发、IO、FIFO 空满状态等条件，并在条件满足后延时 0~65535 个运行时钟周期，再继续执行下一条指令。
- JMP，条件跳转并延时。可判断通用寄存器、IO、EVT 是否满足特定条件，如果满足则跳转到相对偏移地址 (-127~127) 或绝对地址 (TCM 或总线地址)，并延时 0~63 个周期，否则继续执行下一条指令。
- IO，输入输出并延时。可从 X 寄存器输出 0~16 个 bit 到 IO 端口，或从 IO 端口输入 0~16 个 bit 到 Y 寄存器，同时单独控制其中 2 个 IO 输出，之后延时 0~63 个周期。

基础指令在 TCM 中运行时，执行时间为 1 个运行时钟周期，除等待、延时或 FIFO 拥堵等情况外。

访存指令包括：

- LDM，读取立即数地址。从 4 字节对齐的立即数地址读取 32 位数据存入 X 或 Y 寄存器，可读取的地址范围是 0x0~0x7FFFFFFC。
- LDR，读取寄存器偏移地址。以 X 或 Y 寄存器中保存的数据偏移 16 位立即数为总线地址，读取 32 位数据存入通用寄存器，偏移范围为-32768~32767，偏移后的地址应满足 4 字节对齐。
- STM，写入立即数地址。将 X 或 Y 寄存器的数据写入 4 字节对齐的立即数地址，可写入的地址范围是 0x0~0x7FFFFFFC。
- STR，写入寄存器偏移地址。以 X 或 Y 寄存器中保存的数据偏移 16 位立即数为总线地址，将通用寄存器的数据写入该地址，偏移范围为-32768~32767，偏移后的地址应满足 4 字节对齐。

访存指令的执行时间取决于总线繁忙程度，通常不低于 4 个总线时钟周期。

18.1.12 SET 指令

Rn 经过与 16 位立即数 Imm16 的运算后写入 Rd。运算位宽为 32 位。

伪代码：`Rd = Rn op Imm16`

Rn 参数定义:

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值	名称	描述
0	X	读出通用寄存器 X 保存的数据
1	Y	读出通用寄存器 Y 保存的数据
2	A	读出通用寄存器 A 保存的数据，高 16 位补 0
3	B	读出通用寄存器 B 保存的数据，高 16 位补 0
4	XL	读出通用寄存器 XL 保存的数据，高 16 位补 0
5	XH	读出通用寄存器 XH 保存的数据，高 16 位补 0
6	YL	读出通用寄存器 YL 保存的数据，高 16 位补 0
7	YH	读出通用寄存器 YH 保存的数据，高 16 位补 0
11	IN	读出当前处理核 16 位 IO 输入的值，高 16 位补 0
12	FIFO	OFIFO 非空：从 OFIFO 中取出一个 32 位数据；OFIFO 空：OCRx_OBLOCK 为 0 时，读出 0，否则流水线暂停直到 OFIFO 非空
15	0	读出 0
others	reserved	未定义，避免使用

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Rd 参数定义:

值	名称	描述
0	X	运算结果写入通用寄存器 X
1	Y	运算结果写入通用寄存器 Y
2	A	运算结果的低 16 位写入通用寄存器 A
3	B	运算结果的低 16 位写入通用寄存器 B
4	XL	运算结果的低 16 位写入通用寄存器 XL
5	XH	运算结果的低 16 位写入通用寄存器 XH
6	YL	运算结果的低 16 位写入通用寄存器 YL
7	YH	运算结果的低 16 位写入通用寄存器 YH
8	OS	当前处理核 IO 输出值按 bit 置 1，仅置位运算结果的低 16 位里为 1 的 bit
9	OC	当前处理核 IO 输出值按 bit 清 0，仅清除运算结果的低 16 位里为 1 的 bit
10	OEREV	当前处理核 IO 输出使能按 bit 取反，仅取反运算结果的低 16 位里为 1 的 bit
12	FIFO	IFIFO 未满：将运算结果存入 IFIFO；IFIFO 满：OCRx_OBLOCK 为 0 时，读出 0，否则流水线暂停直到 OFIFO 非空
13	EVTS	EVT 标志按 bit 置 1，仅置位运算结果的低 16 位里为 1 的 bit
14	EVTC	EVT 标志按 bit 清 0，仅清除运算结果的低 16 位里为 1 的 bit
others	reserved	未定义，避免使用

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Op 参数定义:

值	名称	描述
0	NOP	Rd=Rn，无运算
1	XOR	Rd=Rn XOR Imm16，按位异或运算
2	AND	Rd=Rn AND Imm16，按位与运算
3	OR	Rd=Rn OR Imm16，按位或运算
4	LSL	Rd=Rn << Imm16，逻辑左移，LSB 补 0
5	LSR	Rd=Rn >> Imm16，逻辑右移，MSB 补 0
6	ADD	Rd=Rn + Imm16，有符号数加法运算，Imm16 视为 16 位有符号数
7	ACCUM	Rd=Rn + Rd。操作数为 16bit 时，高位补 0。仅支持通用寄存器的累加，即 Rd 参数的值为 0~7 时。
8	REV32	32 位 bit 次序翻转。Rd[31:0]=Rn[0:31]
9	REV16	16 位 bit 次序翻转。Rd[31:16]=Rn[16:31], Rd[15:0]=Rn[0:15]
10	REV8	8 位 bit 次序翻转。Rd[31:24]=Rn[24:31], Rd[23:16]=Rn[16:23], Rd[15:8]=Rn[8:15], Rd[7:0]=Rn[0:7]
others	reserved	未定义，避免使用

18.1.13 WAIT 指令

判断当前单 bit 信号 Src 是否等于 Pol，如果相等则结束判断，并延时 Dly 个周期，否则等待下一个周期重复上述判断流程。

伪代码：`wait until Src == Pol, then delay Dly`

Src 参数定义:

值	名称	描述
0	NULL	0
1~127	TRIG1~TRIG127	芯片内各模块产生的事件触发信号
128~215	PA00~PA79	芯片某个 IO(PA) 的输入值
216	OFIFO_EMPTY	OFIFO 空标志
217	OFIFO_FULL	OFIFO 满标志
218	IFIFO_EMPTY	IFIFO 空标志
219	IFIFO_FULL	IFIFO 满标志
224~239	IN0~IN15	当前处理核的某个 IO 输入
240~255	EVT0~EVT15	某个事件通知标志
others	reserved	未定义，避免使用

如果运行在总线地址而非 TCM 上，WAIT 指令不支持连续运行，即两条 WAIT 指令之间必须间隔至少一条其它

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指令，否则可能运行出错。

18.1.14 JMP 指令

判断 Rn/In/EVTn 与 Rm 是否满足 Cond 条件，如果满足则延时 Dly 个周期再跳转到 Tgt 地址，否则顺序执行下一条指令。

伪代码：

```
if Rm and Rn match Cond,
    PC = Tgt, then delay Dly,
else
    PC = PC+1
```

Rn 与 Rm 参数定义:

值	名称	描述
0	X	通用寄存器 X 保存的数据
1	Y	通用寄存器 Y 保存的数据
2	A	通用寄存器 A 保存的数据，高 16 位补 0
3	B	通用寄存器 B 保存的数据，高 16 位补 0
4	XL	通用寄存器 XL 保存的数据，高 16 位补 0
5	XH	通用寄存器 XH 保存的数据，高 16 位补 0
6	YL	通用寄存器 YL 保存的数据，高 16 位补 0
7	YH	通用寄存器 YH 保存的数据，高 16 位补 0
14	ALL1	0xFFFFFFFF
15	0	0
others	reserved	未定义，避免使用

In 参数定义:

当前处理核的某个 IO 输入，0~15 分别代表 IN0~IN15。

Cond 参数定义:

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值	条件	描述
0	Rn=Rm	当 Rn 与 Rm 相等时条件满足
1	Rn≠Rm	当 Rn 与 Rm 不相等时条件满足
2	In=Rm[0]	当 In 与 Rm 的 bit0 相等时条件满足
3	EVTn=Rm[0]	当 EVTn 与 Rm 的 bit0 相等时条件满足
4	Rn−=Rm	当 Rn 与 Rm 相等时条件满足，随后 Rn 自减 1。Rn 只能选择通用寄存器 A 或通用寄存器 B
5	Rn−≠Rm	当 Rn 与 Rm 不相等时条件满足，随后 Rn 自减 1。Rn 只能选择通用寄存器 A 或通用寄存器 B
6	Rn>Rm	当 Rn 大于 Rm 时条件满足
7	Rn<Rm	当 Rn 小于 Rm 时条件满足

Tgt 参数定义:

值	目标地址	描述
-127~127	PC+Tgt	跳转到当前地址的偏移地址，可向前或向后跳转。当前地址为总线地址时，地址每偏移 1 代表总线地址偏移 4。
128~255	Tgt-128	跳转到 TCM 中的绝对地址 0~127
256	X	跳转到通用寄存器 X 保存的总线地址
257	Y	跳转到通用寄存器 Y 保存的总线地址
others	reserved	未定义，避免使用

18.1.15 LDM 指令

读取立即数地址。将 Addr 左移 2 比特作为总线地址，从该地址读取 32 位数据存入 Rd。该总线地址为 4 字节对齐，地址范围是 0x0~0x7FFFFFFC。

伪代码：`Rd = [Addr << 2]`

Rd 参数定义:

值	名称	描述
0	X	数据写入通用寄存器 X
1	Y	数据写入通用寄存器 Y

18.1.16 LDR 指令

读取寄存器偏移地址。以 Rn+Offset 为总线地址读取 32 位数据存入 Rd。Offset 为 16 位有符号数。总线地址必须为 4 字节对齐。

伪代码：`Rd = [Rn + Offset]`

Rn 参数定义:

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值	名称	描述
0	X	通用寄存器 X 保存的数据
1	Y	通用寄存器 Y 保存的数据

Rd 参数定义:

值	名称	描述
0	X	数据写入通用寄存器 X
1	Y	数据写入通用寄存器 Y
2	A	数据的低 16 位写入通用寄存器 A
3	B	数据的低 16 位写入通用寄存器 B
4	XL	数据的低 16 位写入通用寄存器 XL
5	XH	数据的低 16 位写入通用寄存器 XH
6	YL	数据的低 16 位写入通用寄存器 YL
7	YH	数据的低 16 位写入通用寄存器 YH

18.1.17 STM 指令

写入立即数地址。将 Addr 左移 2 比特作为总线地址，向该地址写入 Rn 的 32 位数据。该总线地址为 4 字节对齐，地址范围是 0x0~0x7FFFFFFC。

伪代码：`[Addr << 2] = Rn`

Rn 参数定义:

值	名称	描述
0	X	通用寄存器 X 保存的数据
1	Y	通用寄存器 Y 保存的数据

18.1.18 STR 指令

写入寄存器偏移地址。将 Rn 的 32 位数据写入总线地址 Rd+Offset。Offset 为 16 位有符号数。总线地址必须为 4 字节对齐。

伪代码：`[Rd + Offset] = Rn`

Rn 参数定义:

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值	名称	描述
0	X	通用寄存器 X 保存的数据
1	Y	通用寄存器 Y 保存的数据
2	A	通用寄存器 A 保存的数据，高 16 位补 0
3	B	通用寄存器 B 保存的数据，高 16 位补 0
4	XL	通用寄存器 XL 保存的数据，高 16 位补 0
5	XH	通用寄存器 XH 保存的数据，高 16 位补 0
6	YL	通用寄存器 YL 保存的数据，高 16 位补 0
7	YH	通用寄存器 YH 保存的数据，高 16 位补 0

Rd 参数定义:

值	名称	描述
0	X	通用寄存器 X 保存的数据
1	Y	通用寄存器 Y 保存的数据

18.1.19 CH 通道映射

PTM 共有 16 个输入输出通道，分别为 CH0~CH15。每个处理核都具有处理多达 16 路输入 IN0~IN15 和 16 路输出 OUT0~OUT15 的能力，都可以通过指令，以一定的映射关系对 PTM 的 16 个 CH 中的部分或全部进行输入和输出。

应注意的是,每个处理核的输入与输出都允许以不同的偏移映射到 CH0~CH15 上,也就是说处理核的输入 IN0~IN15 不等同于 CH0~CH15 的输入，输出 OUT0~OUT15 也不等同于 CH0~CH15 的输出。

输入偏移通过寄存器 ICRx_IBASE 指定，输出偏移通过寄存器 OCRx_OBASE 指定。具体的映射关系为：

$$输出: CH[(n+OCRx\_OBASE)\%16] = OUT[n]$$
$$输入: IN[n] = CH[(n+ICRx\_IBASE)\%16]$$

例如，如果 Core3 的 ICR3_IBASE=5, OCR3_OBASE=15, Core2 的 ICR2_IBASE=0，OCR2_OBASE=6，那么这两个核的 IO 通道映射如下表所示。

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PTM IO	CORE3 IN	CORE3 OUT	CORE2 IN	CORE2 OUT
CH0	IN11	OUT1	IN0	OUT10
CH1	IN12	OUT2	IN1	OUT11
CH2	IN13	OUT3	IN2	OUT12
CH3	IN14	OUT4	IN3	OUT13
CH4	IN15	OUT5	IN4	OUT14
CH5	IN0	OUT6	IN5	OUT15
CH6	IN1	OUT7	IN6	OUT0
CH7	IN2	OUT8	IN7	OUT1
CH8	IN3	OUT9	IN8	OUT2
CH9	IN4	OUT10	IN9	OUT3
CH10	IN5	OUT11	IN10	OUT4
CH11	IN6	OUT12	IN11	OUT5
CH12	IN7	OUT13	IN12	OUT6
CH13	IN8	OUT14	IN13	OUT7
CH14	IN9	OUT15	IN14	OUT8
CH15	IN10	OUT0	IN15	OUT9

SET，IO，JMP 与 WAIT 指令中涉及到的 IO 输入与输出，操作的是 IN0~IN15 和 OUT0~OUT15，都需经过偏移后指向 PTM 的各个 CH。

IO 通道映射的目的是，支持多个处理核使用相同的指令序列处理不同的 IO。例如，用户需要使用 PTM 实现 2 套独立的 SPI 接口，即让两个不同的处理核各自使用一套 IO 实现 SPI 通信功能。此时仅通过配置两个处理核的 IO 偏移，而不需要修改 PTM 指令即可达到这个目的。

对于一个处理核，输入和输出采用不同偏移的原因是，使用 IO 指令进行多路 IO 操作时，多路输入固定从最低比特 IN0 开始，多路输出固定从最低比特 OUT0 开始。所以如果需要输入与输出使用不同的 IO，就需要配置不同的输入和输出偏移，使得 IN0 与 OUT0 指向不同 IO。

18.1.20 CH 冲突

由于所有处理核都可以操作全部 16 个 CH，当多个核在同一个 CH 上同时输出时会产生冲突。对于每个 PTM CH，其输出使能基于如下原则确定：

1. 任何一个处理核通过 SET 指令将当前 CH 的输出使能 (OE) 翻转时，OE 取反，即原本输出使能开启的变为关闭，原本关闭的变为开启；
2. 如果条件 1 不满足，且 CPU 将寄存器 DOECR 对应 bit 置 1 时，输出使能关闭；
3. 如果条件 1 和 2 都不满足，且任何一个处理核通过 SET 指令或 IO 指令在当前 CH 上输出，或 CPU 将寄存器 DOESR 对应 bit 置 1 时，输出使能开启。

对于每个 PTM CH，其输出值基于如下原则确定：

1. 任何一个处理核通过 IO 指令将当前 CH 的输出值翻转时，原本输出高的变为输出低，原本输出低的变为输出高；

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2. 如果条件 1 不满足，且任何一个处理核通过 SET 指令或 IO 指令在当前 CH 上输出低，或 CPU 将寄存器 DOCR 对应 bit 置 1 时，输出低；
3. 如果条件 1 和 2 都不满足，且任何一个处理核通过 SET 指令或 IO 指令在当前 CH 上输出高，或 CPU 将寄存器 DOSR 对应 bit 置 1 时，输出高。

18.1.21 IO 指令

输入输出并延时。

IO 指令是 PTM 用于操控 IO 的最主要指令，功能较为复杂。简单而言，IO 指令能够将 OFIFO 或 X 中的数据按比特依次输出给多个 IO，或将多个 IO 的输入按比特依次存入 Y 或 IFIFO，同时改变任意两个 IO 的输出并延时 Dly 个周期。

Dir=0 时，IO 指令可用于多路 IO 输出，具体行为如下：

- 如果 OCRx_ORSH=1，将通用寄存器 X 中的最低 Cnt 个比特推送至 OUT 端口的低位，并将 X 右移 Cnt 位，即 OUT[Cnt-1:0]=X[Cnt-1:0]; X=X>>Cnt。
- 如果 OCRx_ORSH=0，将通用寄存器 X 中的最高 Cnt 个比特次序翻转后推送至 OUT 端口的低位，并将 X 左移 Cnt 位，即 OUT[Cnt-1:0]=X[31-Cnt+1:31]; X=X<<Cnt。
- 每次推送后，输出比特计数会累加，当计数达到输出阈值 (OCRx_OLIMIT)，且 OFIFO 自动获取开启 (OCRx_OAUTO=1) 时，X 可自动从 OFIFO 中取出 1 个新的 32bit 数据。取出新的数据时，输出比特计数会清零。
- 从 OFIFO 取出的数据可以经过额外移位后再存入 X。移位方向与 X 的移位方向相同，移位位数等于 OCRx_OSHIFT。
- 假如输出比特计数已达到输出阈值，X 需要自动取数，但是 OFIFO 为空，若 OCRx_OBLOCK=1，流水线会暂停以等待 OFIFO 被 CPU 或 DMA 填入数据，否则不暂停流水线，直接将 0 赋值给 X。

Dir=1 时，IO 指令可用于多路 IO 输入，具体行为如下：

- 如果 ICRx_IRSH=0，将 Y 左移 Cnt 位，并从 IN 端口的低位获取 Cnt 个比特，存入通用寄存器 Y 的最低 Cnt 个比特，即 Y=Y<<Cnt; Y[Cnt-1:0]=IN[Cnt-1:0]。
- 如果 ICRx_IRSH=1，将 Y 右移 Cnt 位，并从 IN 端口的低位获取 Cnt 个比特，次序翻转后存入通用寄存器 Y 的最高 Cnt 个比特，即 Y=Y>>Cnt; Y[31:31-Cnt+1] = IN[Cnt-1:0]。
- 每次获取输入后，输入比特计数会累加，当计数达到输入阈值 (ICRx_ILIMIT)，且 IFIFO 自动存入开启 (ICRx_IAUTO=1) 时，Y 可自动向 IFIFO 中存入 32bit 数据。存入新的数据时，输入比特计数会清零。
- Y 中的数据可以经过额外移位后再存入 IFIFO。移位方向与 Y 的移位方向相同，移位位数等于 ICRx_ISHIFT。
- 假如输入比特计数已达到输入阈值，Y 需要将数据存入 IFIFO，但是 IFIFO 已满，若 ICRx_IBLOCK=1，流水线会暂停以等待 IFIFO 数据被 CPU 或 DMA 取出，否则不暂停流水线，直接将当前 Y 的数据丢弃。

在多路 IO 输出或输入的同时，IO 指令可以额外改变最多两路 IO 的输出。两个 IO 由 On 和 Om 选择，输出由 Vn 和 Vm 确定。

Vn 和 Vm 参数定义:

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值	名称	描述
0	NOP	不改变输出状态
1	R	输出取反
2	L	输出低
3	H	输出高

18.1.22 FIFO 管理

每个处理核均内置输出与输入 FIFO，数据位宽 32bit，深度可配置如下：

ICRx.IFIFO	OCRx.OFIFO	IFIFOx 深度	OFIFOx 深度
0	0	0	0
0	1	0	8
0	8	0	1
1	1	4	4

OFIFO 用于向 IO 输出，数据由 CPU 或 DMA 通过寄存器 OFIFOx 写入，可通过 SET 指令取出，或自动取出到通用寄存器 X。

OFIFO 的状态可通过 OCRx.OFULL 和 OCRx.OEMPTY 查询。

处理核使能后，如果 OFIFO 未满，会自动产生 DMA 请求以从 DMA 获取数据。

如果 OFIFO 自动获取开启 (OCRx_OAUTO=1)，只要 X 从未被赋值，或输出比特计数已达到输出阈值，处理核会尽早取出 OFIFO 数据填入 X，而非依赖于 IO 指令。也就是说，从 OFIFO 取数的操作由处理核择机自动完成，用户只需要向 OFIFO 填入数据，并在预期时刻使用 IO 指令将 X 中的数据推送至 IO 输出即可。

当 OCRx.OBLOCK 为 1 时，流水线会在如下情况暂停：

- 执行 SET 指令，从 OFIFO 取数但 OFIFO 为空时；
- 执行 IO 指令进行多路 IO 输出，但 X 从未被赋值或输出比特计数已达到输出阈值 (即 X 未能及时从 OFIFO 取出数据) 时。

如果 OCRx.OBLOCK 为 0，上述情况下流水线不会暂停，但本应从 OFIFO 取出的数据会由数据 0 代替，此时 OFIFO 下溢出标志 (OCRx.OUF) 会置位。

IFIFO 用于从 IO 输入，数据可通过 SET 指令写入，或自动从通用寄存器 Y 写入，由 CPU 或 DMA 通过寄存器 IFIFOx 读出。

IFIFO 的状态可通过 ICRx.IFULL 和 ICRx.IEMPTY 查询。

处理核使能后，如果 IFIFO 非空，会自动产生将数据读走的 DMA 请求。

如果 IFIFO 自动存入开启 (ICRx_IAUTO=1)，只要输入比特计数已达到输入阈值，处理核会尽快将 Y 中的数据存入 IFIFO，而非依赖于 IO 指令。也就是说，Y 向 IFIFO 存数的操作由处理核择机自动完成，用户只需要在预期时刻使用 IO 指令将 IO 输入值填入 Y，并及时从 IFIFO 取走数据即可。

当 ICRx.IBLOCK 为 1 时，流水线会在如下情况暂停：

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- 执行 SET 指令，向 IFIFO 存数但 IFIFO 已满；
- 执行 IO 指令进行多路 IO 输入，但输入比特计数已达到输入阈值 (即 Y 的数据未能及时存入 IFIFO) 时。

如果 ICRx.IBLOCK 为 0，上述情况下流水线不会暂停，但本应存入 IFIFO 的数据会被丢弃，此时 IFIFO 溢出标志 (ICRx.IOF) 会置位。

18.1.23 事件通知

PTM 内置 16 个事件通知标志 EVT0~EVT15。SET 指令可以对其中部分或全部 EVT 置 1 或清 0。WAIT 和 JMP 可使用 EVT 进行判断。不同处理核可以基于 EVT 同步状态，实现多核互动。EVT 状态可以通过寄存器 ISR.EVTx 读出，也可以写 1 清 0，但不能置 1。

当 IER.EVTAUTOx 为 1 时，第 x 个处理核的任务运行结束时会自动将 EVTx 置为 1。可自动置位的事件仅限 EVT0 EVT7。

当 IER.EVTIEx 为 1 时，EVTx 为 1 时会产生 CPU 中断。可产生中断的事件仅限 EVT0 EVT7。

18.1.24 错误通知

处理核运行过程中，可能发生如下错误：

- 总线错误。通过 JMP 指令跳转或顺序执行指令时，总线地址是非法地址，或访存指令访问的总线地址是非法地址，都会产生总线错误。总线错误发生时，对应处理核的 ISR.ERRx 会置 1，如果 IER.ERRIEx 为 1 则会产生 CPU 中断。
- 指令错误。当前执行指令为非法指令时，会发生指令错误，对应处理核的 ISR.ERRx 会置 1，如果 IER.ERRIEx 为 1 则会产生 CPU 中断。
- TCM 冲突。如果处理核的指令超过 16 条，而需禁用的其它处理核仍被使能，会产生 TCM 冲突，对应处理核的 ISR.TCMx 会置 1，如果 IER.ERRIEx 为 1 则会产生 CPU 中断。

发生上述任何一种错误时，该处理核运行中止。可以通过 PCx 查询当前的指令地址。

18.1.25 调试手段

处理核启动以后，可以通过向 CER.STEPx 写 1 请求暂停运行，并读取 CER_ENx 的值判断处理核是否已经停止运行。处理核当前的指令地址可通过 PCx 查询。所有通用寄存器都可以通过寄存器接口获取实时值，并可改写。处理核暂停时，向 CER.STEPx 写 1 可以单步执行一条指令。需要注意如果单步执行的指令会使流水线暂停，单步执行可能一直卡住无法结束，即 CER_ENx 一直为 1，此时需要将引发流水线暂停的条件消除才能完成执行。

18.1.26 指令结束的判定标准

每个处理核可以设置两个指令结束地址，分别为 CCRx.END0 和 CCRx.END1，这是为了使不同分支的指令可以分别结束。每个核必须设定至少一个非 0 的指令结束地址，否则可能永久循环执行，并侵入其它核的指令空间。

当核的执行地址不为 0，且等于指令结束地址中的任何一个时，该条指令执行完成后会结束核的运行 (CCRx.REP=0 时)，或者从 0 地址重新开始执行 (CCRx.REP>0 时)。

如果在指令结束地址执行的是 WAIT 指令，执行完成的判定条件是 Src 等于 Pol，不包含随后的延时 Dly。当 Src 等于 Pol 的条件成立时，如果当前 CCRx.REP=0，处理核的执行会立即结束，而不等待 Dly 延时；如果当前

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CCRx.REP>0，处理核会将 CCRx.REP 减 1，跳转到 0 地址，等待 Dly 延时，再开始执行。

如果在指令结束地址执行的是 JMP 指令，执行立即完成，原有跳转功能失效。如果当前 CCRx.REP=0，处理核的执行会立即结束；如果当前 CCRx.REP>0，处理核会将 CCRx.REP 减 1，并跳转到 0 地址执行。不论是哪种方式，都与 JMP 指令的原有功能不相符，因此应当避免在指令结束地址执行 JMP 指令。

18.1.27 事件触发

WAIT 指令可等待芯片内各模块产生的事件触发信号。TRIG0~TRIG127 的定义如下表。

ptm1_trig	7	6	5	4	3	2	1	0	
127	PTM1_EVT7	PTM1_EVT6	PTM1_EVT5	PTM1_EVT4	PTM1_EVT3	PTM1_EVT2	PTM1_EVT1	PTM1_EVT0	120
119	I2S2_OF	I2S2_UF	I2S1_OF	I2S1_UF	AES_DONE	TRNG_RANDGEN	TRNG_SEEDGEN	HCPU_SLEEPDEEP	112
111	EPIC_LINEHIT	EPIC_DONE	JPEGD_INT	LCDC1_ERR	LCDC1_LINE	LCDC1_LINEHIT	LCDC1_FMARK	LCDC1_DONE	104
103	LCDC1_BUSY	TSEN_DONE	EZIP1_ROW	EZIP1_DONE	USART3_TXBYTE	USART3_RXBYTE	USB_RX	USB_TX	96
95	I2C4_RXFULL	I2C4_TXEMPTY	I2C4_DMADONE	I2C4_ATDONE	USART2_TXBYTE	USART2_RXBYTE	USART1_TXBYTE	USART1_RXBYTE	88
87	SDMMC2_DATDONE	SDMMC2_CMDDONE	SDMMC1_DATDONE	SDMMC1_CMDDONE	SPI2_START	SPI2_DONE	SPI1_START	SPI1_DONE	80
79	I2C3_RXFULL	I2C3_TXEMPTY	I2C3_DMADONE	I2C3_ATDONE	I2C2_RXFULL	I2C2_TXEMPTY	I2C2_DMADONE	I2C2_ATDONE	72
71	I2C1_RXFULL	I2C1_TXEMPTY	I2C1_DMADONE	I2C1_ATDONE	WLAN_ACTIVE	BT_COLLISION	BT_PRIORITY	BT_ACTIVE	64
63	ATIM2_CH1	ATIM2_TRIG	ATIM2_UPDATE	PWM1_UPDATE5	PWM1_UPDATE4	PWM1_UPDATE3	PWM1_UPDATE2	PWM1_UPDATE1	56
55	MAILBOX1_C4IRQ7	MAILBOX1_C3IRQ7	MAILBOX1_C2IRQ7	MAILBOX1_C1IRQ7	BT_TX_EN	BT_RX_EN	DCMI_FRAMESYNC	DCMI_VSYNC	48
47	DMAC1_LDONE8	DMAC1_LDONE7	DMAC1_LDONE6	DMAC1_LDONE5	DMAC1_LDONE4	DMAC1_LDONE3	DMAC1_LDONE2	DMAC1_LDONE1	40
39	DMAC1_HALF8	DMAC1_HALF7	DMAC1_HALF6	DMAC1_HALF5	DMAC1_HALF4	DMAC1_HALF3	DMAC1_HALF2	DMAC1_HALF1	32
31	DMAC1_DONE8	DMAC1_DONE7	DMAC1_DONE6	DMAC1_DONE5	DMAC1_DONE4	DMAC1_DONE3	DMAC1_DONE2	DMAC1_DONE1	24
23	CAN1_BUSY	ATIM1_COM	ATIM1_CH4	ATIM1_CH3	ATIM1_CH2	ATIM1_CH1	ATIM1_TRIG	ATIM1_UPDATE	16
15	BTIM2_UPDATE	BTIM1_UPDATE	0	0	GPTIM2_CH2	GPTIM2_CH1	GPTIM2_TRIG	GPTIM2_UPDATE	8
7	GPTIM1_CH4	GPTIM1_CH3	GPTIM1_CH2	GPTIM1_CH1	GPTIM1_TRIG	GPTIM1_UPDATE	HCPU_SLEEPING	0	0

18.1.28 PTM 寄存器

PTM 的基地址是 0x500A1000。

表 18-1: PTM 寄存器映射表

Offset	Attribute	Reset Value	Register Name	Register Description
0x00			**ISR**	interrupt status register
[31:28]			RSVD	
[27]	r	1'h0	TCM3	TCM collision flag of core 3, will be cleared by CER_RST3
[26]	r	1'h0	TCM2	TCM collision flag of core 2, will be cleared by CER_RST2
[25]	r	1'h0	TCM1	TCM collision flag of core 1, will be cleared by CER_RST1
[24]	r	1'h0	TCM0	TCM collision flag of core 0, will be cleared by CER_RST0
[23:20]			RSVD	
[19]	r	1'h0	ERR3	bus error or illegal instruction flag of core 3, will be cleared by CER_RST3
[18]	r	1'h0	ERR2	bus error or illegal instruction flag of core 2, will be cleared by CER_RST2
[17]	r	1'h0	ERR1	bus error or illegal instruction flag of core 1, will be cleared by CER_RST1
[16]	r	1'h0	ERR0	bus error or illegal instruction flag of core 0, will be cleared by CER_RST0
[15]	rw	1'h0	EVT15	event flag 15, set by instruction. Write 1 clear. Write 0 no effect.
[14]	rw	1'h0	EVT14	event flag 14, set by instruction. Write 1 clear. Write 0 no effect.
[13]	rw	1'h0	EVT13	event flag 13, set by instruction. Write 1 clear. Write 0 no effect.
[12]	rw	1'h0	EVT12	event flag 12, set by instruction. Write 1 clear. Write 0 no effect.
[11]	rw	1'h0	EVT11	event flag 11, set by instruction. Write 1 clear. Write 0 no effect.
[10]	rw	1'h0	EVT10	event flag 10, set by instruction. Write 1 clear. Write 0 no effect.
[9]	rw	1'h0	EVT9	event flag 9, set by instruction. Write 1 clear. Write 0 no effect.
[8]	rw	1'h0	EVT8	event flag 8, set by instruction. Write 1 clear. Write 0 no effect.
[7]	rw	1'h0	EVT7	event flag 7, set by instruction. Write 1 clear. Write 0 no effect.
[6]	rw	1'h0	EVT6	event flag 6, set by instruction. Write 1 clear. Write 0 no effect.

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表 18-1: PTM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[5]	rw	1'h0	EVT5	event flag 5, set by instruction. Write 1 clear. Write 0 no effect.
[4]	rw	1'h0	EVT4	event flag 4, set by instruction. Write 1 clear. Write 0 no effect.
[3]	rw	1'h0	EVT3	event flag 3, set by instruction. Write 1 clear. Write 0 no effect. Set when core 3 execution done and IER_EVTAUTO3 is 1.
[2]	rw	1'h0	EVT2	event flag 2, set by instruction. Write 1 clear. Write 0 no effect. Set when core 2 execution done and IER_EVTAUTO2 is 1.
[1]	rw	1'h0	EVT1	event flag 1, set by instruction. Write 1 clear. Write 0 no effect. Set when core 1 execution done and IER_EVTAUTO1 is 1.
[0]	rw	1'h0	EVT0	event flag 0, set by instruction. Write 1 clear. Write 0 no effect. Set when core 0 execution done and IER_EVTAUTO0 is 1.
0x04			**IER**	interrupt enable register
[31:20]			RSVD	
[19]	rw	1'h0	ERRIE3	enable error interrupt of core 3
[18]	rw	1'h0	ERRIE2	enable error interrupt of core 2
[17]	rw	1'h0	ERRIE1	enable error interrupt of core 1
[16]	rw	1'h0	ERRIE0	enable error interrupt of core 0, including bus error, illegal instruction and tcm collision
[15:12]			RSVD	
[11]	rw	1'h0	EVTAUTO3	enable auto event 3
[10]	rw	1'h0	EVTAUTO2	enable auto event 2
[9]	rw	1'h0	EVTAUTO1	enable auto event 1
[8]	rw	1'h0	EVTAUTO0	enable auto event 0 1: event 0 will assert automatically when core 0 execution done (repetition done). 0: no auto event 0
[7:4]			RSVD	
[3]	rw	1'h0	EVTIE3	enable event 3 interrupt
[2]	rw	1'h0	EVTIE2	enable event 2 interrupt
[1]	rw	1'h0	EVTIE1	enable event 1 interrupt
[0]	rw	1'h0	EVTIE0	enable event 0 interrupt 1: event 0 interrupt enabled 0: event 0 interrupt disabled
0x08			**CER**	Core Enable Register
[31:28]			RSVD	
[27]	w1s	1'h0	STEP3	core 3 single step
[26]	w1s	1'h0	STEP2	core 2 single step
[25]	w1s	1'h0	STEP1	core 1 single step
[24]	w1s	1'h0	STEP0	core 0 single step write 1 to step. Core will execute the next instruction, then stop automatically. write 0 has no effect
[23:20]			RSVD	
[19]	w1s	1'h0	RST3	reset core 3
[18]	w1s	1'h0	RST2	reset core 2
[17]	w1s	1'h0	RST1	reset core 1
[16]	w1s	1'h0	RST0	write 1 to reset core 0. Will reset all status and registers including X/Y/A/B/PC/FIFO. TCM code will not be affected. write 0 has no effect
[15:12]			RSVD	
[11]	w1s	1'h0	STOP3	stop core 3

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表 18-1: PTM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[10]	w1s	1'h0	STOP2	stop core 2
[9]	w1s	1'h0	STOP1	stop core 1
[8]	w1s	1'h0	STOP0	write 1 to stop core 0 write 0 has no effect
[7:4]			RSVD	
[3]	rw	1'h0	EN3	enable core 3
[2]	rw	1'h0	EN2	enable core 2
[1]	rw	1'h0	EN1	enable core 1
[0]	rw	1'h0	EN0	write 1 to enable core 0 write 0 has no effect read 1 indicates core is working read 0 indicates core is not working
0x10			**DOER**	Data Output Enable Register
[31:16]			RSVD	
[15:0]	r	16'h0	DOE	Read as output enable of PTM_CH. Bit n is for PTM_CH[n]. Should be modified by instruction or by setting DOESR/DOECR registers.
0x14			**DOR**	Data Output Register
[31:16]			RSVD	
[15:0]	r	16'h0	DO	Read as output value of PTM_CH. Bit n is for PTM_CH[n]. Should be modified by instruction or by setting DOSR/DOCR registers.
0x18			**DOESR**	Data Output Enable Set Register
[31:16]			RSVD	
[15:0]	w	16'h0	DOES	Write 1 to bit n: set output enable of PTM_CH[n] to 1. Write 0 to bit n: no effect.
0x1C			**DOECR**	Data Output Enable Clear Register
[31:16]			RSVD	
[15:0]	w	16'h0	DOEC	Write 1 to bit n: set output enable of PTM_CH[n] to 0. Write 0 to bit n: no effect.
0x20			**DOSR**	Data Output Set Register
[31:16]			RSVD	
[15:0]	w	16'h0	DOS	Write 1 to bit n: set output value of PTM_CH[n] to 1. Write 0 to bit n: no effect.
0x24			**DOCR**	Data Output Clear Register
[31:16]			RSVD	
[15:0]	w	16'h0	DOC	Write 1 to bit n: set output value of PTM_CH[n] to 0. Write 0 to bit n: no effect.
0x30			**CCR0**	Core 0 control register
[31:24]	rw	8'h0	END1	Another TCM instruction index to end instruction sequence. After executes this instruction, current core will stop execution if REP=0, or restart from index 0 if REP!=0
[23:16]	rw	8'h0	END0	TCM instruction index to end instruction sequence. After executes this instruction, current core will stop execution if REP=0, or restart from index 0 if REP!=0

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表 18-1: PTM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[15:8]	rw	8'h0	REP	Repetition times for instruction sequence. 0: No repetition. Core will stop after executes TCM instruction of index END0 or END1. 1~254: Finite Repetition. Core will restart from index 0 after executes TCM instruction of index END0 or END1, and REP will be decreased by 1, until REP become 0. 255: Infinite Repetion. Core will restart from index 0 after executes TCM instruction of index END0 or END1, and REP will not be decreased.
[7:0]	rw	8'h0	PSC	Prescaler factor. Core will execute at a divided rate of hclk/(PSC+1). All instructions will be affected.
0x34			**ICR0**	Input control register for core 0
[31]	r	1'h0	IFULL	1: IFIFO is full 0: IFIFO is not full
[30]	r	1'h1	IEMPTY	1: IFIFO is empty 0: IFIFO is not empty
[29]	r	1'h0	IOF	1: IFIFO overflow occurs, when new data is to be pushed into IFIFO but IFIFO is already full, thus the new data is discarded 0: IFIFO never overflow
[28:24]	rw	5'h0	ILIMIT	Input threshold for IFIFO auto push, valid when IAUTO=1. 0: Input threshold is 32 others: Input threshold is ILIMIT If accumulated input bit counter(named as Y_CNT) reaches or exceeds input threshold, input data stored in Y register will be pushed into IFIFO automatically, and accumulated input bit counter is cleared to 0.
[23:21]			RSVD	
[20:16]	rw	5'h0	ISHIFT	Shift bit count of Y register when Y is automatically pushed into IFIFO, valid when IAUTO=1. Data pushed into IFIFO is Y left shifted by ISHIFT if IRSH=0, or Y right shifted by ISHIFT if IRSH=1. Only valid for automatic IFIFO push of PTM_IO instruction. When pushing IFIFO by PTM_SET instruction, shift processing should be coded in the OP and IMM16 field of the instruction instead of ISHIFT.
[15:12]			RSVD	
[11:8]	rw	4'h0	IBASE	Input offset for this core. CORE_IN[n] = PTM_CH[(n+IBASE) round 16] For example, if IBASE=5, CORE_IN[0] = PTM_CH[5], CORE_IN[11] = PTM_CH[0], CORE_IN[15] = PTM_CH[4]
[7:4]			RSVD	
[3]	rw	1'h0	IBLOCK	1: Core execution is blocked if a new data is to be pushed into IFIFO but IFIFO is already full. Related instruction are PTM_IO and PTM_SET. Core execution will continue if the data can be successfully pushed into IFIFO after IFIFO been fetched by CPU or DMA. 0: Core execution will not be blocked, so IFIFO may overflow. New data will be discarded.

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表 18-1: PTM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[2]	rw	1'h0	IRSH	1: for PTM_IO instruction, Y register will be right shifted, and CORE_IN signals will be placed from MSB of Y register. For example, if PTM_IO input 8-bit signal, Y will be right shifted by 8, and CORE_IN[0]->Y[31], CORE_IN[1]->Y[30] ..... CORE_IN[7]->Y[24]. When Y is automatically pushed into IFIFO, pushed data will be additionally right shifted by ISHIFT. This is useful when input sequence is LSB first but data need to be stored in lower bits of a word. 0: for PTM_IO instruction, Y register will be left shifted, and CORE_IN data will be placed from LSB of Y register. For example, if PTM_IO input 8-bit signal, Y will be left shifted by 8, and CORE_IN[0]->Y[0], CORE_IN[1]->Y[1] ..... CORE_IN[7]->Y[7]. When Y is automatically pushed into IFIFO, pushed data will be additionally left shifted by ISHIFT. This is useful when input sequence is MSB first but data need to be stored in higher bits of a word.
[1]	rw	1'h0	IAUTO	1: If accumulated input bit counter reaches or exceeds input threshold, input data stored in Y register will be pushed into IFIFO automatically, and accumulated input bit counter is cleared to 0. 0: Y register will not be pushed into IFIFO automatically. PTM_SET instruction can push IFIFO instead.
[0]	rw	1'h0	IFIFO	1: IFIFO enabled. IFIFO depth will be 4 if OFIFO also enabled, and be 8 if OFIFO disabled. 0: IFIFO disabled.
0x38			**OCR0**	Output control register for core 0
[31]	r	1'h0	OFULL	1: OFIFO is full 0: OFIFO is not full
[30]	r	1'h1	OEMPTY	1: OFIFO is empty 0: OFIFO is not empty
[29]	r	1'h0	OUF	1: OFIFO underflow occurs, which means new data is to be poped from OFIFO but OFIFO is empty, thus the poped data is 0 0: OFIFO never underflow
[28:24]	rw	5'h0	OLIMIT	Output bit counter for OFIFO auto pop, valid when OAUTO=1. 0: Output bit counter is 32 others: Output bit counter is OLIMIT If left output bit counter(named as X_CNT) reaches 0, OFIFO will be poped to X register automatically, and left output bit counter is reset to OLIMIT.
[23:21]			RSVD	
[20:16]	rw	5'h0	OSHIFT	Shift bit count of OFIFO data when OFIFO is automatically poped into X register, valid when OAUTO=1. Data poped from OFIFO is left shifted by OSHIFT if ORSH=0, or right shifted by OSHIFT if ORSH=1, before storing into X register. Only valid for automatic OFIFO pop of PTM_IO instruction. When poping OFIFO by PTM_SET instruction, shift processing should be coded in the OP and IMM16 field of the instruction instead of OSHIFT.
[15:12]			RSVD	
[11:8]	rw	4'h0	OBASE	Output offset for this core. PTM_CH[(n+IBASE) round 16] = CORE_OUT[n] For example, if OBASE=5, PTM_CH[5] = CORE_OUT[0], PTM_CH[0] = CORE_OUT[11], PTM_CH[4] = CORE_OUT[15]
[7:4]			RSVD	

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表 18-1: PTM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[3]	rw	1'h0	OBLOCK	1: Core execution is blocked if a new data is to be poped from OFIFO but OFIFO is empty. Related instruction are PTM_IO and PTM_SET. Core execution will continue if data can be successfully poped from OFIFO after OFIFO been filled by CPU or DMA. 0: Core execution will not be blocked, so OFIFO may underflow. Poped data will be 0.
[2]	rw	1'h0	ORSH	1: for PTM_IO instruction, CORE_OUT signals will be pushed from LSB of X register, and X register will be right shifted. For example, if PTM_IO output 8-bit signal, X[0] ->CORE_OUT[0], X[1] ->CORE_OUT[1] ..... X[7] ->CORE_OUT[7], and X will be right shifted by 8. When OFIFO is automatically poped, poped data will be right shifted by OSHIFT before set to X. This is useful when output sequence is LSB first but data need to be stored in higher bits of a word. 0: for PTM_IO instruction, CORE_OUT signals will be pushed from MSB of X register, and X register will be left shifted. For example, if PTM_IO output 8-bit signal, X[31] ->CORE_OUT[0], X[30] ->CORE_OUT[1] ..... X[24] ->CORE_OUT[7], and X will be left shifted by 8. When OFIFO is automatically poped, poped data will be left shifted by OSHIFT before set to X. This is useful when output sequence is MSB first but data need to be stored in lower bits of a word.
[1]	rw	1'h0	OAUTO	1: If left output bit counter reaches 0, OFIFO will be poped to X register automatically, and left output bit counter is reset to OLIMIT. 0: OFIFO will not be poped to X register automatically. PTM_SET instruction can pop OFIFO instead.
[0]	rw	1'h0	OFIFO	1: OFIFO enabled. OFIFO depth will be 4 if IFIFO also enabled, and be 8 if IFIFO disabled. 0: OFIFO disabled.
0x3C			**X0**	X register for core 0
[31:0]	rw	32'h0	VAL	Instant value of X register. Bit 31 to 16 is XH register. Bit 15 to 0 is XL register.
0x40			**Y0**	Y register for core 0
[31:0]	rw	32'h0	VAL	Instant value of Y register. Bit 31 to 16 is YH register. Bit 15 to 0 is YL register.
0x44			**A0**	A register for core 0
[31:16]			RSVD	
[15:0]	rw	16'h0	VAL	Instant value of A register.
0x48			**B0**	B register for core 0
[31:16]			RSVD	
[15:0]	rw	16'h0	VAL	Instant value of B register.
0x4C			**PC0**	PC register for core 0
[31:0]	r	32'h0	VAL	Instant value of PC(program counter).
0x50			**IFIFO0**	IFIFO entry for core 0
[31:0]	r	32'h0	DAT	Read this entry to pop IFIFO. Return 0 if IFIFO empty.
0x54			**OFIFO0**	OFIFO entry for core 0
[31:0]	w	32'h0	DAT	Write this entry to push OFIFO.
0x60			**CCR1**	Core 1 control register

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表 18-1: PTM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:24]	rw	8'h0	END1	Another TCM instruction index to end instruction sequence. After executes this instruction, current core will stop execution if REP=0, or restart from index 0 if REP!=0
[23:16]	rw	8'h0	END0	TCM instruction index to end instruction sequence. After executes this instruction, current core will stop execution if REP=0, or restart from index 0 if REP!=0
[15:8]	rw	8'h0	REP	Repetition times for instruction sequence. 0: No repetition. Core will stop after executes TCM instruction of index END0 or END1. 1~254: Finite Repetition. Core will restart from index 0 after executes TCM instruction of index END0 or END1, and REP will be decreased by 1, until REP become 0. 255: Infinite Repetion. Core will restart from index 0 after executes TCM instruction of index END0 or END1, and REP will not be decreased.
[7:0]	rw	8'h0	PSC	Prescaler factor. Core will execute at a divided rate of hclk/(PSC+1). All instructions will be affected.
0x64			**ICR1**	Input control register for core 1
[31]	r	1'h0	IFULL	1: IFIFO is full 0: IFIFO is not full
[30]	r	1'h1	IEMPTY	1: IFIFO is empty 0: IFIFO is not empty
[29]	r	1'h0	IOF	1: IFIFO overflow occurs, when new data is to be pushed into IFIFO but IFIFO is already full, thus the new data is discarded 0: IFIFO never overflow
[28:24]	rw	5'h0	ILIMIT	Input threshold for IFIFO auto push, valid when IAUTO=1. 0: Input threshold is 32 others: Input threshold is ILIMIT If accumulated input bit counter(named as Y_CNT) reaches or exceeds input threshold, input data stored in Y register will be pushed into IFIFO automatically, and accumulated input bit counter is cleared to 0.
[23:21]			RSVD	
[20:16]	rw	5'h0	ISHIFT	Shift bit count of Y register when Y is automatically pushed into IFIFO, valid when IAUTO=1. Data pushed into IFIFO is Y left shifted by ISHIFT if IRSH=0, or Y right shifted by ISHIFT if IRSH=1. Only valid for automatic IFIFO push of PTM_IO instruction. When pushing IFIFO by PTM_SET instruction, shift processing should be coded in the OP and IMM16 field of the instruction instead of ISHIFT.
[15:12]			RSVD	
[11:8]	rw	4'h0	IBASE	Input offset for this core. CORE_IN[n] = PTM_CH[(n+IBASE) round 16] For example, if IBASE=5, CORE_IN[0] = PTM_CH[5], CORE_IN[11] = PTM_CH[0], CORE_IN[15] = PTM_CH[4]
[7:4]			RSVD	
[3]	rw	1'h0	IBLOCK	1: Core execution is blocked if a new data is to be pushed into IFIFO but IFIFO is already full. Related instruction are PTM_IO and PTM_SET. Core execution will continue if the data can be successfully pushed into IFIFO after IFIFO been fetched by CPU or DMA. 0: Core execution will not be blocked, so IFIFO may overflow. New data will be discarded.

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表 18-1: PTM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[2]	rw	1'h0	IRSH	1: for PTM_IO instruction, Y register will be right shifted, and CORE_IN signals will be placed from MSB of Y register. For example, if PTM_IO input 8-bit signal, Y will be right shifted by 8, and CORE_IN[0]->Y[31], CORE_IN[1]->Y[30] ..... CORE_IN[7]->Y[24]. When Y is automatically pushed into IFIFO, pushed data will be additionally right shifted by ISHIFT. This is useful when input sequence is LSB first but data need to be stored in lower bits of a word. 0: for PTM_IO instruction, Y register will be left shifted, and CORE_IN data will be placed from LSB of Y register. For example, if PTM_IO input 8-bit signal, Y will be left shifted by 8, and CORE_IN[0]->Y[0], CORE_IN[1]->Y[1] ..... CORE_IN[7]->Y[7]. When Y is automatically pushed into IFIFO, pushed data will be additionally left shifted by ISHIFT. This is useful when input sequence is MSB first but data need to be stored in higher bits of a word.
[1]	rw	1'h0	IAUTO	1: If accumulated input bit counter reaches or exceeds input threshold, input data stored in Y register will be pushed into IFIFO automatically, and accumulated input bit counter is cleared to 0. 0: Y register will not be pushed into IFIFO automatically. PTM_SET instruction can push IFIFO instead.
[0]	rw	1'h0	IFIFO	1: IFIFO enabled. IFIFO depth will be 4 if OFIFO also enabled, and be 8 if OFIFO disabled. 0: IFIFO disabled.
0x68			**OCR1**	Output control register for core 1
[31]	r	1'h0	OFULL	1: OFIFO is full 0: OFIFO is not full
[30]	r	1'h1	OEMPTY	1: OFIFO is empty 0: OFIFO is not empty
[29]	r	1'h0	OUF	1: OFIFO underflow occurs, which means new data is to be poped from OFIFO but OFIFO is empty, thus the poped data is 0 0: OFIFO never underflow
[28:24]	rw	5'h0	OLIMIT	Output bit counter for OFIFO auto pop, valid when OAUTO=1. 0: Output bit counter is 32 others: Output bit counter is OLIMIT If left output bit counter(named as X_CNT) reaches 0, OFIFO will be poped to X register automatically, and left output bit counter is reset to OLIMIT.
[23:21]			RSVD	
[20:16]	rw	5'h0	OSHIFT	Shift bit count of OFIFO data when OFIFO is automatically poped into X register, valid when OAUTO=1. Data poped from OFIFO is left shifted by OSHIFT if ORSH=0, or right shifted by OSHIFT if ORSH=1, before storing into X register. Only valid for automatic OFIFO pop of PTM_IO instruction. When poping OFIFO by PTM_SET instruction, shift processing should be coded in the OP and IMM16 field of the instruction instead of OSHIFT.
[15:12]			RSVD	
[11:8]	rw	4'h0	OBASE	Output offset for this core. PTM_CH[(n+IBASE) round 16] = CORE_OUT[n] For example, if OBASE=5, PTM_CH[5] = CORE_OUT[0], PTM_CH[0] = CORE_OUT[11], PTM_CH[4] = CORE_OUT[15]
[7:4]			RSVD	

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表 18-1: PTM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[3]	rw	1'h0	OBLOCK	1: Core execution is blocked if a new data is to be poped from OFIFO but OFIFO is empty. Related instruction are PTM_IO and PTM_SET. Core execution will continue if data can be successfully poped from OFIFO after OFIFO been filled by CPU or DMA. 0: Core execution will not be blocked, so OFIFO may underflow. Poped data will be 0.
[2]	rw	1'h0	ORSH	1: for PTM_IO instruction, CORE_OUT signals will be pushed from LSB of X register, and X register will be right shifted. For example, if PTM_IO output 8-bit signal, X[0] ->CORE_OUT[0], X[1] ->CORE_OUT[1] ..... X[7] ->CORE_OUT[7], and X will be right shifted by 8. When OFIFO is automatically poped, poped data will be right shifted by OSHIFT before set to X. This is useful when output sequence is LSB first but data need to be stored in higher bits of a word. 0: for PTM_IO instruction, CORE_OUT signals will be pushed from MSB of X register, and X register will be left shifted. For example, if PTM_IO output 8-bit signal, X[31] ->CORE_OUT[0], X[30] ->CORE_OUT[1] ..... X[24] ->CORE_OUT[7], and X will be left shifted by 8. When OFIFO is automatically poped, poped data will be left shifted by OSHIFT before set to X. This is useful when output sequence is MSB first but data need to be stored in lower bits of a word.
[1]	rw	1'h0	OAUTO	1: If left output bit counter reaches 0, OFIFO will be poped to X register automatically, and left output bit counter is reset to OLIMIT. 0: OFIFO will not be poped to X register automatically. PTM_SET instruction can pop OFIFO instead.
[0]	rw	1'h0	OFIFO	1: OFIFO enabled. OFIFO depth will be 4 if IFIFO also enabled, and be 8 if IFIFO disabled. 0: OFIFO disabled.
0x6C			**X1**	X register for core 1
[31:0]	rw	32'h0	VAL	Instant value of X register. Bit 31 to 16 is XH register. Bit 15 to 0 is XL register.
0x70			**Y1**	Y register for core 1
[31:0]	rw	32'h0	VAL	Instant value of Y register. Bit 31 to 16 is YH register. Bit 15 to 0 is YL register.
0x74			**A1**	A register for core 1
[31:16]			RSVD	
[15:0]	rw	16'h0	VAL	Instant value of A register.
0x78			**B1**	B register for core 1
[31:16]			RSVD	
[15:0]	rw	16'h0	VAL	Instant value of B register.
0x7C			**PC1**	PC register for core 1
[31:0]	r	32'h0	VAL	Instant value of PC(program counter).
0x80			**IFIFO1**	IFIFO entry for core 1
[31:0]	r	32'h0	DAT	Read this entry to pop IFIFO. Return 0 if IFIFO empty.
0x84			**OFIFO1**	OFIFO entry for core 1
[31:0]	w	32'h0	DAT	Write this entry to push OFIFO.
0x90			**CCR2**	Core 2 control register

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表 18-1: PTM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:24]	rw	8'h0	END1	Another TCM instruction index to end instruction sequence. After executes this instruction, current core will stop execution if REP=0, or restart from index 0 if REP!=0
[23:16]	rw	8'h0	END0	TCM instruction index to end instruction sequence. After executes this instruction, current core will stop execution if REP=0, or restart from index 0 if REP!=0
[15:8]	rw	8'h0	REP	Repetition times for instruction sequence. 0: No repetition. Core will stop after executes TCM instruction of index END0 or END1. 1~254: Finite Repetition. Core will restart from index 0 after executes TCM instruction of index END0 or END1, and REP will be decreased by 1, until REP become 0. 255: Infinite Repetion. Core will restart from index 0 after executes TCM instruction of index END0 or END1, and REP will not be decreased.
[7:0]	rw	8'h0	PSC	Prescaler factor. Core will execute at a divided rate of hclk/(PSC+1). All instructions will be affected.
0x94			**ICR2**	Input control register for core 2
[31]	r	1'h0	IFULL	1: IFIFO is full 0: IFIFO is not full
[30]	r	1'h1	IEMPTY	1: IFIFO is empty 0: IFIFO is not empty
[29]	r	1'h0	IOF	1: IFIFO overflow occurs, when new data is to be pushed into IFIFO but IFIFO is already full, thus the new data is discarded 0: IFIFO never overflow
[28:24]	rw	5'h0	ILIMIT	Input threshold for IFIFO auto push, valid when IAUTO=1. 0: Input threshold is 32 others: Input threshold is ILIMIT If accumulated input bit counter(named as Y_CNT) reaches or exceeds input threshold, input data stored in Y register will be pushed into IFIFO automatically, and accumulated input bit counter is cleared to 0.
[23:21]			RSVD	
[20:16]	rw	5'h0	ISHIFT	Shift bit count of Y register when Y is automatically pushed into IFIFO, valid when IAUTO=1. Data pushed into IFIFO is Y left shifted by ISHIFT if IRSH=0, or Y right shifted by ISHIFT if IRSH=1. Only valid for automatic IFIFO push of PTM_IO instruction. When pushing IFIFO by PTM_SET instruction, shift processing should be coded in the OP and IMM16 field of the instruction instead of ISHIFT.
[15:12]			RSVD	
[11:8]	rw	4'h0	IBASE	Input offset for this core. CORE_IN[n] = PTM_CH[(n+IBASE) round 16] For example, if IBASE=5, CORE_IN[0] = PTM_CH[5], CORE_IN[11] = PTM_CH[0], CORE_IN[15] = PTM_CH[4]
[7:4]			RSVD	
[3]	rw	1'h0	IBLOCK	1: Core execution is blocked if a new data is to be pushed into IFIFO but IFIFO is already full. Related instruction are PTM_IO and PTM_SET. Core execution will continue if the data can be successfully pushed into IFIFO after IFIFO been fetched by CPU or DMA. 0: Core execution will not be blocked, so IFIFO may overflow. New data will be discarded.

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表 18-1: PTM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[2]	rw	1'h0	IRSH	1: for PTM_IO instruction, Y register will be right shifted, and CORE_IN signals will be placed from MSB of Y register. For example, if PTM_IO input 8-bit signal, Y will be right shifted by 8, and CORE_IN[0]->Y[31], CORE_IN[1]->Y[30] ..... CORE_IN[7]->Y[24]. When Y is automatically pushed into IFIFO, pushed data will be additionally right shifted by ISHIFT. This is useful when input sequence is LSB first but data need to be stored in lower bits of a word. 0: for PTM_IO instruction, Y register will be left shifted, and CORE_IN data will be placed from LSB of Y register. For example, if PTM_IO input 8-bit signal, Y will be left shifted by 8, and CORE_IN[0]->Y[0], CORE_IN[1]->Y[1] ..... CORE_IN[7]->Y[7]. When Y is automatically pushed into IFIFO, pushed data will be additionally left shifted by ISHIFT. This is useful when input sequence is MSB first but data need to be stored in higher bits of a word.
[1]	rw	1'h0	IAUTO	1: If accumulated input bit counter reaches or exceeds input threshold, input data stored in Y register will be pushed into IFIFO automatically, and accumulated input bit counter is cleared to 0. 0: Y register will not be pushed into IFIFO automatically. PTM_SET instruction can push IFIFO instead.
[0]	rw	1'h0	IFIFO	1: IFIFO enabled. IFIFO depth will be 4 if OFIFO also enabled, and be 8 if OFIFO disabled. 0: IFIFO disabled.
0x98			**OCR2**	Output control register for core 2
[31]	r	1'h0	OFULL	1: OFIFO is full 0: OFIFO is not full
[30]	r	1'h1	OEMPTY	1: OFIFO is empty 0: OFIFO is not empty
[29]	r	1'h0	OUF	1: OFIFO underflow occurs, which means new data is to be poped from OFIFO but OFIFO is empty, thus the poped data is 0 0: OFIFO never underflow
[28:24]	rw	5'h0	OLIMIT	Output bit counter for OFIFO auto pop, valid when OAUTO=1. 0: Output bit counter is 32 others: Output bit counter is OLIMIT If left output bit counter(named as X_CNT) reaches 0, OFIFO will be poped to X register automatically, and left output bit counter is reset to OLIMIT.
[23:21]			RSVD	
[20:16]	rw	5'h0	OSHIFT	Shift bit count of OFIFO data when OFIFO is automatically poped into X register, valid when OAUTO=1. Data poped from OFIFO is left shifted by OSHIFT if ORSH=0, or right shifted by OSHIFT if ORSH=1, before storing into X register. Only valid for automatic OFIFO pop of PTM_IO instruction. When poping OFIFO by PTM_SET instruction, shift processing should be coded in the OP and IMM16 field of the instruction instead of OSHIFT.
[15:12]			RSVD	
[11:8]	rw	4'h0	OBASE	Output offset for this core. PTM_CH[(n+IBASE) round 16] = CORE_OUT[n] For example, if OBASE=5, PTM_CH[5] = CORE_OUT[0], PTM_CH[0] = CORE_OUT[11], PTM_CH[4] = CORE_OUT[15]
[7:4]			RSVD	

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表 18-1: PTM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[3]	rw	1'h0	OBLOCK	1: Core execution is blocked if a new data is to be poped from OFIFO but OFIFO is empty. Related instruction are PTM_IO and PTM_SET. Core execution will continue if data can be successfully poped from OFIFO after OFIFO been filled by CPU or DMA. 0: Core execution will not be blocked, so OFIFO may underflow. Poped data will be 0.
[2]	rw	1'h0	ORSH	1: for PTM_IO instruction, CORE_OUT signals will be pushed from LSB of X register, and X register will be right shifted. For example, if PTM_IO output 8-bit signal, X[0] ->CORE_OUT[0], X[1] ->CORE_OUT[1] ..... X[7] ->CORE_OUT[7], and X will be right shifted by 8. When OFIFO is automatically poped, poped data will be right shifted by OSHIFT before set to X. This is useful when output sequence is LSB first but data need to be stored in higher bits of a word. 0: for PTM_IO instruction, CORE_OUT signals will be pushed from MSB of X register, and X register will be left shifted. For example, if PTM_IO output 8-bit signal, X[31] ->CORE_OUT[0], X[30] ->CORE_OUT[1] ..... X[24] ->CORE_OUT[7], and X will be left shifted by 8. When OFIFO is automatically poped, poped data will be left shifted by OSHIFT before set to X. This is useful when output sequence is MSB first but data need to be stored in lower bits of a word.
[1]	rw	1'h0	OAUTO	1: If left output bit counter reaches 0, OFIFO will be poped to X register automatically, and left output bit counter is reset to OLIMIT. 0: OFIFO will not be poped to X register automatically. PTM_SET instruction can pop OFIFO instead.
[0]	rw	1'h0	OFIFO	1: OFIFO enabled. OFIFO depth will be 4 if IFIFO also enabled, and be 8 if IFIFO disabled. 0: OFIFO disabled.
0x9C			**X2**	X register for core 2
[31:0]	rw	32'h0	VAL	Instant value of X register. Bit 31 to 16 is XH register. Bit 15 to 0 is XL register.
0xA0			**Y2**	Y register for core 2
[31:0]	rw	32'h0	VAL	Instant value of Y register. Bit 31 to 16 is YH register. Bit 15 to 0 is YL register.
0xA4			**A2**	A register for core 2
[31:16]			RSVD	
[15:0]	rw	16'h0	VAL	Instant value of A register.
0xA8			**B2**	B register for core 2
[31:16]			RSVD	
[15:0]	rw	16'h0	VAL	Instant value of B register.
0xAC			**PC2**	PC register for core 2
[31:0]	r	32'h0	VAL	Instant value of PC(program counter).
0xB0			**IFIFO2**	IFIFO entry for core 2
[31:0]	r	32'h0	DAT	Read this entry to pop IFIFO. Return 0 if IFIFO empty.
0xB4			**OFIFO2**	OFIFO entry for core 2
[31:0]	w	32'h0	DAT	Write this entry to push OFIFO.
0xC0			**CCR3**	Core 3 control register

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表 18-1: PTM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[31:24]	rw	8'h0	END1	Another TCM instruction index to end instruction sequence. After executes this instruction, current core will stop execution if REP=0, or restart from index 0 if REP!=0
[23:16]	rw	8'h0	END0	TCM instruction index to end instruction sequence. After executes this instruction, current core will stop execution if REP=0, or restart from index 0 if REP!=0
[15:8]	rw	8'h0	REP	Repetition times for instruction sequence. 0: No repetition. Core will stop after executes TCM instruction of index END0 or END1. 1~254: Finite Repetition. Core will restart from index 0 after executes TCM instruction of index END0 or END1, and REP will be decreased by 1, until REP become 0. 255: Infinite Repetion. Core will restart from index 0 after executes TCM instruction of index END0 or END1, and REP will not be decreased.
[7:0]	rw	8'h0	PSC	Prescaler factor. Core will execute at a divided rate of hclk/(PSC+1). All instructions will be affected.
0xC4			**ICR3**	Input control register for core 3
[31]	r	1'h0	IFULL	1: IFIFO is full 0: IFIFO is not full
[30]	r	1'h1	IEMPTY	1: IFIFO is empty 0: IFIFO is not empty
[29]	r	1'h0	IOF	1: IFIFO overflow occurs, when new data is to be pushed into IFIFO but IFIFO is already full, thus the new data is discarded 0: IFIFO never overflow
[28:24]	rw	5'h0	ILIMIT	Input threshold for IFIFO auto push, valid when IAUTO=1. 0: Input threshold is 32 others: Input threshold is ILIMIT If accumulated input bit counter(named as Y_CNT) reaches or exceeds input threshold, input data stored in Y register will be pushed into IFIFO automatically, and accumulated input bit counter is cleared to 0.
[23:21]			RSVD	
[20:16]	rw	5'h0	ISHIFT	Shift bit count of Y register when Y is automatically pushed into IFIFO, valid when IAUTO=1. Data pushed into IFIFO is Y left shifted by ISHIFT if IRSH=0, or Y right shifted by ISHIFT if IRSH=1. Only valid for automatic IFIFO push of PTM_IO instruction. When pushing IFIFO by PTM_SET instruction, shift processing should be coded in the OP and IMM16 field of the instruction instead of ISHIFT.
[15:12]			RSVD	
[11:8]	rw	4'h0	IBASE	Input offset for this core. CORE_IN[n] = PTM_CH[(n+IBASE) round 16] For example, if IBASE=5, CORE_IN[0] = PTM_CH[5], CORE_IN[11] = PTM_CH[0], CORE_IN[15] = PTM_CH[4]
[7:4]			RSVD	
[3]	rw	1'h0	IBLOCK	1: Core execution is blocked if a new data is to be pushed into IFIFO but IFIFO is already full. Related instruction are PTM_IO and PTM_SET. Core execution will continue if the data can be successfully pushed into IFIFO after IFIFO been fetched by CPU or DMA. 0: Core execution will not be blocked, so IFIFO may overflow. New data will be discarded.

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表 18-1: PTM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[2]	rw	1'h0	IRSH	1: for PTM_IO instruction, Y register will be right shifted, and CORE_IN signals will be placed from MSB of Y register. For example, if PTM_IO input 8-bit signal, Y will be right shifted by 8, and CORE_IN[0]->Y[31], CORE_IN[1]->Y[30] ..... CORE_IN[7]->Y[24]. When Y is automatically pushed into IFIFO, pushed data will be additionally right shifted by ISHIFT. This is useful when input sequence is LSB first but data need to be stored in lower bits of a word. 0: for PTM_IO instruction, Y register will be left shifted, and CORE_IN data will be placed from LSB of Y register. For example, if PTM_IO input 8-bit signal, Y will be left shifted by 8, and CORE_IN[0]->Y[0], CORE_IN[1]->Y[1] ..... CORE_IN[7]->Y[7]. When Y is automatically pushed into IFIFO, pushed data will be additionally left shifted by ISHIFT. This is useful when input sequence is MSB first but data need to be stored in higher bits of a word.
[1]	rw	1'h0	IAUTO	1: If accumulated input bit counter reaches or exceeds input threshold, input data stored in Y register will be pushed into IFIFO automatically, and accumulated input bit counter is cleared to 0. 0: Y register will not be pushed into IFIFO automatically. PTM_SET instruction can push IFIFO instead.
[0]	rw	1'h0	IFIFO	1: IFIFO enabled. IFIFO depth will be 4 if OFIFO also enabled, and be 8 if OFIFO disabled. 0: IFIFO disabled.
0xC8			**OCR3**	Output control register for core 3
[31]	r	1'h0	OFULL	1: OFIFO is full 0: OFIFO is not full
[30]	r	1'h1	OEMPTY	1: OFIFO is empty 0: OFIFO is not empty
[29]	r	1'h0	OUF	1: OFIFO underflow occurs, which means new data is to be poped from OFIFO but OFIFO is empty, thus the poped data is 0 0: OFIFO never underflow
[28:24]	rw	5'h0	OLIMIT	Output bit counter for OFIFO auto pop, valid when OAUTO=1. 0: Output bit counter is 32 others: Output bit counter is OLIMIT If left output bit counter(named as X_CNT) reaches 0, OFIFO will be poped to X register automatically, and left output bit counter is reset to OLIMIT.
[23:21]			RSVD	
[20:16]	rw	5'h0	OSHIFT	Shift bit count of OFIFO data when OFIFO is automatically poped into X register, valid when OAUTO=1. Data poped from OFIFO is left shifted by OSHIFT if ORSH=0, or right shifted by OSHIFT if ORSH=1, before storing into X register. Only valid for automatic OFIFO pop of PTM_IO instruction. When poping OFIFO by PTM_SET instruction, shift processing should be coded in the OP and IMM16 field of the instruction instead of OSHIFT.
[15:12]			RSVD	
[11:8]	rw	4'h0	OBASE	Output offset for this core. PTM_CH[(n+IBASE) round 16] = CORE_OUT[n] For example, if OBASE=5, PTM_CH[5] = CORE_OUT[0], PTM_CH[0] = CORE_OUT[11], PTM_CH[4] = CORE_OUT[15]
[7:4]			RSVD	

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表 18-1: PTM 寄存器映射表（续）

Offset	Attribute	Reset Value	Register Name	Register Description
[3]	rw	1'h0	OBLOCK	1: Core execution is blocked if a new data is to be poped from OFIFO but OFIFO is empty. Related instruction are PTM_IO and PTM_SET. Core execution will continue if data can be successfully poped from OFIFO after OFIFO been filled by CPU or DMA. 0: Core execution will not be blocked, so OFIFO may underflow. Poped data will be 0.
[2]	rw	1'h0	ORSH	1: for PTM_IO instruction, CORE_OUT signals will be pushed from LSB of X register, and X register will be right shifted. For example, if PTM_IO output 8-bit signal, X[0] ->CORE_OUT[0], X[1] ->CORE_OUT[1] ..... X[7] ->CORE_OUT[7], and X will be right shifted by 8. When OFIFO is automatically poped, poped data will be right shifted by OSHIFT before set to X. This is useful when output sequence is LSB first but data need to be stored in higher bits of a word. 0: for PTM_IO instruction, CORE_OUT signals will be pushed from MSB of X register, and X register will be left shifted. For example, if PTM_IO output 8-bit signal, X[31] ->CORE_OUT[0], X[30] ->CORE_OUT[1] ..... X[24] ->CORE_OUT[7], and X will be left shifted by 8. When OFIFO is automatically poped, poped data will be left shifted by OSHIFT before set to X. This is useful when output sequence is MSB first but data need to be stored in lower bits of a word.
[1]	rw	1'h0	OAUTO	1: If left output bit counter reaches 0, OFIFO will be poped to X register automatically, and left output bit counter is reset to OLIMIT. 0: OFIFO will not be poped to X register automatically. PTM_SET instruction can pop OFIFO instead.
[0]	rw	1'h0	OFIFO	1: OFIFO enabled. OFIFO depth will be 4 if IFIFO also enabled, and be 8 if IFIFO disabled. 0: OFIFO disabled.
0xCC			**X3**	X register for core 3
[31:0]	rw	32'h0	VAL	Instant value of X register. Bit 31 to 16 is XH register. Bit 15 to 0 is XL register.
0xD0			**Y3**	Y register for core 3
[31:0]	rw	32'h0	VAL	Instant value of Y register. Bit 31 to 16 is YH register. Bit 15 to 0 is YL register.
0xD4			**A3**	A register for core 3
[31:16]			RSVD	
[15:0]	rw	16'h0	VAL	Instant value of A register.
0xD8			**B3**	B register for core 3
[31:16]			RSVD	
[15:0]	rw	16'h0	VAL	Instant value of B register.
0xDC			**PC3**	PC register for core 3
[31:0]	r	32'h0	VAL	Instant value of PC(program counter).
0xE0			**IFIFO3**	IFIFO entry for core 3
[31:0]	r	32'h0	DAT	Read this entry to pop IFIFO. Return 0 if IFIFO empty.
0xE4			**OFIFO3**	OFIFO entry for core 3
[31:0]	w	32'h0	DAT	Write this entry to push OFIFO.

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